High Common-Mode Voltage, Single-Supply Difference Amplifier

AD8203

FEATURES

High common-mode voltage range
–6 V to +30 V at a 5 V supply voltage
Operating temperature range: –40°C to +125°C
Supply voltage range: 3.5 V to 12 V
Low-pass filter (1-pole or 2-pole)
Excellent ac and dc performance
- **±1 mV voltage offset (8-lead SOIC)**
- **±1 ppm/°C typical gain drift**
- **80 dB CMRR minimum dc to 10 kHz**

APPLICATIONS

Transmission control
Diesel injection control
Engine management
Adaptive suspension control
Vehicle dynamics control

GENERAL DESCRIPTION

The AD8203 is a single-supply difference amplifier for amplifying and low-pass filtering small differential voltages in the presence of a large common-mode voltage (CMV). The input CMV range extends from −6 V to +30 V at a typical supply voltage of 5 V.

The AD8203 is available in die and packaged form. The MSOP and SOIC packages are specified over a wide temperature range, from −40°C to +125°C, while the die is specified over a wider temperature range, from −40°C to +150°C, making the AD8203 well-suited for use in many automotive platforms.

Automotive platforms demand precision components for better system control. The AD8203 provides excellent ac and dc performance keeping errors to a minimum in the user's system. Typical offset and gain drift in the SOIC package are 0.3 µV/°C and 1 ppm/°C, respectively. Typical offset and gain drift in the MSOP package are 2 µV/°C and 1 ppm/°C, respectively. The device also delivers a minimum CMRR of 80 dB from dc to 10 kHz.

The AD8203 features an externally accessible 100 kΩ resistor at the output of the Preamp A1, which can be used for low-pass filter applications and for establishing gains other than 14.

FUNCTIONAL BLOCK DIAGRAMS

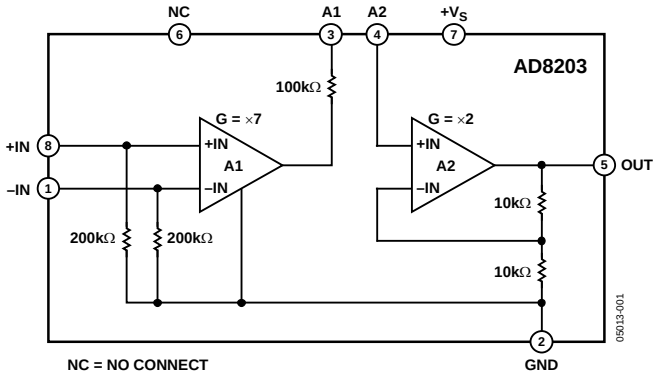


Figure 1. Functional Block Diagram

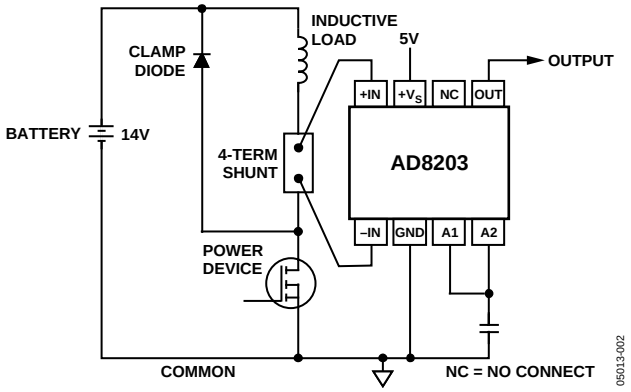


Figure 2. High Line Current Sensor

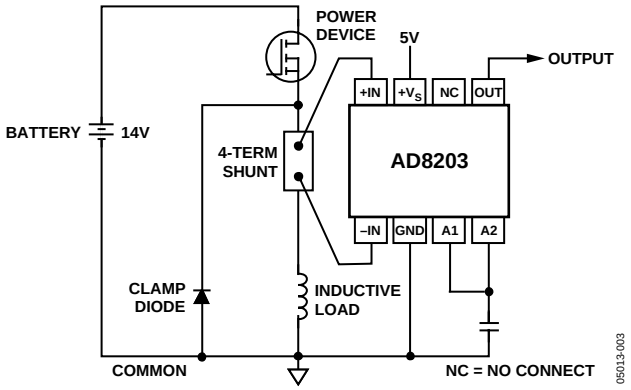


Figure 3. Low Line Current Sensor

Rev. B
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **© 2005 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

10/05—Rev. A to Rev. B

Added SOIC Package ..... Universal
Replaced Figure 23 8
Added Figure 24 to Figure 29 9
Changes to Theory of Operation Section 12
Added Figure 41 12
Updated Outline Dimensions 17
Changes to Ordering Guide 17

2/05—Rev. 0 to Rev. A

Changes to Specifications Table 3
Changes to Caption on Figure 6 and Figure 8 6
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Added Figure 14 to Figure 23 7
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Changes to Ordering Guide 13

10/04—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

T_A = operating temperature range, V_S = 5 V, unless otherwise noted.

Table 1.

		AD8203 SOIC			AD8203 MSOP			AD8203 Die			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SYSTEM GAIN											
Initial			14			14			14		V/V
Error	0.02 ≤ V_{OUT} ≤ 4.8 V dc @ 25°C	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	%
vs. Temperature			1	20		1	25		1	30	ppm/°C
VOLTAGE OFFSET											
Input Offset (RTI)	V_{CM} = 0.15 V; 25°C	−1		+1	−2		+2	−1		+1	mV
vs. Temperature	−40°C to +125°C	−10	+0.3	+10	−20	+2	+20	−10	+0.3	+10	µV/°C
	−40°C to +150°C							−15	+5	+15	µV/°C
INPUT											
Input Impedance											
Differential		260	320	380	260	320	380	260	320	380	kΩ
Common Mode		130	160	190	130	160	190	130	160	190	kΩ
CMV	Continuous	−6		+30	−6		+30	−6		+30	V
CMRR[1]	V_{CM} = −6 V to +30 V										
	f = dc	82			82			82			dB
	f = 1 kHz	82			82			82			dB
	f = 10 kHz[2]	80			80			80			dB
PREAMPLIFIER											
Gain			7			7			7		V/V
Gain Error		−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	%
Output Voltage Range		0.02		4.8	0.02		4.8	0.02		4.8	V
Output Resistance		97	100	103	97	100	103	97	100	103	kΩ
OUTPUT BUFFER											
Gain			2			2			2		V/V
Gain Error	0.02 ≤ V_{OUT} ≤ 4.8 V dc	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	%
Output Voltage Range		0.02		4.8	0.02		4.8	0.02		4.8	V
Input Bias Current			40			40			40		nA
Output Resistance			2			2			2		Ω
DYNAMIC RESPONSE											
System Bandwidth	V_{IN} = 0.01 V p-p, V_{OUT} = 0.14 V p-p	40	60		40	60		40	60		kHz
Slew Rate	V_{IN} = 0.28 V, V_{OUT} = 4 V step		0.33			0.33			0.33		V/µs
NOISE											
0.1 Hz to 10 Hz			10			10			10		µV p-p
Spectral Density, 1 kHz (RTI)			300			300			300		nV/√Hz
POWER SUPPLY											
Operating Range		3.5		12	3.5		12	3.5		12	V
Quiescent Current vs. Temperature	V_O = 0.1 V dc		0.25	1.0		0.25	1.0		0.25	1.0	mA
PSRR	V_S = 3.5 V to 12 V	75	83		75	83		75	83		dB
TEMPERATURE RANGE											
For Specified Performance		−40		+125	−40		+125	−40		+150	°C

[1] Source imbalance <2 Ω.

[2] The AD8203 preamplifier exceeds 80 dB CMRR at 10 kHz. However, since the signal is available only by way of a 100 kΩ resistor, even the small amount of pin-to-pin capacitance between Pin 1, Pin 8 and Pin 3, Pin 4 may couple an input common-mode signal larger than the greatly attenuated preamplifier output. The effect of pin-to-pin coupling may be neglected in all applications by using filter capacitors at Node 3.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	12.5 V
Transient Input Voltage (400 ms)	44 V
Continuous Input Voltage (Common Mode)	35 V
Reversed Supply Voltage Protection	0.3 V
Operating Temperature Range	
Die	−40°C to +150°C
SOIC	−40°C to +125°C
MSOP	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Output Short-Circuit Duration	Indefinite
Lead Temperature Range (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

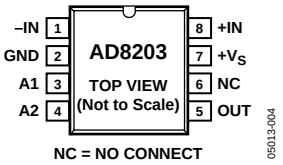


Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	X	Y
1	−IN	−409.0	−205.2
2	GND	−244.6	−413.0
3	A1	+229.4	−413.0
4	A2	+410.0	−308.6
5	OUT	+410.0	+272.4
6	NC	NA	NA
7	$+V_S$	+121.0	+417.0
8	+IN	−409.0	+205.2

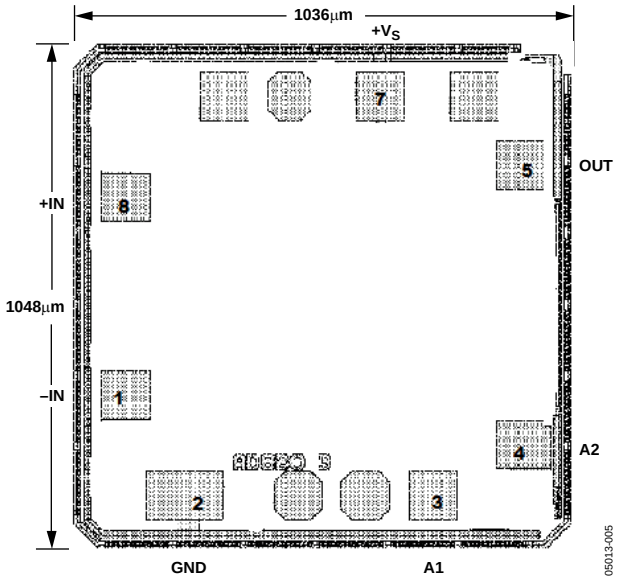


Figure 5. Metallization Photograph

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, V_{CM} = 0 V, R_L = 10 kΩ, unless otherwise noted.

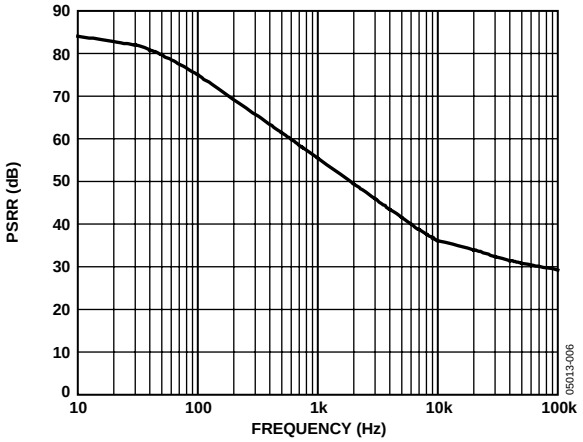


Figure 6. Power Supply Rejection Ratio vs. Frequency for Common-Mode Range −6 V to +30 V

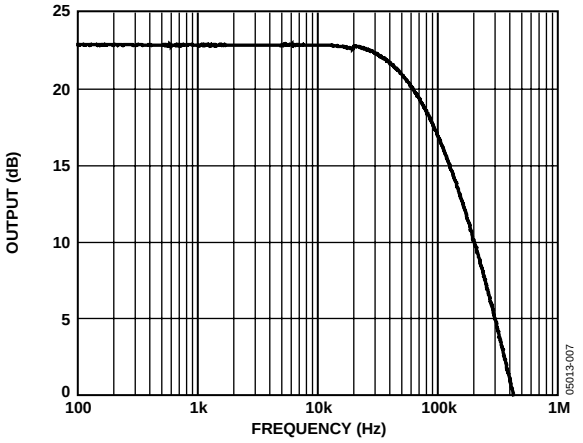


Figure 7. Bandwidth

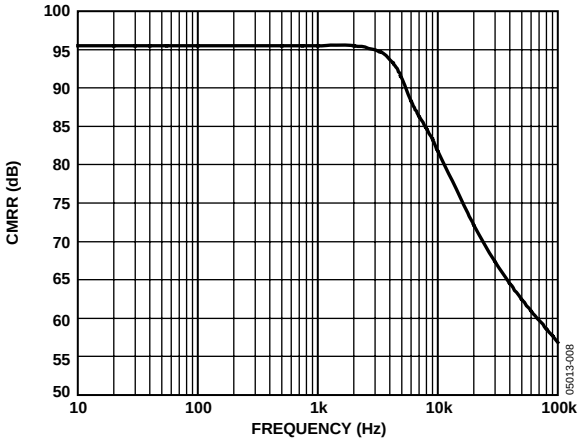


Figure 8. Common-Mode Rejection Ratio vs. Frequency for Common-Mode Range −6 V to +30 V

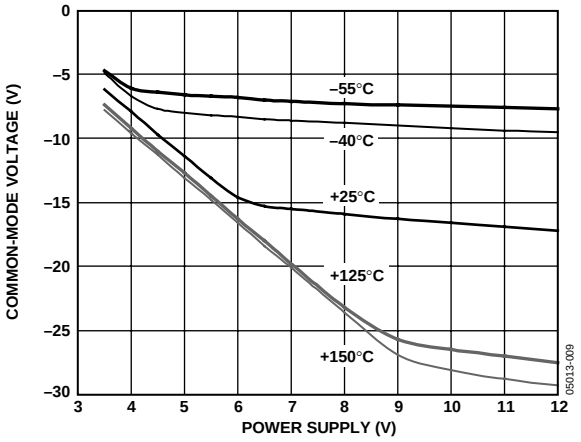


Figure 9. Negative Common-Mode Voltage vs. Voltage Supply

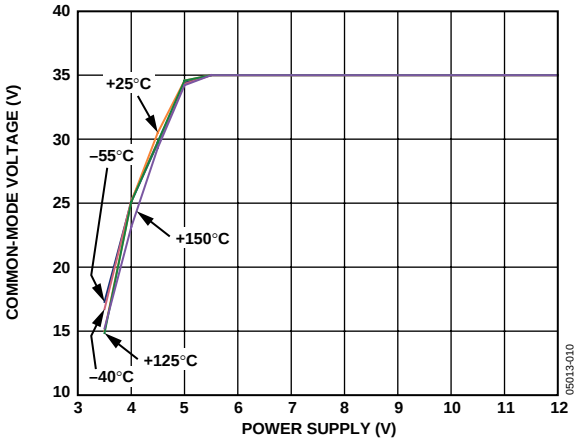


Figure 10. Positive Common-Mode Voltage vs. Voltage Supply

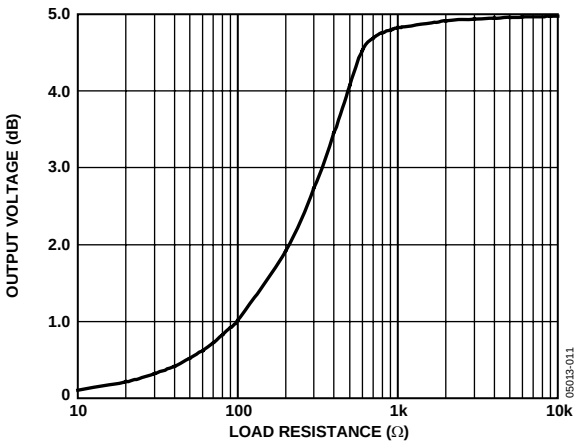


Figure 11. Output Swing vs. Load Resistance

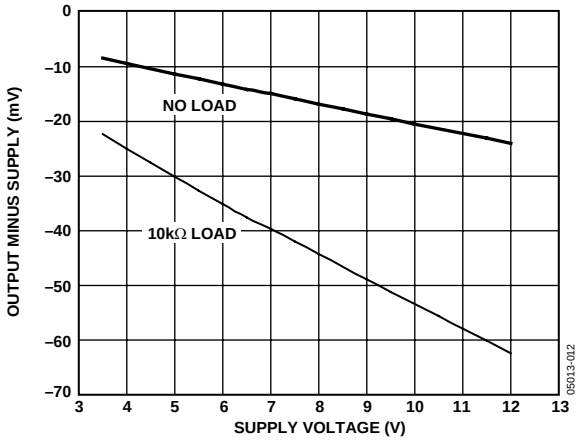


Figure 12. Swing Minus Supply vs. Supply Voltage

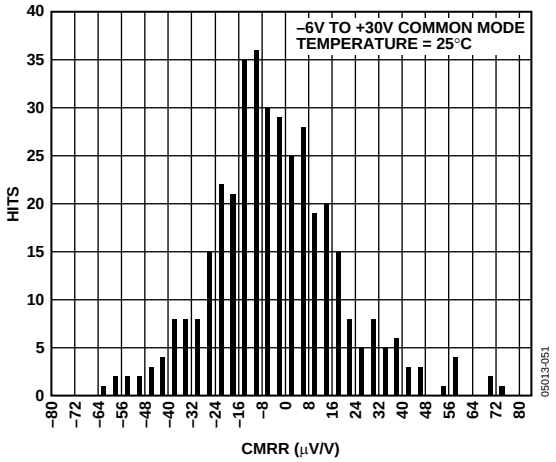


Figure 15. CMRR Distribution, Temperature = 25°C

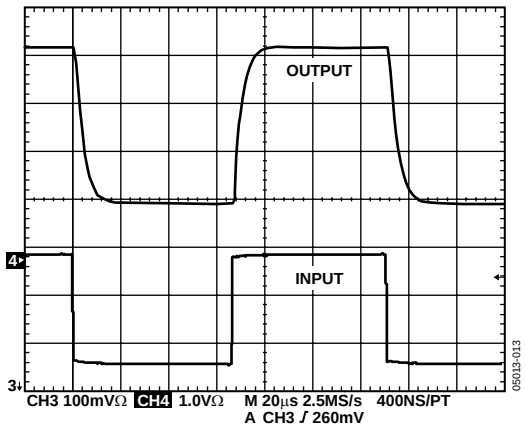


Figure 13. Pulse Response

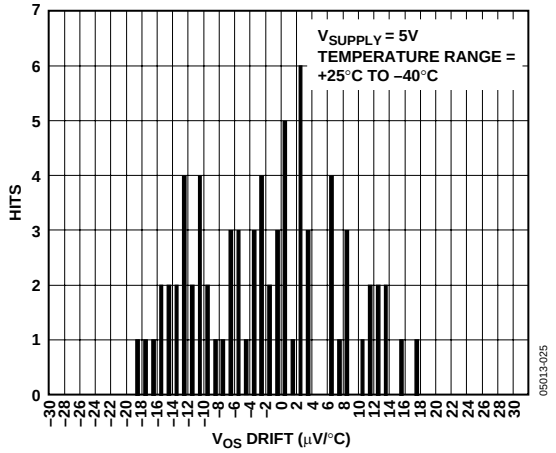


Figure 16. Offset Drift Distribution, MSOP, Temperature Range = +25°C to –40°C

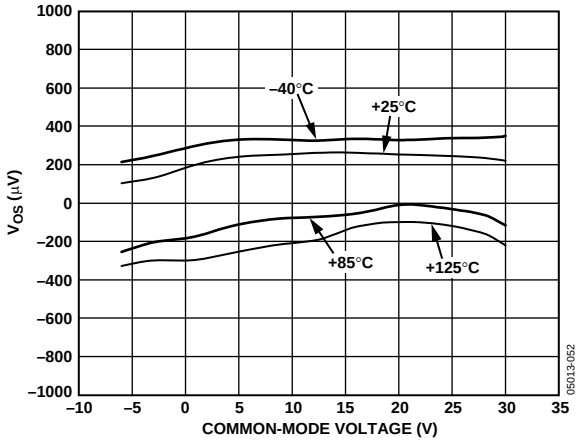


Figure 14. V_{OS} vs. Common-Mode Voltage

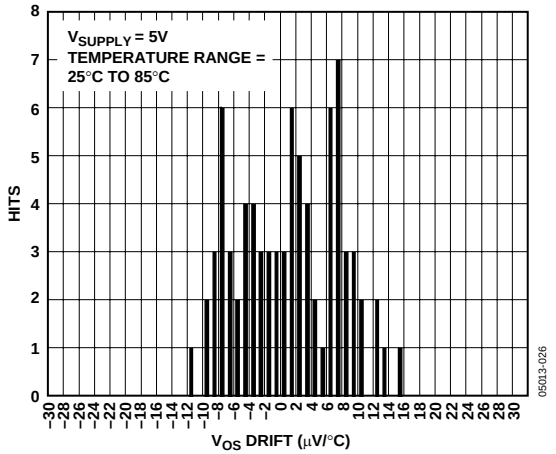


Figure 17. Offset Drift Distribution, MSOP, Temperature Range = 25°C to 85°C

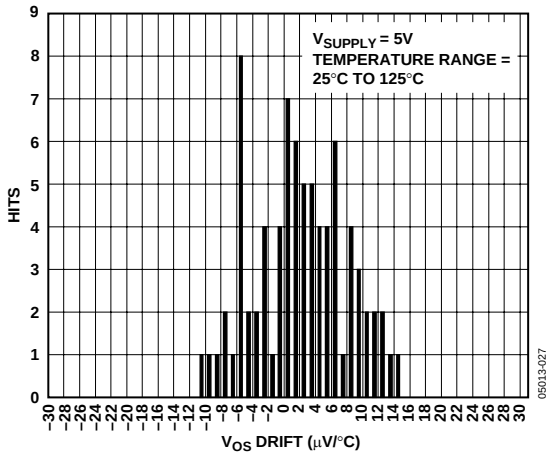


Figure 18. V_{OS} Distribution, MSOP, Temperature Range = 25°C to 125°C

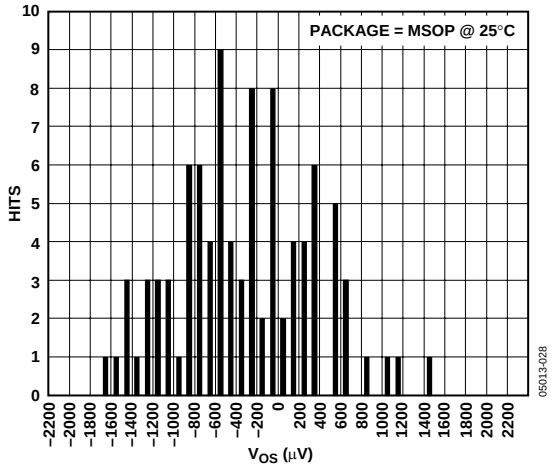


Figure 19. V_{OS} Distribution, MSOP, Temperature = 25°C

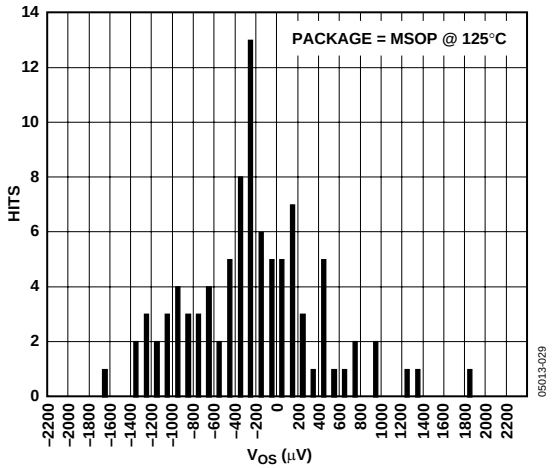


Figure 20. V_{OS} Distribution, MSOP, Temperature = 125°C

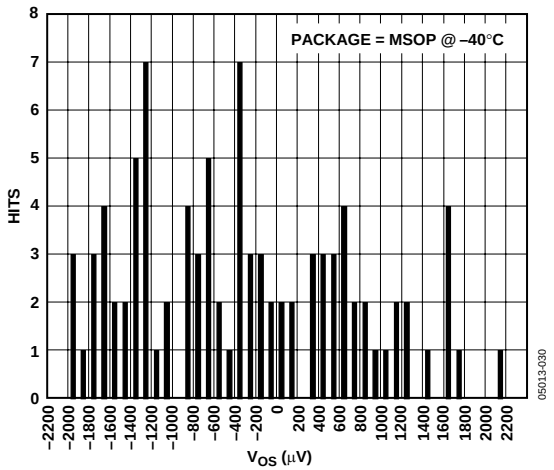


Figure 21. V_{OS} Distribution, MSOP, Temperature = –40°C

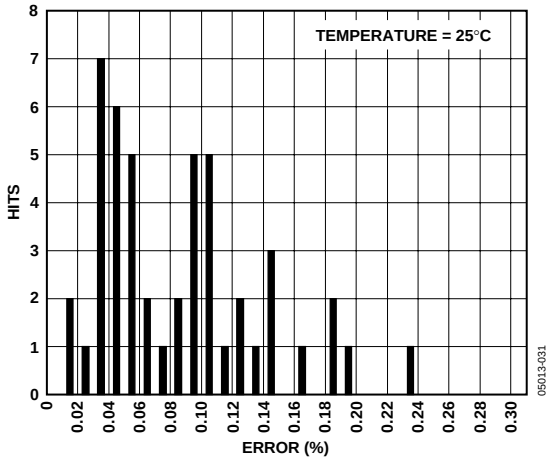


Figure 22. MSOP Gain Accuracy, Temperature = 25°C

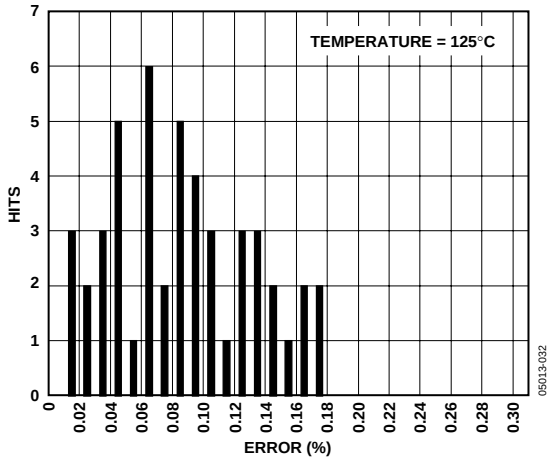


Figure 23. MSOP Gain Accuracy, Temperature = 125°C

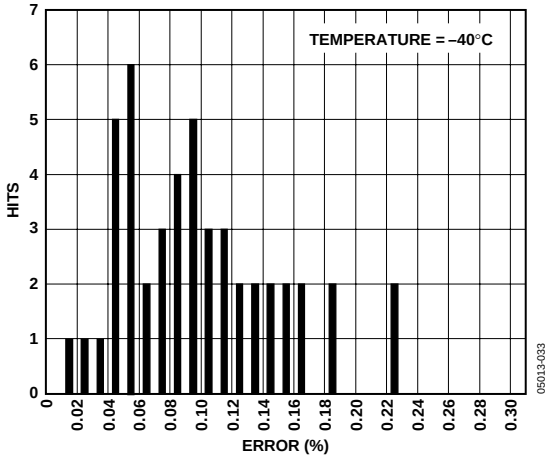


Figure 24. MSOP Gain Accuracy, Temperature = –40°C

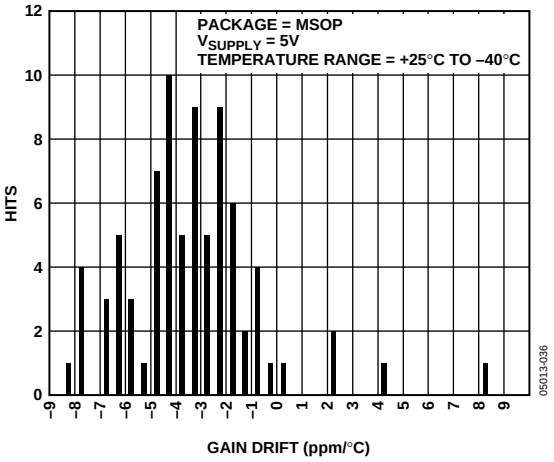


Figure 25. Gain Drift Distribution, Temperature Range = +25°C to –40°C

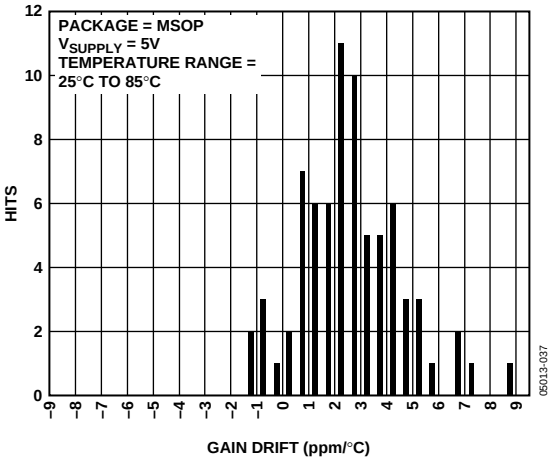


Figure 26. Gain Drift Distribution, MSOP, Temperature Range = 25°C to 85°C

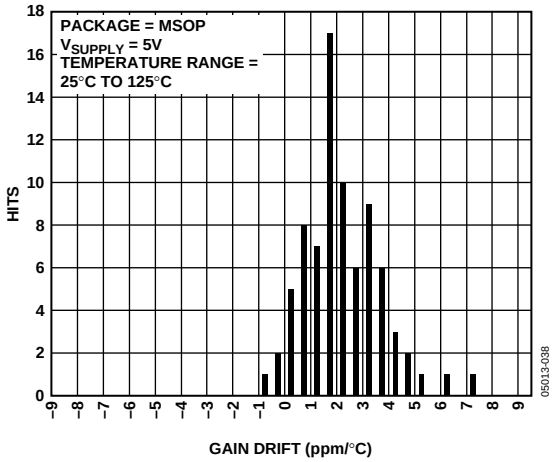


Figure 27. Gain Drift Distribution, MSOP, Temperature Range = 25°C to 125°C

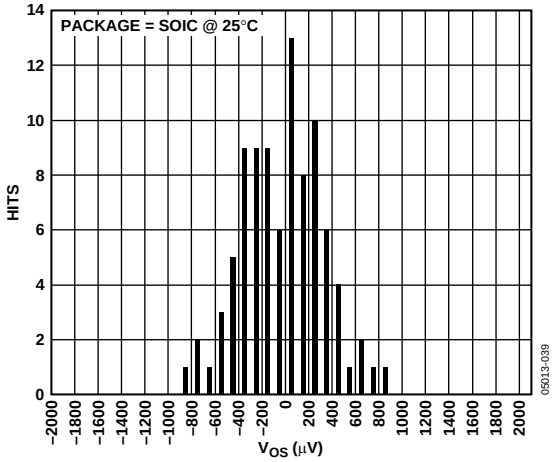


Figure 28. V_{OS} Distribution, SOIC, Temperature = 25°C

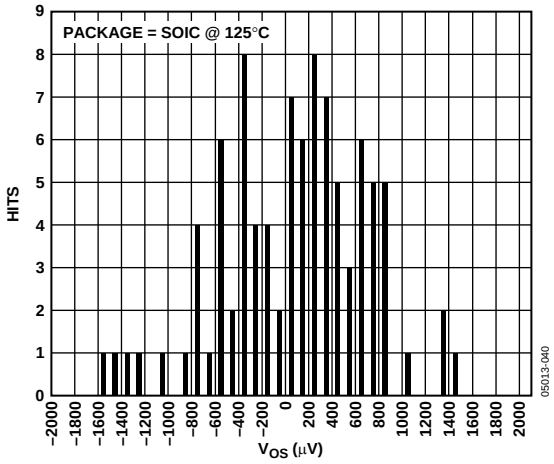


Figure 29. V_{OS} Distribution, SOIC, Temperature = 125°C

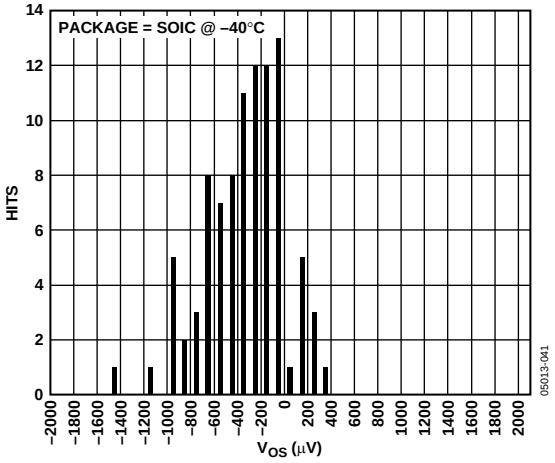


Figure 30. V_{OS} Distribution, SOIC, Temperature = −40°C

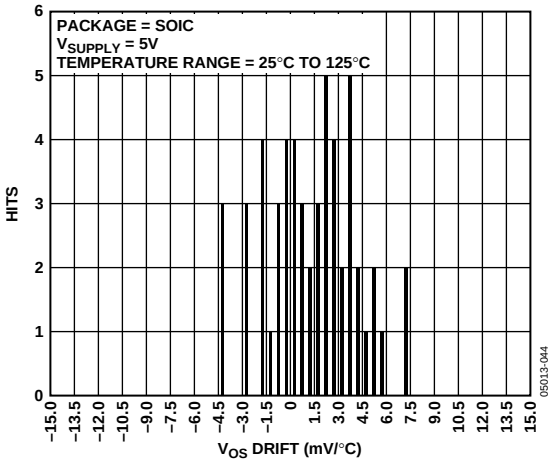


Figure 33. Offset Drift Distribution, SOIC, Temperature Range = +25°C to 125°C

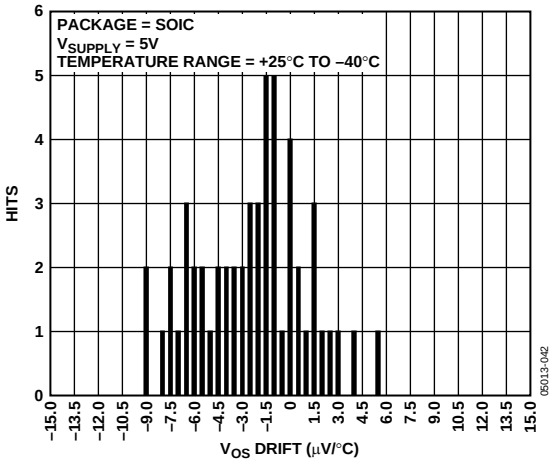


Figure 31. Offset Drift Distribution, SOIC, Temperature Range = +25°C to −40°C

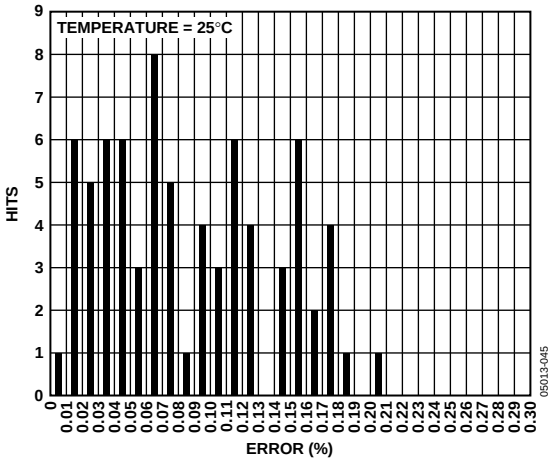


Figure 34. Gain Accuracy, SOIC, Temperature = 25°C

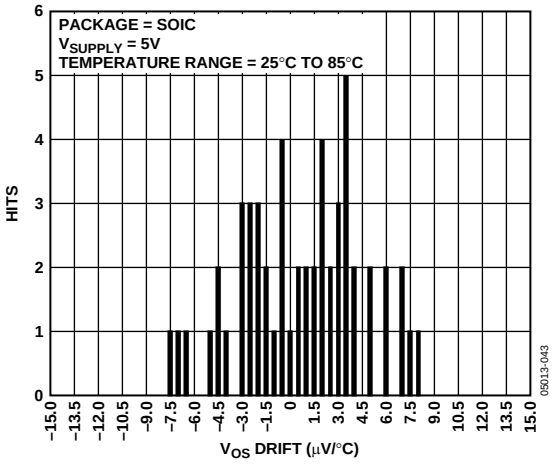


Figure 32. Offset Drift Distribution, SOIC, Temperature Range = 25°C to 85°C

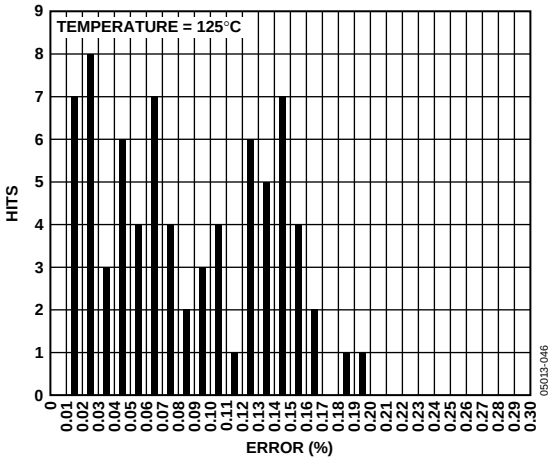


Figure 35. Gain Accuracy, SOIC, Temperature = 125°C

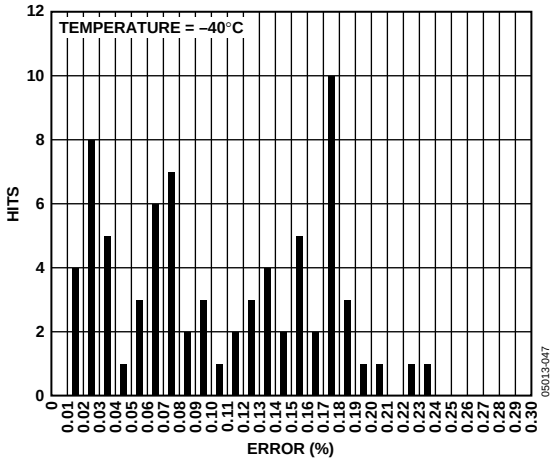


Figure 36. Gain Accuracy, SOIC, Temperature = –40°C

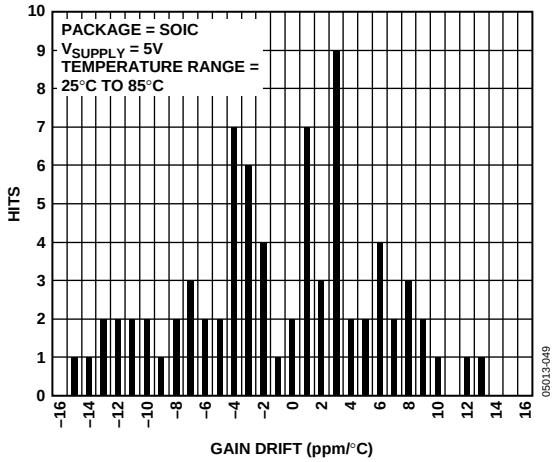


Figure 38. Gain Drift Distribution, SOIC, Temperature Range = 25°C to 85°C

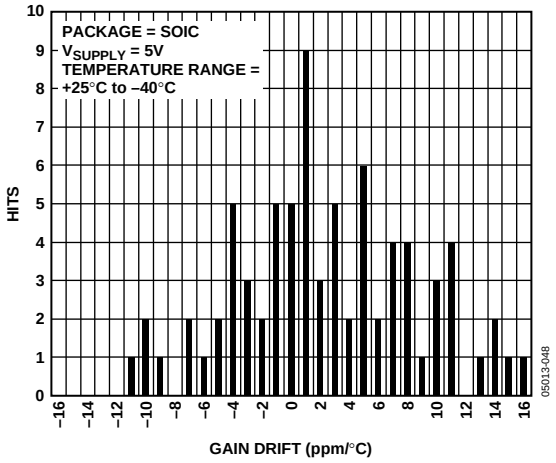


Figure 37. Gain Drift Distribution, SOIC, Temperature Range = +25°C to –40°C

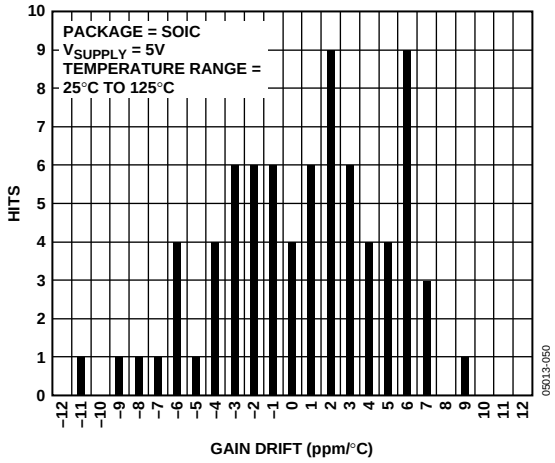


Figure 39. Gain Drift Distribution, SOIC, Temperature Range = 25°C to 125°C

THEORY OF OPERATION

The AD8203 consists of a preamp and buffer, arranged as shown in Figure 40. Like-named resistors have equal values.

The preamp incorporates a dynamic bridge (subtractor) circuit. Identical networks (within the shaded areas) consisting of R_A, R_B, R_C, and R_G, attenuate input signals applied to Pin 1 and Pin 8. Note that when equal amplitude signals are asserted at Input 1 and Input 8, and the output of A1 is equal to the common potential (that is, 0), the two attenuators form a balanced-bridge network. When the bridge is balanced, the differential input voltage at A1, and thus its output, is 0.

Any common-mode voltage applied to both inputs keeps the bridge balanced and the A1 output at 0. Because the resistor networks are carefully matched, the common-mode signal rejection approaches this ideal state.

However, if the signals applied to the inputs differ, the result is a difference at the input to A1. A1 responds by adjusting its output to drive R_B, by way of R_G, to adjust the voltage at its inverting input until it matches the voltage at its noninverting input.

By attenuating voltages at Pin 1 and Pin 8, the amplifier inputs are held within the power supply range, even if Pin 1 and Pin 8 input levels exceed the supply or fall below common (ground). The input network also attenuates normal (differential) mode voltages. R_C and R_G form an attenuator that scales A1 feedback, forcing large output signals to balance relatively small differential inputs. The resistor ratios establish the preamp gain at 7.

Because the differential input signal is attenuated and then amplified to yield an overall gain of 7, Amplifier A1 operates at a higher noise gain, multiplying deficiencies such as input offset voltage and noise with respect to Pin 1 and Pin 8.

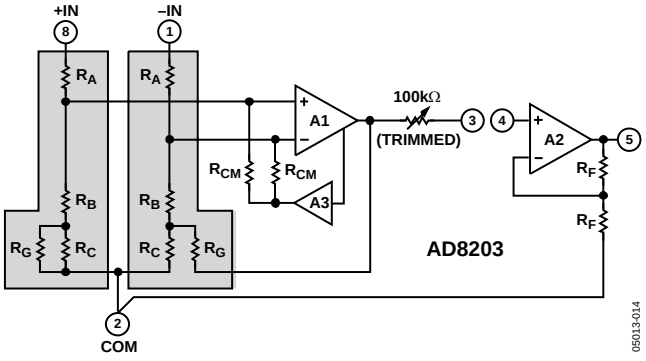


Figure 40. Simplified Schematic

To minimize these errors while extending the common-mode range, a dedicated feedback loop is used to reduce the range of common-mode voltage applied to A1 for a given overall range at the inputs. By offsetting the range of voltage applied to the compensator, the input common-mode range is also offset to include voltages more negative than the power supply. The A3 amplifier detects the common-mode signal applied to A1 and adjusts the voltage on the matched R_{CM} resistors to reduce the common-mode voltage range at the A1 inputs. By adjusting the common voltage of these resistors, the common-mode input range is extended while, at the same time, the normal mode signal attenuation is reduced, leading to better performance referred to input.

The output of the dynamic bridge taken from A1 is connected to Pin 3 by way of a 100 kΩ series resistor, provided for low-pass filtering and gain adjustment. The resistors in the input networks of the preamp and the buffer feedback resistors are ratio-trimmed for high accuracy.

The output of the preamp drives a gain-of-2 buffer amplifier, A2, implemented with carefully matched feedback resistors R_F.

The 2-stage system architecture of the AD8203 enables the user to incorporate a low-pass filter prior to the output buffer. By separating the gain into two stages, a full-scale, rail-to-rail signal from the preamp can be filtered at Pin 3, and a half-scale signal, resulting from filtering, can be restored to full scale by the output buffer amp. The source resistance seen by the inverting input of A2 is approximately 100 kΩ to minimize the effects of the input bias current of A2. However, this current is quite small, and errors resulting from applications that mismatch the resistance are correspondingly small.

The A2 input bias current has a typical value of 40 nA, however, this can increase under certain conditions. For example, if the input signal to the A2 amplifier is $V_{CC}/2$, the output attempts to go to V_{CC} due to the gain of 2. However, the output saturates because the maximum specified voltage for correct operation is 200 mV below V_{CC}. Under these conditions the total input bias current increases (see Figure 41 for more information).

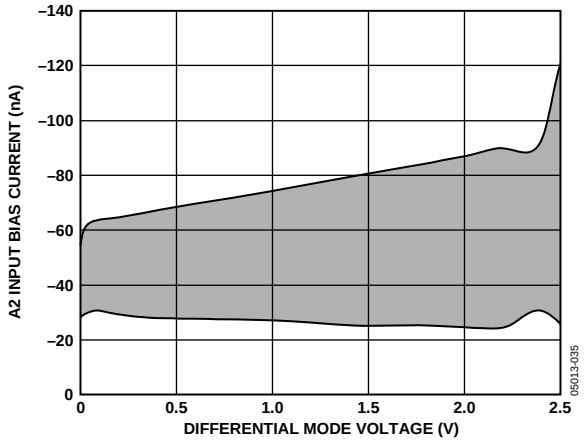


Figure 41. A2 Input Bias Current vs. Input Voltage and Temperature. The Shaded Area Is the Bias Current from –40°C to +125°C.

An increase in the A2 bias current, in addition to the output saturation voltage of A1, directly affects the output voltage of

the AD8203 system (Pin 3 and Pin 4 shorted). An example of how to calculate the correct output voltage swing of the AD8203, by taking all variables into account, follows:

- Amplifier A1 output saturation potential can go as low as 20 mV at its output.
- A2 typical input bias current of 40 nA multiplied by the 100 kΩ preamplifier output resistor produces

  40 nA × 100 kΩ = 4 mV at the A2 input
- Total voltage at the A2 input equals the output saturation voltage of A1 combined with the voltage error generated by the input bias current

  20 mV + 4 mV = 24 mV
- The total error at the input of A2, 24 mV, multiplied by the buffer gain generates a resulting error of 48 mV at the output of the buffer. This is the AD8203 system output low saturation potential.
- The high output voltage range of the AD8203 is specified as 4.8 V. Therefore, assuming a typical A2 input bias current, the output voltage range for the AD8203 is 48 mV to 4.8 V.

For an example of the effect of changes in A2 input bias current vs. applied input potentials, see Figure 41. The change in bias current causes a change in error voltage at the input of the buffer amplifier. This results in a change in overall error potential at the output of the buffer amplifier.

APPLICATIONS

The AD8203 difference amplifier is intended for applications that require extracting a small differential signal in the presence of large common-mode voltages. The input resistance is nominally 320 kΩ, and the device can tolerate common-mode voltages higher than the supply voltage and lower than ground.

The open collector output stage sources current to within 20 mV of ground and to within 200 mV of V_S.

CURRENT SENSING

High Line, High Current Sensing

Basic automotive applications making use of the large common-mode range are shown in Figure 2 and Figure 3. The capability of the device to operate as an amplifier in primary battery supply circuits is shown in Figure 2. Figure 3 illustrates the ability of the device to withstand voltages below system ground.

Low Current Sensing

The AD8203 is also used in low current sensing applications, such as the 4 to 20 mA current loop shown in Figure 42. In such applications, the relatively large shunt resistor can degrade the common-mode rejection. Adding a resistor of equal value on the low impedance side of the input corrects this error.

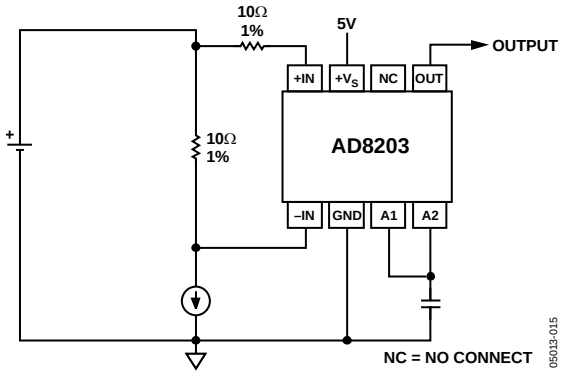


Figure 42. 4 to 20 mA Current Loop Receiver

GAIN ADJUSTMENT

The default gain of the preamplifier and buffer are ×7 and ×2, respectively, resulting in a composite gain of ×14. With the addition of external resistor(s) or trimmer(s), the gain can be lowered, raised, or finely calibrated.

Gains Less Than 14

Since the preamplifier has an output resistance of 100 kΩ, an external resistor connected from Pin 3 and Pin 4 to GND decreases the gain by a factor $R_{EXT}/(100\ k\Omega + R_{EXT})$, as shown in Figure 43.

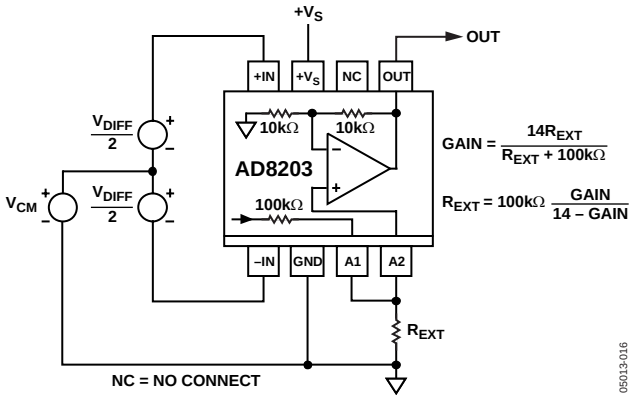


Figure 43. Adjusting for Gains < 14

The overall bandwidth is unaffected by changes in gain by using this method, although there may be a small offset voltage due to the imbalance in source resistances at the input to the buffer. This can often be ignored, but if desired, it can be nulled by inserting a resistor equal to 100 kΩ minus the parallel sum of R_{EXT} and 100 kΩ, in series with Pin 4. For example, with R_{EXT} = 100 kΩ (yielding a composite gain of ×7), the optional offset nulling resistor is 50 kΩ.

Gains Greater Than 14

Connecting a resistor from the output of the buffer amplifier to its noninverting input, as shown in Figure 44, increases the gain. The gain is now multiplied by the factor $R_{EXT}/(R_{EXT} - 100\ k\Omega)$; for example, the gain is doubled for R_{EXT} = 200 kΩ. Overall gains as high as 50 are achievable this way. Note that the accuracy of the gain becomes critically dependent on the resistor value at high gains. Also, the effective input offset voltage at Pin 1 and Pin 8 (about six times the actual offset of A1) limits the part's use in high gain, dc-coupled applications.

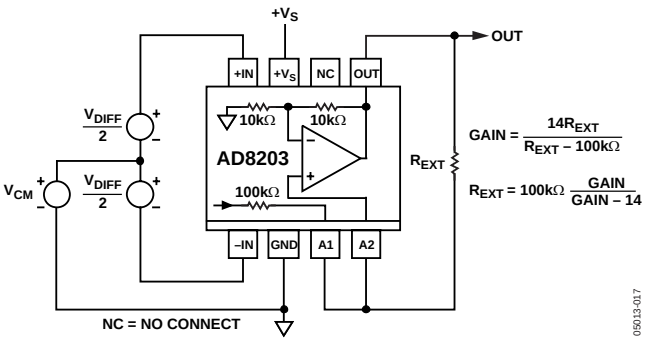


Figure 44. Adjusting for Gains > 14

GAIN TRIM

Figure 45 shows a method for incremental gain trimming by using a trim potentiometer and external resistor R_{EXT}.

The following approximation is useful for small gain ranges:

$$\Delta G \approx (10\ M\Omega/R_{EXT})\%$$

Thus, the adjustment range is ±2% for R_{EXT} = 5 MΩ; ±10% for R_{EXT} = 1 MΩ, and so on.

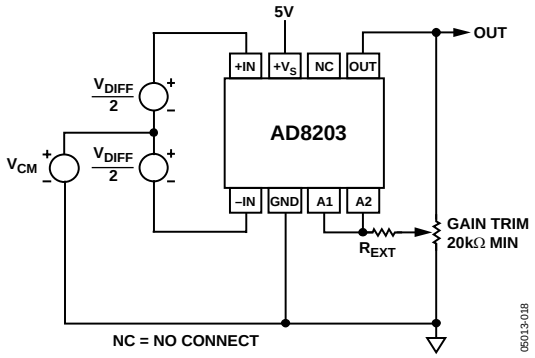


Figure 45. Incremental Gain Trim

Internal Signal Overload Considerations

When configuring gain for values other than 14, the maximum input voltage with respect to the supply voltage and ground must be considered, since either the preamplifier or the output buffer reaches its full-scale output (approximately V_S – 0.2 V) with large differential input voltages. The input of the AD8203 is limited to (V_S – 0.2)/7 for overall gains ≤ 7, since the pre-amplifier, with its fixed gain of ×7, reaches its full-scale output before the output buffer. For gains greater than 7, the swing at the buffer output reaches its full scale first and limits the AD8203 input to (V_S – 0.2)/G, where G is the overall gain.

LOW-PASS FILTERING

In many transducer applications, it is necessary to filter the signal to remove spurious high frequency components, including noise, or to extract the mean value of a fluctuating signal with a peak-to-average ratio (PAR) greater than unity. For example, a full-wave rectified sinusoid has a PAR of 1.57, a raised cosine has a PAR of 2, and a half-wave sinusoid has a PAR of 3.14. Signals having large spikes can have PARs of 10 or more.

When implementing a filter, the PAR should be considered so that the output of the AD8203 preamplifier (A1) does not clip before A2, since this nonlinearity would be averaged and appear as an error at the output. To avoid this error, both amplifiers should be made to clip at the same time. This condition is achieved when the PAR is no greater than the gain of the second amplifier (2 for the default configuration). For example, if a PAR of 5 is expected, the gain of A2 should be increased to 5.

Low-pass filters can be implemented in several ways by using the features provided by the AD8203. In the simplest case, a single-pole filter (20 dB/decade) is formed when the output of A1 is connected to the input of A2 via the internal 100 kΩ resistor by strapping Pin 3, Pin 4, and a capacitor added from this node to ground, as shown in Figure 46. If a resistor is added across the capacitor to lower the gain, the corner frequency increases; it should be calculated using the parallel sum of the resistor and 100 kΩ.

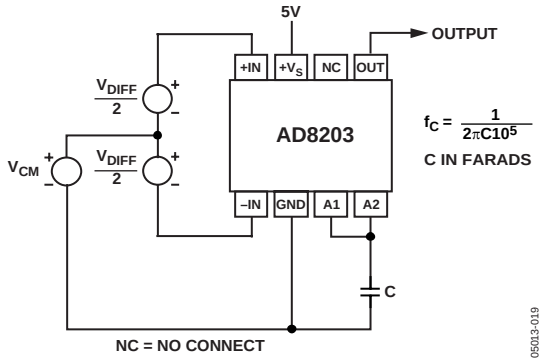


Figure 46. Single-Pole, Low-Pass Filter Using the Internal 100 kΩ Resistor

If the gain is raised using a resistor, as shown in Figure 44, the corner frequency is lowered by the same factor as the gain is raised. Thus, using a resistor of 200 kΩ (for which the gain would be doubled), the corner frequency is now 0.796 Hz μF (0.039 μF for a 20 Hz corner frequency).

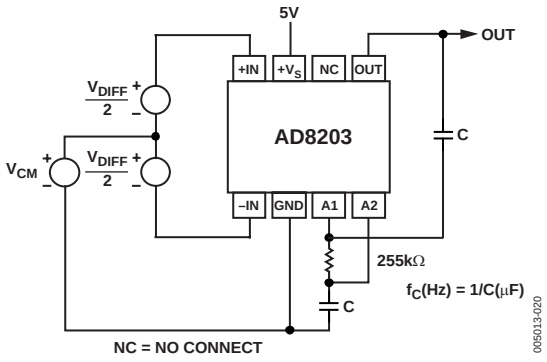


Figure 47. 2-Pole, Low-Pass Filter

A 2-pole filter (with a roll-off of 40 dB/decade) can be implemented using the connections shown in Figure 47. This is a Sallen-Key form based on a ×2 amplifier. It is useful to remember that a 2-pole filter with a corner frequency f_2 and a 1-pole filter with a corner at f_1 have the same attenuation at the frequency (f_2^2/f_1). The attenuation at that frequency is 40 log (f_2/f_1), which is illustrated in Figure 48. Using the standard resistor value shown and equal capacitors (see Figure 47), the corner frequency is conveniently scaled at 1 Hz μF (0.05 μF for a 20 Hz corner). A maximally flat response occurs when the resistor is lowered to 196 kΩ and the scaling is then 1.145 Hz μF. The output offset is raised by approximately 5 mV (equivalent to 250 μV at the input pins).

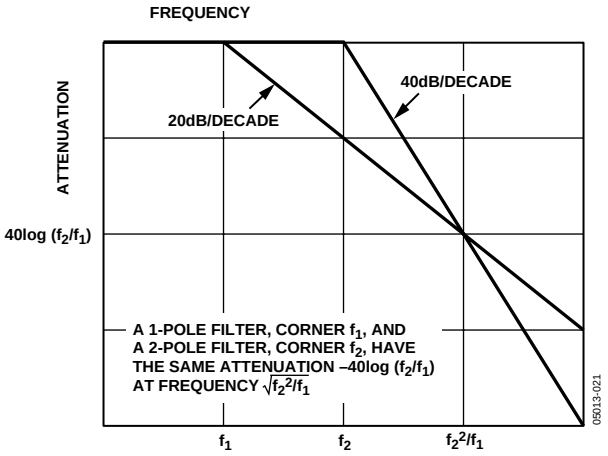


Figure 48. Comparative Responses of 1-Pole and 2-Pole Low-Pass Filters

HIGH LINE CURRENT SENSING WITH LPF AND GAIN ADJUSTMENT

Figure 49 is another refinement of Figure 2, including gain adjustment and low-pass filtering.

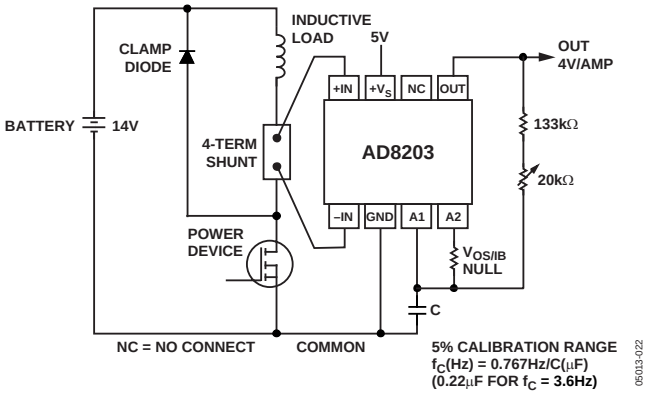


Figure 49. High Line Current Sensor Interface; Gain = ×40, Single-Pole Low-Pass Filter

A power device that is either on or off controls the current in the load. The average current is proportional to the duty cycle of the input pulse and is sensed by a small value resistor. The average differential voltage across the shunt is typically 100 mV, although its peak value is higher by an amount that depends on the inductance of the load and the control frequency. The common-mode voltage, conversely, extends from roughly 1 V above ground for the on condition to about 1.5 V above the battery voltage for the off condition. The conduction of the clamping diode regulates the common-mode potential applied to the device. For example, a battery spike of 20 V may result in an applied common-mode potential of 21.5 V to the input of the devices.

To produce a full-scale output of 4 V, a gain ×40 is used, adjustable by ±5% to absorb the tolerance in the shunt. There is sufficient headroom to allow 10% overrange (to 4.4 V). The roughly triangular voltage across the sense resistor is averaged by a 1-pole low-pass filter, shown in Figure 49, set with a corner frequency of 3.6 Hz, which provides about 30 dB of attenuation at 100 Hz. A higher rate of attenuation can be obtained using a 2-pole filter with f_C = 20 Hz, as shown in Figure 50. Although this circuit uses two separate capacitors, the total capacitance is less than half that needed for the 1-pole filter.

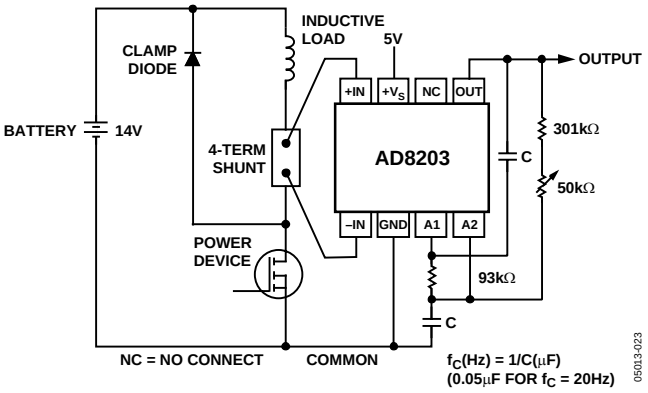


Figure 50. 2-Pole Low-Pass Filter

DRIVING CHARGE REDISTRIBUTION ADCS

When driving CMOS ADCs, such as those embedded in popular microcontrollers, the charge injection (ΔQ) can cause a significant deflection in the output voltage of the AD8203. Though generally of short duration, this deflection may persist until after the sample period of the ADC has expired due to the relatively high open-loop output impedance (21 kΩ) of the AD8203. Including an R-C network in the output can significantly reduce the effect. The capacitor helps to absorb the transient charge, effectively lowering the high frequency output impedance of the AD8203. For these applications, the output signal should be taken from the midpoint of the R_{LAG} to C_{LAG} combination, as shown in Figure 51.

Since the perturbations from the analog-to-digital converter are small, the output impedance of the AD8203 appears to be low. The transient response, therefore, has a time constant governed by the product of the two LAG components, $C_{LAG} \times R_{LAG}$. For the values shown in Figure 51, this time constant is programmed at approximately 10 μs. Therefore, if samples are taken at several tens of microseconds or more, there is negligible charge stack-up.

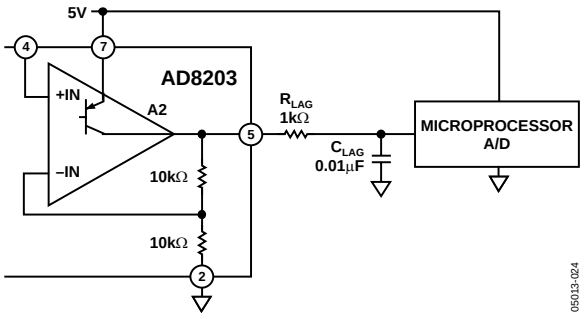


Figure 51. Recommended Circuit for Driving CMOS A/D

OUTLINE DIMENSIONS

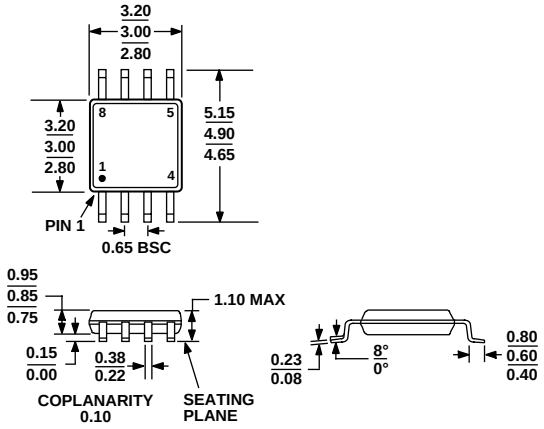


Figure 52. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

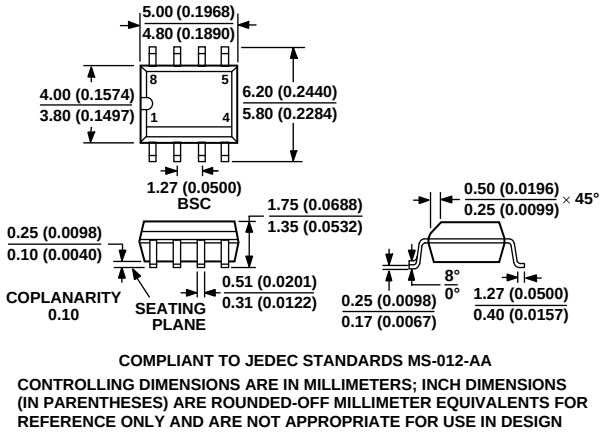


Figure 53. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline	Branding
AD8203YRMZ[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	JXA
AD8203YRMZ-RL[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	JXA
AD8203YRMZ-R7[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	JXA
AD8203YRZ[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8203YRZ-RL[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8203YRZ-R7[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8203YCSURF		Die		

[1] Z = Pb-free part.

NOTES

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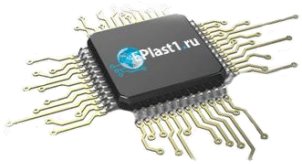
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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.