# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT273

Octal D-type flip-flop with reset; positive-edge trigger

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

# Octal D-type flip-flop with reset; positive-edge trigger

# 74HC/HCT273

## FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See “377” for clock enable version
- See “373” for transparent latch version
- See “374” for 3-state version
- Output capability; standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.
The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output ($Q_n$) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay | $C_L$ = 15 pF; $V_{CC}$ = 5 V | | | |
| | CP to $Q_n$ | | 15 | 15 | ns |
| | $\overline{MR}$ to $Q_n$ | | 15 | 20 | ns |
| $f_{max}$ | maximum clock frequency | | 66 | 36 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per flip-flop | notes 1 and 2 | 20 | 23 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC}$ – 1.5 V

## ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

**PIN DESCRIPTION**

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $\overline{MR}$ | master reset input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | $Q_0$ to $Q_7$ | flip-flop outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | $D_0$ to $D_7$ | data inputs |
| 10 | GND | ground (0 V) |
| 11 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 20 | $V_{CC}$ | positive supply voltage |

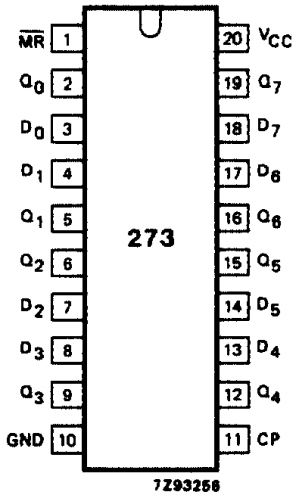



Fig.1 Pin configuration.

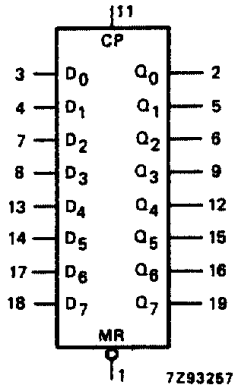



Fig.2 Logic symbol.

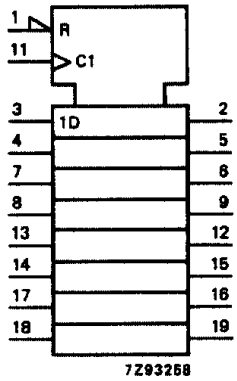



Fig.3 IEC logic symbol.

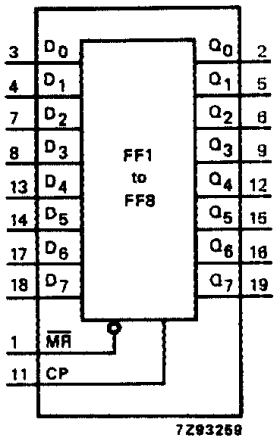



Fig.4 Functional diagram.

**FUNCTION TABLE**

| OPERATING MODES | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_n$ | $Q_n$ |
| reset (clear) | L | X | X | L |
| load “1” | H | ↑ | h | H |
| load “0” | H | ↑ | l | L |

**Note**

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   ↑ = LOW-to-HIGH transition
   X = don’t care

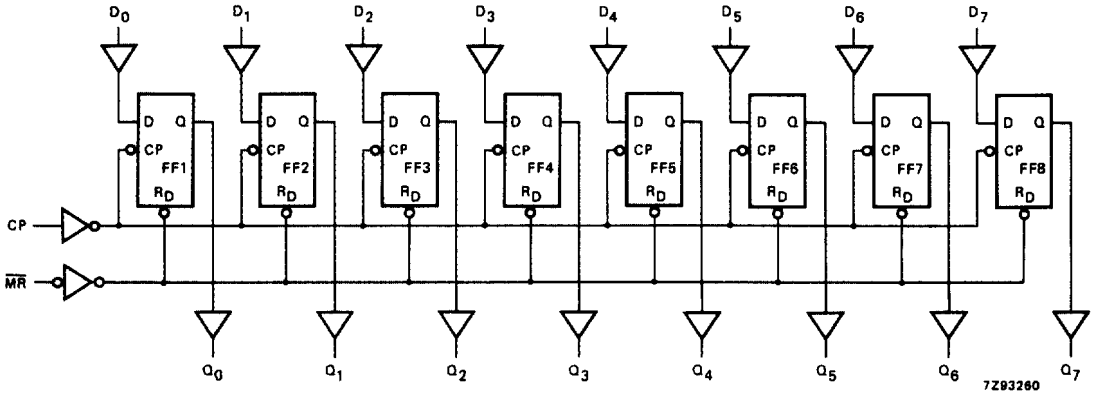



Fig.5 Logic diagram.

### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

### AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay CP to $Q_n$ | | 41<br>15<br>13 | 150<br>30<br>26 | | 185<br>37<br>31 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_n$ | | 44<br>16<br>14 | 150<br>30<br>26 | | 185<br>37<br>31 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 19<br>7<br>6 | 75<br>15<br>13 | | 95<br>19<br>15 | | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_W$ | clock pulse width HIGH or LOW | 80<br>16<br>14 | 14<br>5<br>4 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_W$ | master reset pulse width LOW | 60<br>12<br>10 | 17<br>6<br>5 | | 75<br>15<br>13 | | 90<br>18<br>15 | | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{rem}$ | removal time $\overline{MR}$ to CP | 50<br>10<br>9 | −6<br>−2<br>−2 | | 65<br>13<br>11 | | 75<br>15<br>13 | | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{su}$ | set-up time $D_n$ to CP | 60<br>12<br>10 | 11<br>4<br>3 | | 75<br>15<br>13 | | 90<br>18<br>15 | | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_h$ | hold time $D_n$ to CP | 3<br>3<br>3 | −6<br>−2<br>−2 | | 3<br>3<br>3 | | 3<br>3<br>3 | | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $f_{max}$ | maximum clock pulse frequency | 6.0<br>30<br>35 | 20.6<br>103<br>122 | | 4.8<br>24<br>28 | | 4.0<br>20<br>24 | | MHz | 2.0<br>4.5<br>6.0 | Fig.6 |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

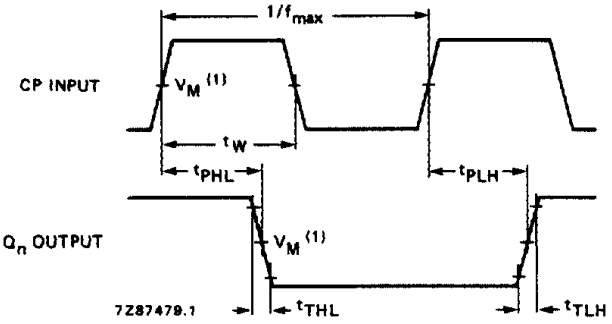
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $\overline{MR}$ | 1.00 |
| CP | 1.75 |
| $D_n$ | 0.15 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

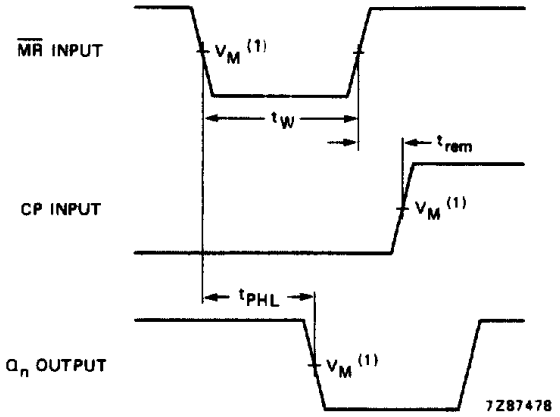
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay CP to $Q_n$ | | 16 | 30 | | 38 | | 45 | ns | 4.5 | Fig.6 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_n$ | | 23 | 34 | | 43 | | 51 | ns | 4.5 | Fig.7 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |
| $t_W$ | clock pulse width HIGH or LOW | 16 | 9 | | 20 | | 24 | | ns | 4.5 | Fig.6 |
| $t_W$ | master reset pulse width LOW | 16 | 8 | | 20 | | 24 | | ns | 4.5 | Fig.7 |
| $t_{rem}$ | removal time $\overline{MR}$ to CP | 10 | −2 | | 13 | | 15 | | ns | 4.5 | Fig.7 |
| $t_{su}$ | set-up time $D_n$ to CP | 12 | 5 | | 15 | | 18 | | ns | 4.5 | Fig.8 |
| $t_h$ | hold time $D_n$ to CP | 3 | −4 | | 3 | | 3 | | ns | 4.5 | Fig.8 |
| $f_{max}$ | maximum clock pulse frequency | 30 | 56 | | 24 | | 20 | | MHz | 4.5 | Fig.6 |

**AC WAVEFORMS**



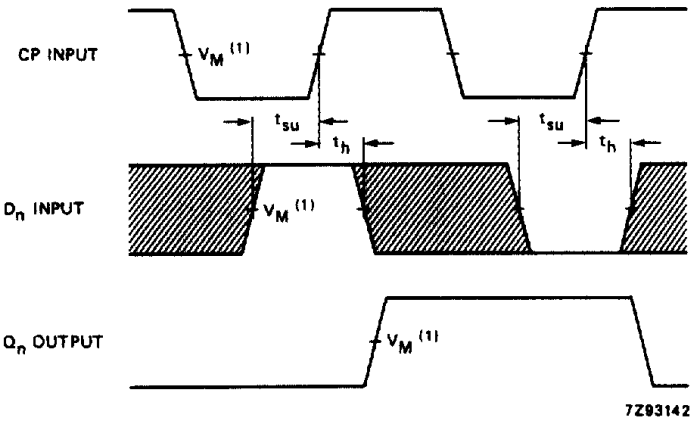

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.6 Waveforms showing the clock (CP) to output ($Q_n$) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output ($Q_n$) propagation delays and the master reset to clock (CP) removal time.




The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.8 Waveforms showing the data set-up and hold times for the data input ($D_n$).

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

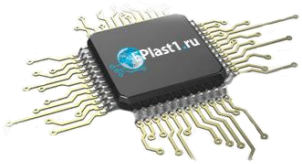
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