# Future Technology Devices International Ltd.

# FT232BL/BQ USB UART IC




The FT232B is a USB to serial UART interface with the following advanced features:

- Single Chip USB to Asynchronous Serial Data Transfer
- Full Handshaking & Modem Interface Signals
- UART I/F Supports 7 / 8 Bit Data, 1 / 2 Stop Bits and Odd/Even/Mark/Space/No Parity
- Data rate 300 => 3M Baud (TTL)
- Data rate 300 => 1M Baud (RS232)
- Data rate 300 => 3M Baud (RS422/RS485)
- 384 Byte Receive Buffer / 128 Byte Transmit Buffer for high data throughput
- Adjustable RX buffer timeout
- Fully Assisted Hardware or X-On / X-Off Handshaking In-built support for event characters and line break condition
- Auto Transmit Buffer control for RS485
- Support for USB Suspend / Resume through SLEEP# and RI# pins
- 4.35V to 5.25V single supply operation
- Support for high power USB Bus powered devices through PWREN# pin
- Integrated level converter on UART and control signals for interfacing to 5V and 3.3V logic
- Integrated 3.3V regulator for USB IO
- Integrated Power-On-Reset circuit
- Integrated 6MHz – 48Mhz clock multiplier PLL
- UHCI / OHCI / EHCI host controller compatible
- USB 1.1 and USB 2.0 compatible
- USB VID, PID, Serial Number and Product Description strings in external EEPROM
- EEPROM programmable on-board via USB
- Available as a compact lead free RoHS compliant 32-LD LQFP package (FT232BL) or 32-LD QFN package (FT232BQ).

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# 1 Typical Applications

- USB to RS232/RS422/RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU/PLD/FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Industrial Control
- USB MP3 Player Interface
- Set Top Box PC - USB interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Smart Card Readers
- USB Instrumentation

## 1.1 Driver Support

**Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...**

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32, 64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS 8/9, OS-X
- Linux 2.4 and greater

**Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)**

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32, 64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

## 1.2 Part Numbers

| Part Number | Package |
|---|---|
| FT232BQ-XXYY | 32 Pin QFN |
| FT232BL- XXYY | 32 Pin LQFP |

**Table 1.1 Part Numbers**

Note: Packing codes for xxxx is:
- Reel: Taped and Reel, (LQFP is 1,000pcs per reel, QFN is 2,500pcs per reel).
- Tray: Tray packing, 250pcs per tray (LQFP only)

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# 2 FT232B Block Diagram

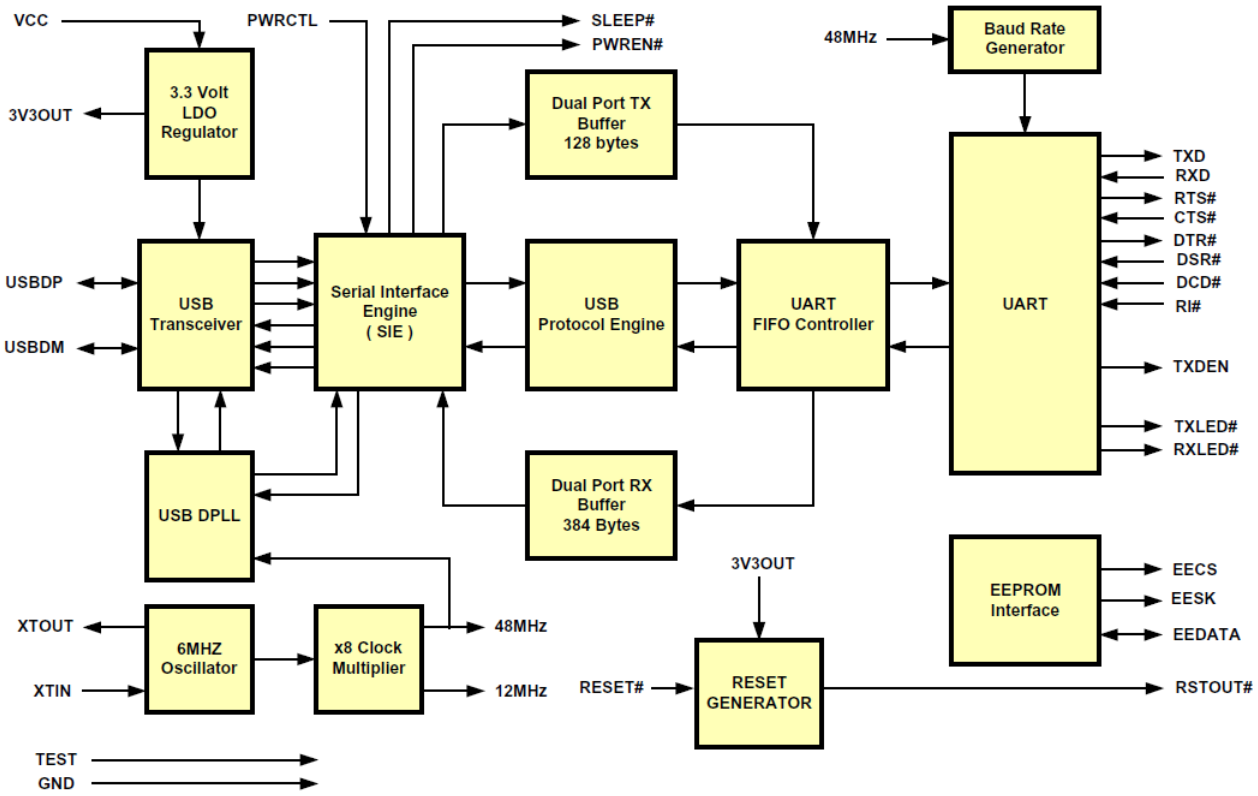



**Figure 2.1 FT232B Block Diagram**

For a description of each function please refer to Section 4.

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# 3 Device Pin Out and Signal Description

## 3.1 32 Pin LQFP Package

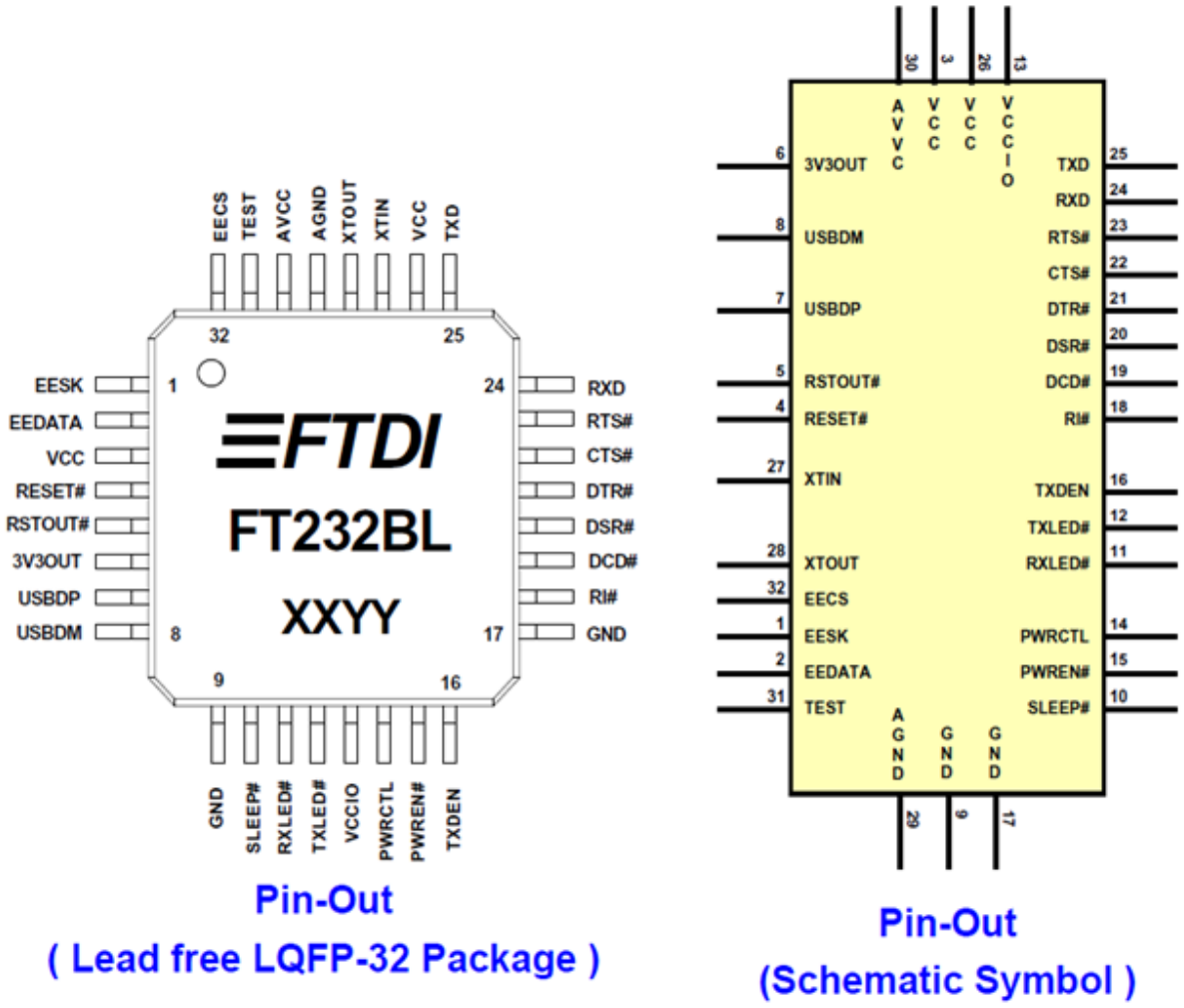



**Figure 3.1 QFN-32 Package Pin Out and schematic symbol**

The part number FT232BM version is also a LQFP-32 package. Please note that this datasheet is not for the FT232BM. Refer to FTDI website for the FT232BM datasheet.

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## 3.2 32 Pin QFN Package

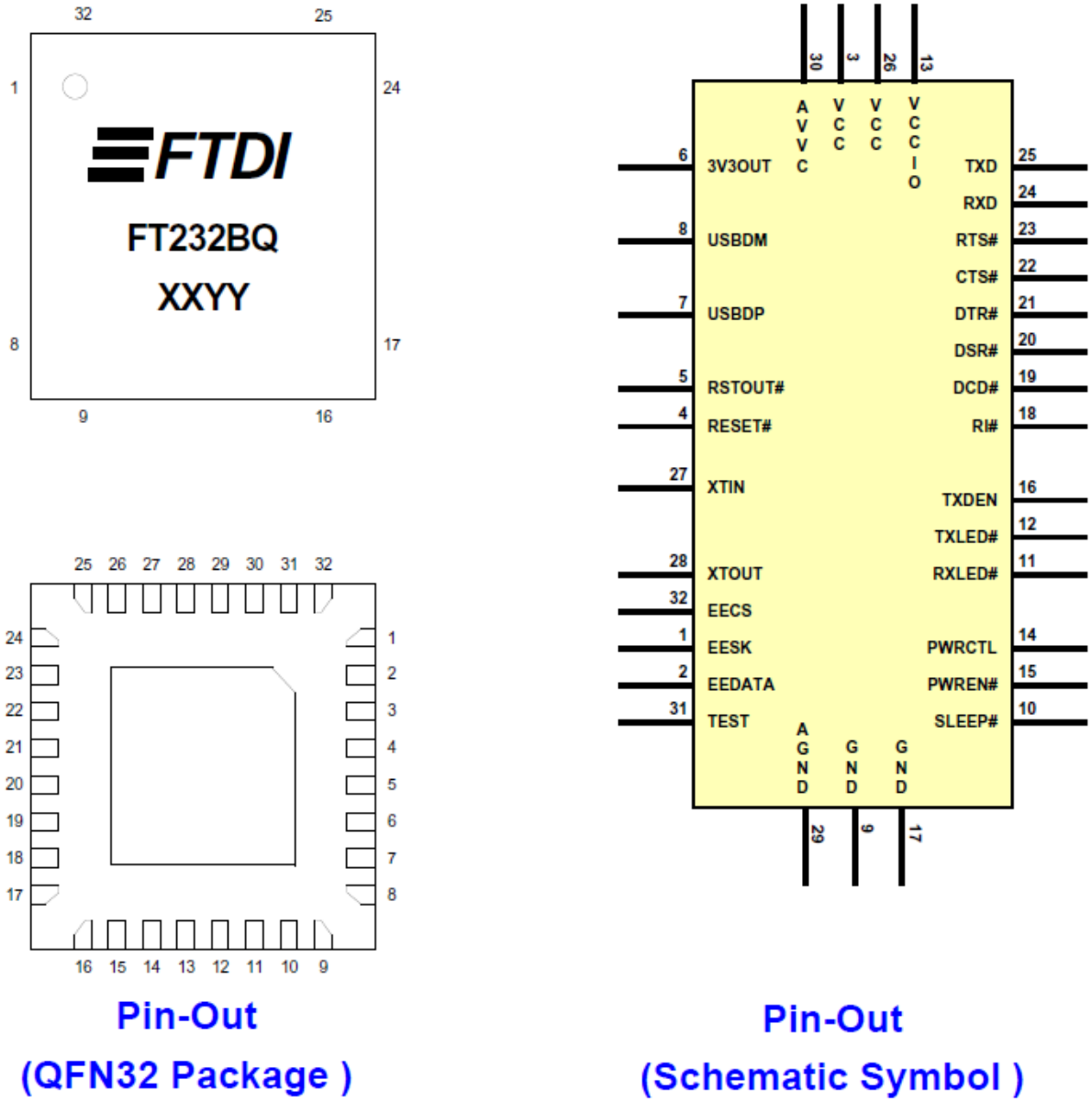



**Figure 3.2 QFN-32 Package Pin Out and schematic symbol**

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## 3.3 LQFP and QFN Package Pin Out Description

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 7 | USBDP | I/O | USB Data Signal Plus ( Requires 1.5k pull-up to 3V3OUT or RSTOUT# ) |
| 8 | USBDM | I/O | USB Data Signal Minus |

**Table 3.1 USB Interface Group**

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 13 | VCCIO | PWR | +3.0 volt to +5.25 volt VCC to the UART interface pins 10...12, 14...16 and 18...25. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level. |
| 9,17 | GND | PWR | Device ground supply pins |
| 6 | 3V3OUT | Output | 3.3 volt Output from the integrated LDO regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. Its prime purpose is to provide the internal 3.3V supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3v logic if required. |
| 3,26 | VCC | PWR | +4.35 volt to +5.25 volt VCC to the device core, LDO and non-UART interface pins |
| 30 | AVCC | PWR | Device analogue power supply for internal x8 clock multiplier |
| 29 | AGND | PWR | Device analogue ground supply for internal x8 clock multiplier |

**Table 3.2 Power and Ground Group**

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 4 | RESET# | Input | Active low reset pin. This can be used by an external device to reset the FT232B. If not required can be left unconnected, or pulled up to VCC. |
| 5 | RSTOUT# | Output | Output of the internal Reset Generator. Stays high impedance for ~ 5ms after VCC > 3.5V and the internal clock starts up, and then clamps its output to the 3.3v output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset |
| 12 | TXLED# | O.C | LED Drive – Pulses Low when Transmitting Data via USB |
| 11 | RXLED# | O.C | LED Drive – Pulses Low when Receiving Data via USB |
| 27 | XTIN | Input | Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note: Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or AC-coupled to centre around VCC/2. |
| 28 | XTOUT | Output | Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic. |
| 31 | TEST | Input | Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail. |

**Table 3.3 Miscellaneous Signal Group**

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| Pin No. | Name | Type | Description |
|---|---|---|---|
| 25 | TXD | Output | Transmit Asynchronous Data Output. |
| 24 | RXD | Input | Receiving Asynchronous Data Input |
| 23 | RTS# | Output | Request to Send Control Output / Handshake Signal. |
| 22 | CTS# | Input | Data Terminal Ready Control Output / Handshake Signal. |
| 21 | DTR# | Output | Clear To Send Control Input / Handshake Signal. |
| 20 | DSR# | Input | Data Set Ready Control Input / Handshake Signal. |
| 19 | DCD# | Input | Data Carrier Detect Control Input. |
| 18 | RI# | Input | Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend. |
| 16 | TXDEN | Output | Enable Transmit Data for RS485. |

**Table 3.4 UART Interface Group**

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 32 | EECS | I/O | EEPROM – Chip Select. For 48MHz operation pull EECS to GND using a 10K resistor. For 6MHz operation no resistor is required. Tri-State during device reset. ****Note 1** |
| 1 | EESK | Output | Clock signal to EEPROM. Tri-State during device reset, else drives out. Adding a 10K pull down resistor onto EESK will cause the FT232B to use USB Product ID 6004 (hex) instead of 6001 (hex). All of the other USB device descriptors are unchanged.****Note 1** |
| 2 | EEDATA | I/O | EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. ****Note 1** |

**Table 3.5 EEPROM Interface Group**

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 10 | SLEEP# | Output | Goes Low during USB Suspend Mode. Typically used to power-down an external TTL to RS232 level converter IC in USB ⇔ RS232 converter designs |
| 15 | PWREN# | Output | Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way. |
| 14 | PWRCTL | Input | Bus Powered – Tie Low / Self Powered – Tie High (to VCCIO) |

**Table 3.6 Power Control Group**

****Note 1 –** During device reset, these pins are tri-state but pulled up to VCC via internal 200K resistors.

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# 4 Function Description

The FT232B is a lead free version of the 2nd generation of FTDI's USB to serial UART interface device which simplifies USB to serial designs. This device not only adds extra functionality to its FT8U232AM predecessor and reduces external component count, but also maintains a high degree of pin compatibility with the original, making it easy to upgrade or cost reduce existing designs as well as increasing the potential for using the device in new application areas. This section summarises the enhancements of the 2nd generation device compared to its FT8U232AM predecessor.

## 4.1 Key Features and Enhancements from FT8U232AM

**Integrated Power-On-Reset (POR) Circuit.** The device now incorporates an internal POR function. The existing RESET# pin is maintained in order to allow external logic to reset the device where required, however for many applications this pin can now simply be hard wired to VCC. In addition, a new reset output pin (RSTOUT#) is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices. RSTOUT# was the TEST pin on the previous generation of devices.

**Integrated RCCLK Circuit.** In the previous devices, an external RC circuit was required to ensure that the oscillator and clock multiplier PLL frequency was stable prior to enabling the clock internal to the device. This circuit is now embedded on-chip – the pin assigned to this function is now designated as the TEST pin and should be tied to GND for normal operation

**Integrated Level Converter on UART interface and control signals.** The previous FTDI devices drive the UART and control signals at 5V CMOS logic levels. The FT232B has a separate VCCIO pin allowing the device to directly interface to 3.3V and other logic families without the need for external level converter Ics

**Improved Power Management control for USB Bus Powered, high current devices.** The previous devices had a USBEN pin, which became active when the device was enumerated by USB. To provide power control, this signal had to be externally gated with SLEEP# and RESET#.

This gating is now done on-chip – USBEN has now been replaced with the new PWREN# signal which can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. A new EEPROM based option makes the device pull gently down its UART interface lines when the power is shut off (PWREN# is High). In this mode, any residual voltage on external circuitry is bled to GND when power is removed thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored

**Lower Suspend Current.** Integration of RCCLK within the device and internal design improvements reduce the suspend current of the FT232B to under 200uA (excluding the 1.5k pull-up on USBDP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.

**Programmable Receive Buffer Timeout.** In the previous device, the receive buffer timeout flushed remaining data from the receive buffer at a fixed 16ms timeout. This timeout is now programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better 10ptimized for protocols requiring faster response times from short data packets.

**TXDEN Timing fix.** TXDEN timing has now been fixed to remove the external delay that was previously required for RS485 applications at high baud rates. TXDEN now works correctly during a transmit send-break condition.

**Relaxed VCC Decoupling.** The FT232B devices now incorporate a level of on-chip VCC decoupling. Though this does not eliminate the need for external decoupling capacitors, it significantly improves the ease of PCB design requirements to meet FCC, CE and other EMI related specifications.

**Improved PreScaler Granularity.** The previous version of the Prescaler supported division by (n + 0), (n+0.125), (n + 0.25) and (n + 0.5) where n is an integer between 2 and 16,384 (214). To this FTDI have added (n + 0.375), (n + 0.625), (n + 0.75) and (n+ 0.875) which can be used to improve the accuracy of some baud rates and generate new baud rates which were previously impossible (especially with higher baud rates).

**Bit Bang Mode.** The 2nd generation device has a new option referred to as "Bit Bang" mode. In Bit Bang mode, the eight UART interface control lines can be switched between UART interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by the prescaler setting. As well as allowing the device to be used stand-alone as a general purpose IO controller for example controlling lights, relays and switches, some other interesting

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possibilities exist. For instance, it may be possible to connect the device to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use Bit Bang Mode to download configuration data to the FPGA which would define its hardware function, then after the FPGA device is configured the FT232B can switch back into UART interface mode to allow the programmed FPGA device to communicate with the PC over USB. This approach allows a customer to create a "generic" USB peripheral whose hardware function can be defined under control of the application software. The FPGA based hardware can be easily upgraded or totally changed simply by changing the FPGA configuration data file. Application notes, software and development modules for this application area will be available from FTDI and other 3rd parties.

**PreScaler Divide By 1 Fix.** The previous device had a problem when the integer part of the divisor was set to 1. In the 2nd generation device setting the prescaler value to 1 gives a baud rate of 2 million baud and setting it to zero gives a baud rate of 3 million baud. Non-integer division is not supported with divisor values of 0 and 1.

**Less External Support Components.** As well as eliminating the RCCLK RC network, and for most applications the need for an external reset circuit, we have also eliminated the requirement for a 100K pull-up on EECS to select 6MHz operation. When the FT232B is being used without the configuration EEPROM, EECS, EESK and EEDATA can now be left n/c. For circuits requiring a long reset time (where the device is reset externally using a reset generator I.C., or reset is controlled by the IO port of a MCU, FPGA or ASIC device) an external transistor circuit is no longer required as the 1.5k pull-up resistor on USBDP can be wired to the RSTOUT# pin instead of to 3.3V. Note : RSTOUT# drives out at 3.3V level, not at 5V VCC level. This is the preferred configuration for new designs.

**Extended EEPROM Support.** The previous generation of devices only supported EEPROM of type 93C46 (64 x 16 bit). The new devices will also work with EEPROM type 93C56 (128 x 16 bit) and 93C66 (256 x 16 bit). The extra space is not used by the device, however it is available for use by other external MCU / logic whilst the FT232B is being held in reset.

**USB 2.0 (full speed option).** A new EEPROM based option allows the FT232B to return a USB 2.0 device descriptor as opposed to USB 1.1. Note : The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

**Multiple Device Support without EEPROM.** When no EEPROM (or a blank or invalid EEPROM) is attached to the device, the FT232B no longer gives a serial number as part of its USB descriptor. This allows multiple devices to be simultaneously connected to the same PC. However, we still highly recommend that EEPROM is used, as without serial numbers a device can only be identified by which hub port in the USB tree it is connected to which can change if the end user re-plugs the device into a different port

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## 4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT232B. Please refer to the block diagram shown in **Figure 2.1** .

**The 3.3V LDO Regulator** generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of not greater than 5mA could also draw its power from the 3V3OUT pin if required.

**USB Transceiver.** The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

**USB DPLL.** The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

**6MHz Oscillator.** The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz crystal or ceramic resonator

**X8 Clock Multiplier.** The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 12MHz reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks. It also generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

**Serial Interface Engine (SIE).** The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

**USB Protocol Engine.** The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

**Dual Port TX Buffer (128 bytes).** Data from the USB data out endpoint is stored in the Dual Port TX buffer and removed from the buffer to the UART transmit register under control of the UART FIFO controller.

**Dual Port RX Buffer (384 bytes).** Data from the UART receive register is stored in the Dual Port RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

**UART FIFO Controller.** The UART FIFO controller handles the transfer of data between the Dual FIFO RX and TX buffers and the UART transmit and receive registers.

**UART.** The UART performs asynchronous 7/8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by the UART include RTS, CTS, DTR, DSR, DCD and RI. The UART provides a transmitter enable control signal (TXDEN) to assist with interfacing to RS485 transceivers. The UART supports RTS/CTS, DTR/DSR and X-On/X-Off handshaking options. Handshaking, where required, is handled in hardware to ensure fast response times. The UART also supports the RS232 BREAK setting and detection conditions.

**Baud Rate Generator.** The Baud Rate Generator provides a x16 clock input to the UART from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a whole number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 3M baud.

**RESET Generator**. The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. RESET# input and RSTOUT# output are provided to allow other devices to reset the FT232B to reset other devices respectively. During reset, RSTOUT# is driven low, otherwise it drives out at the 3.3V provided by the onboard regulator. RSTOUT# can be used to control the 1.5k pull-up on USBDP directly where delayed USB enumeration is required. It can also be used to reset other devices. RSTOUT# will stay high-impedance for approximately 5ms after VCC has risen above 3.5V AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator IC.

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**EEPROM interface**. Though the FT232B will work without the optional EEPROM, an external 93C46 (93C56 or 93C66) EEPROM can be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT232B for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and USB 2.0 descriptor modes. The EEPROM should be a 16 bit wide configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.35V to 5.25V. The EEPROM is programmable-on board over USB using a utility available from FTDI's web site (http://www.ftdichip.com). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. If no EEPROM is connected (or the EEPROM is blank), the FT232B will use its built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

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# 5 Devices Characteristics and Ratings

## 5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT232B devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

| Parameter | Value | Unit |
|---|---|---|
| Storage Temperature | -65 to +150 | °C |
| Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity) | 192 (MSL 3 Compliant) ****Note 2** | Hours |
| Ambient Temperature (Power Applied) | 0 to +70 | °C |
| M.T.B.F. (at 35°C) | 247484<br>≈ 28 | Hours<br>Years |
| VCC Supply Voltage | -0.5 to +6.00 | V |
| DC Input Voltage – USBDP and USBDM | -0.5 to +3.8 | V |
| DC Input Voltage – High Impedance Bidirectional | -0.5 to + (VCC +0.5) | V |
| DC Input Voltage – All Other Inputs | -0.5 to + (VCC +0.5) | V |
| DC Output Current – Outputs | 24 | mA |
| DC Output Current – Low Impedance Bidirectional | 24 | mA |
| Power Dissipation (VCC = 5.25V) | 500 | mW |
| Electrostatic Discharge Voltage (Human Body Model) (I<1uA) | ±3000 | V |
| Latch Up Current (Vi = +/- 10V maximum, for 10ms) | ±200 | mA |

**Table 5.1 Absolute Maximum Ratings**

****Note 2 –** If devices are stored out of the packaging beyond this time limit the devices should be baked before use. Refer to JEDEC 033b for baking details.

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## 5.2 DC Characteristics

DC Characteristics (Ambient Temperature = 0°C to 70°C)

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| VCC1 | VCC Operating Supply Voltage | 4.35 | 5 | 5.25 | V | |
| VCC2 | VCCIO Operating Supply Voltage | 3.0 | --- | 5.25 | V | |
| Icc1 | Operating Supply Current | --- | 25 | --- | mA | Normal Operation |
| Icc2 | Operating Supply Current | --- | 180 | 200 | µA | USB Suspend **Note 3 |

**Table 5.2 Operating Voltage and Current**

****Note 3** – Supply current excludes the 200uA nominal drawn by the external pull-up resistor on USBDP.

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 3.2 | 4.1 | 4.9 | V | I source = 2mA |
| Vol | Output Voltage Low | 0.3 | 0.4 | 0.6 | V | I sink = 2mA |
| Vin | Input Switching Threshold | 1.0 | 1.2 | 1.5 | V | **Note 4 |
| Vhys | Input Switching Hysteresis | 50 | 55 | 60 | mV | |

**Table 5.3 UART IO Pin Characteristics (VCCIO = +5.0V)**

****Note 4** – Inputs have an internal 200K pull-up resistor to VCCIO.

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 2.2 | 2.7 | 3.2 | V | I source = 1mA |
| Vol | Output Voltage Low | 0.3 | 0.4 | 0.5 | V | I sink = 2mA |
| Vin | Input Switching Threshold | 1.0 | 1.2 | 1.5 | V | **Note 4 |
| Vhys | Input Switching Hysteresis | 20 | 25 | 30 | mV | |

**Table 5.4 UART IO Pin Characteristics (VCCIO = +3.0 to +3.6V)**

****Note 4** – Inputs or IO pin in input mode have an internal 200K pull-up resistor to VCCIO.

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| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 4.0 | - | 5.0 | V | Fosch = 6MHZ |
| Vol | Output Voltage Low | 0.1 | - | 1.0 | V | Fosch = 6MHZ |
| Vin | Input Switching Threshold | 1.8 | 2.5 | 3.2 | V | |

**Table 5.5 XTIN / XTOUT Pin Characteristics**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 3.2 | 4.1 | 4.9 | V | I source = 2mA |
| Vol | Output Voltage Low | 0.3 | 0.4 | 0.6 | V | I sink = 2mA |
| Vin | Input Switching Threshold | 1.3 | 1.6 | 1.9 | V | |
| Vhys | Input Switching Hysteresis | 50 | 55 | 60 | mV | ****Note 5** |

**Table 5.6 RESET#, TEST, EECS, EESK, EEDATA Pin Characteristics**

****Note 5** – EECS, EESK and EEDATA pins have an internal 200K pull-up resistor to VCC

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Voh | Output Voltage High | 3.0 | - | 3.6 | V | I source = 2mA |
| Vol | Output Voltage Low | 0.3 | - | 0.6 | V | I sink = 2mA |

**Table 5.7 RSTOUT Pin Characteristics (VCCIO = +1.8V, Standard Drive Level)**

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|---|---|---|---|---|---|---|
| Uvoh | IO Pins Static Output ( High) | 2.8 | - | 3.6 | V | RI = 1.5K to 3V3Out ( D+)<br>I = 15K to GND ( D-) |
| Uvol | IO Pins Static Output ( Low) | 0 | - | 0.3 | V | RI = 1.5K to 3V3Out ( D+)<br>I = 15K to GND ( D-) |
| Uvse | Single Ended Rx Threshold | 0.8 | - | 2.0 | V | |
| Ucom | Differential Common Mode | 0.8 | - | 2.5 | V | |
| UVDif | Differential Input Sensitivity | 0.2 | - | | V | |
| UdrvZ | Driver Output Impedance | 29 | - | 44 | Ohms | ****Note 6** |

**Table 5.8 USB I/O Pin Characteristics**

****Note 6** – Driver Output Impedance includes the external 27R series resistors on USBDP and USBDM pins.

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# 6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT232B.

## 6.1 USB Bus Powered Configuration

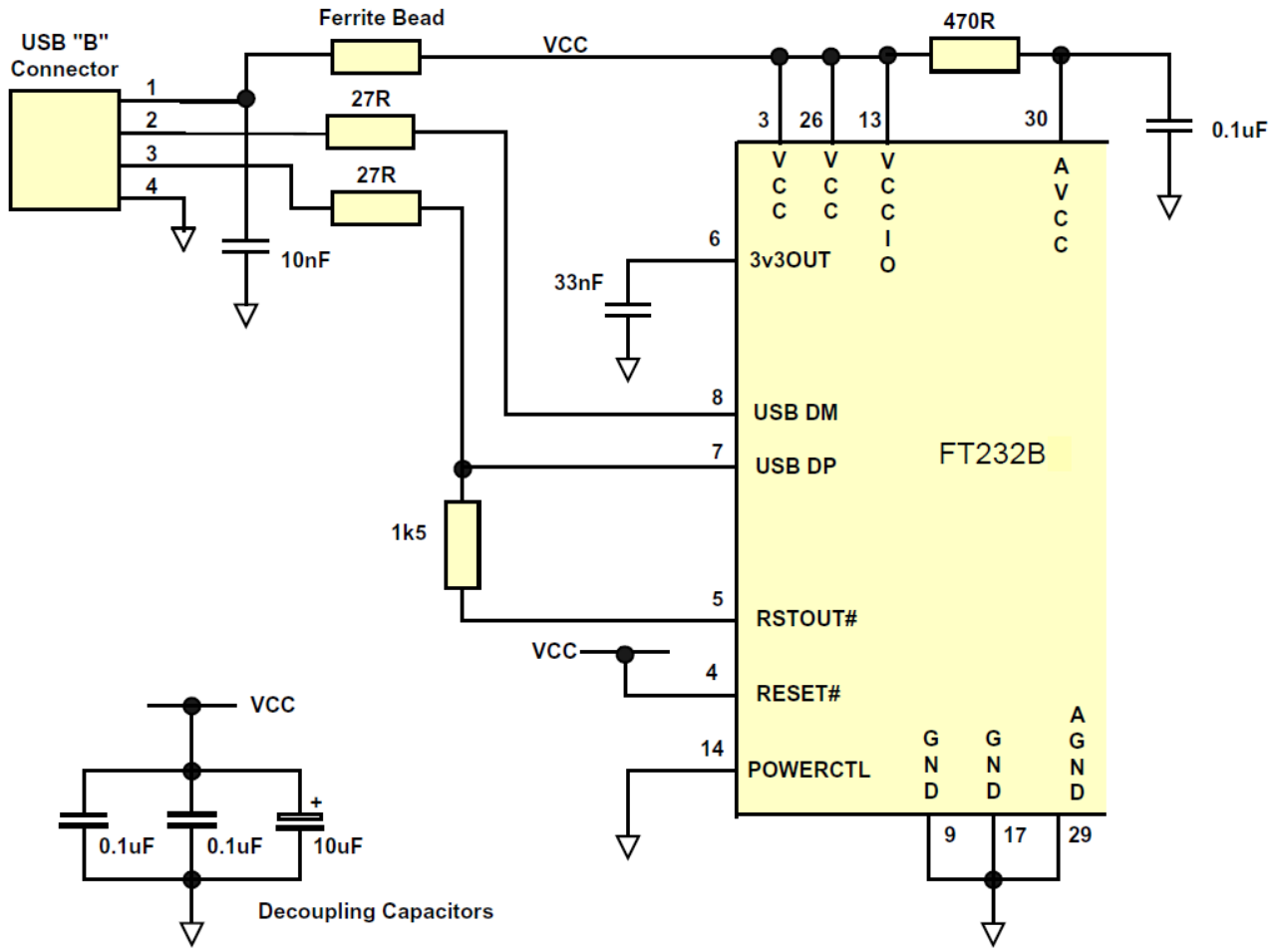



**Figure 6.1 Bus Powered Configuration**

Figure 6.1 illustrates a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows:

a) On plug-in, the device must draw no more than 100mA
b) On USB Suspend the device must draw no more than 500uA (2.5mA for devices configured to support remote wake-up).
c) A Bus Powered High Power Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500uA(2.5mA) on USB suspend.
d) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub
e) No device can draw more that 500mA from the USB Bus.

The power descriptor in the EEPROM should be programmed to match the current draw of the device.

PWRCTL (pin 14) is pulled low to configure the device with a USB Bus Power descriptor. A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit – a suitable range of Ferrite Beads is available from Steward (www.steward.com) for example Steward Part # MI0805K400R-00, also available as DigiKey Part # 240-1035-1.

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## 6.2 Self Powered Configuration

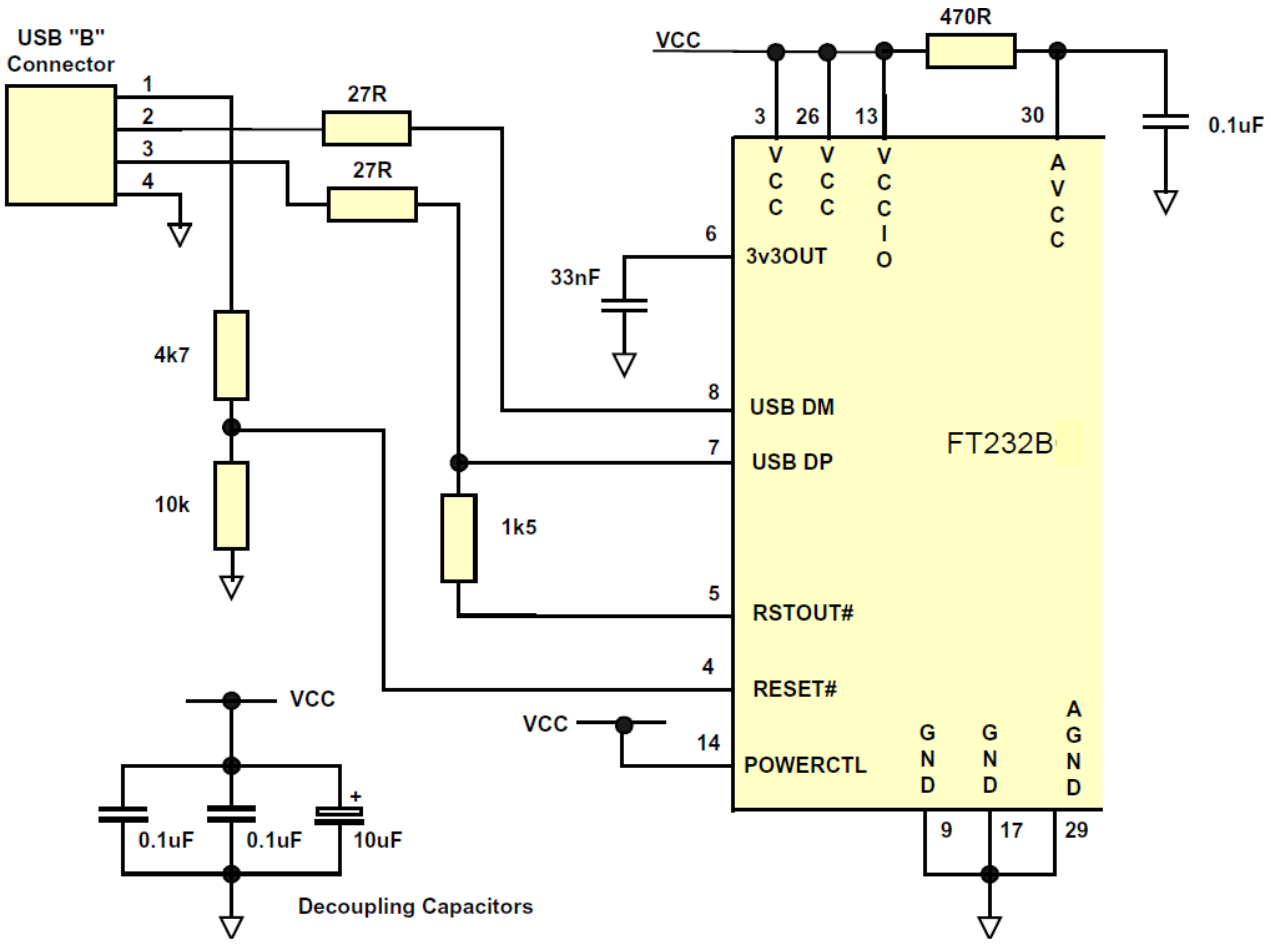



**Figure 6.2 Self Powered Configuration**

Figure 6.2 illustrates a typical USB self powered configuration. A USB Self Powered device gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows:

a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
b) A Self Powered Device can take as much current as it requires during normal operation and USB suspend as it has its own POWER SUPPLY.
c) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs

PWRCTL (pin 14) is pulled high to configure the device with a USB Bus Power descriptor. The power descriptor in the EEPROM should be programmed to a value of zero. The USB power descriptor option in the EEPROM should be programmed to a value of zero (self powered).

To meet requirement, the 1.5 K pull-up resistors on USBDP is connected to RSTOUT# as per the bus-power circuit. However, the USB Bus Power is used to control the RESET# Pin of the FT232B device. When the USB Host or Hub is powered up RSTOUT# will pull the 1.5K resistor on USBDP to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, RSTOUT# will also be low, so no current will be forced down USBDP via the 1.5K pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note: When the FT232B is in reset, the UART interface pins all go tri-state. These pins have internal 200K pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

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## 6.3 Interfacing to 3.3V Logic

### 6.3.1 Bus Powered Circuit with 3.3V logic drive / supply voltage

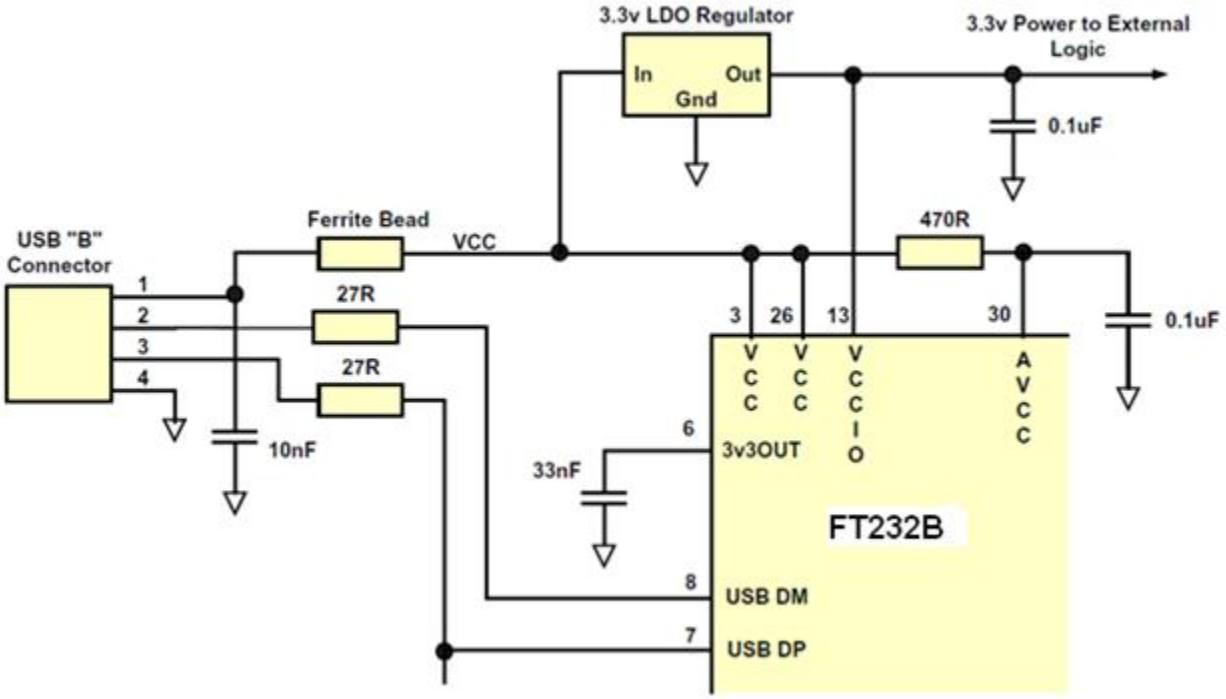



**Figure 6.3 Bus Powered Circuit with 3.3V logic drive / supply voltage**

Figure 6.3 shows how to configure the FT232B to interface with a 3.3V logic device. In this example, a discrete 3.3V regulator is used to supply the 3.3V logic from the USB supply. VCCIO is connected to the output of the 3.3V regulator, which in turn will cause the UART interface IO pins to drive out at 3.3V level. For USB bus powered circuits some considerations have to be taken into account when selecting the regulator:

a) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35 volts. A Low Drop Out (LDO) regulator must be selected.
b) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500uA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip MCP1700 Series. These devices can supply up to 250mA current and have a quiescent current of under 1uA.

In some cases, where only a small amount of current is required (< 5mA) , it may be possible to use the in-built regulator of the FT232B to supply the 3.3v without any other components being required. In this case, connect VCCIO to the 3v3OUT pin of the FT232B.

Note: It should be emphasized that the 3.3V supply for VCCIO in a bus powered design with a 3.3V logic interface should come from an LDO which is supplied by the USB bus, or from the 3V3OUT pin of the FT232B, and not from any other source.

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### 6.3.2 Self Powered Circuit with 3.3V logic drive / supply

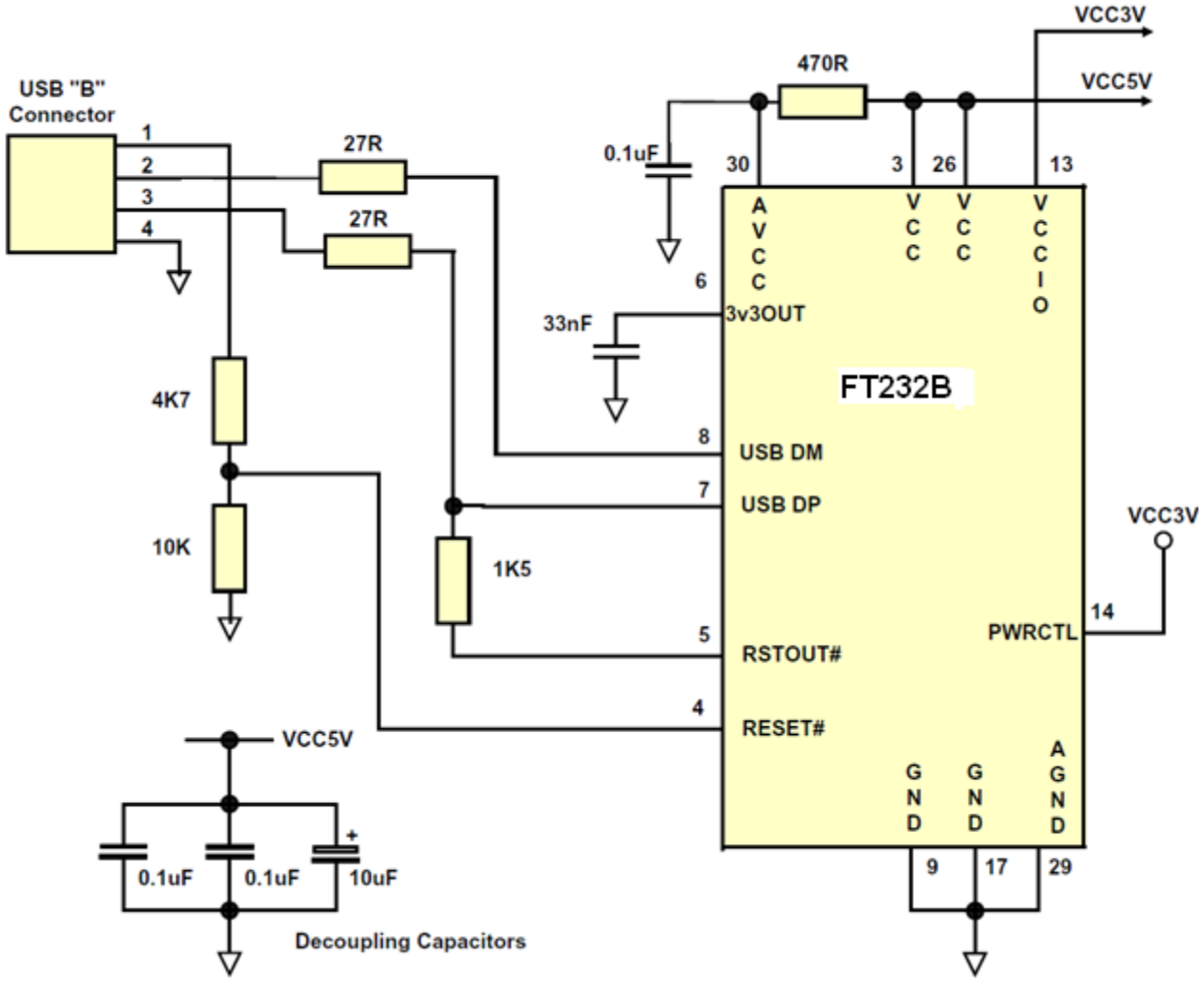



**Figure 6.4 Self Powered Circuit with 3.3V logic drive / supply**

Figure 6.4 is an example of a USB self powered design with 3.3V interface. In this case VCCIO is supplied by an external 3.3V supply in order to make the device IO pins drive out at 3.3V logic level, thus allowing it to be connected to a 3.3V MCU or other external logic. A USB self powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get its power from the USB port.

As with bus powered 3.3V interface designs, in some cases, where only a small amount of current is required (<5mA), it may be possible to use the in-built regulator of the FT232B to supply the 3.3V without any other components being required. In this case, connect VCCIO to the 3v3OUT pin of the FT232B.

Note that in this case PWRCTL is pulled up to VCCIO, not VCC.

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## 6.4 Bus Powered Circuit (<=100mA) with Power Control

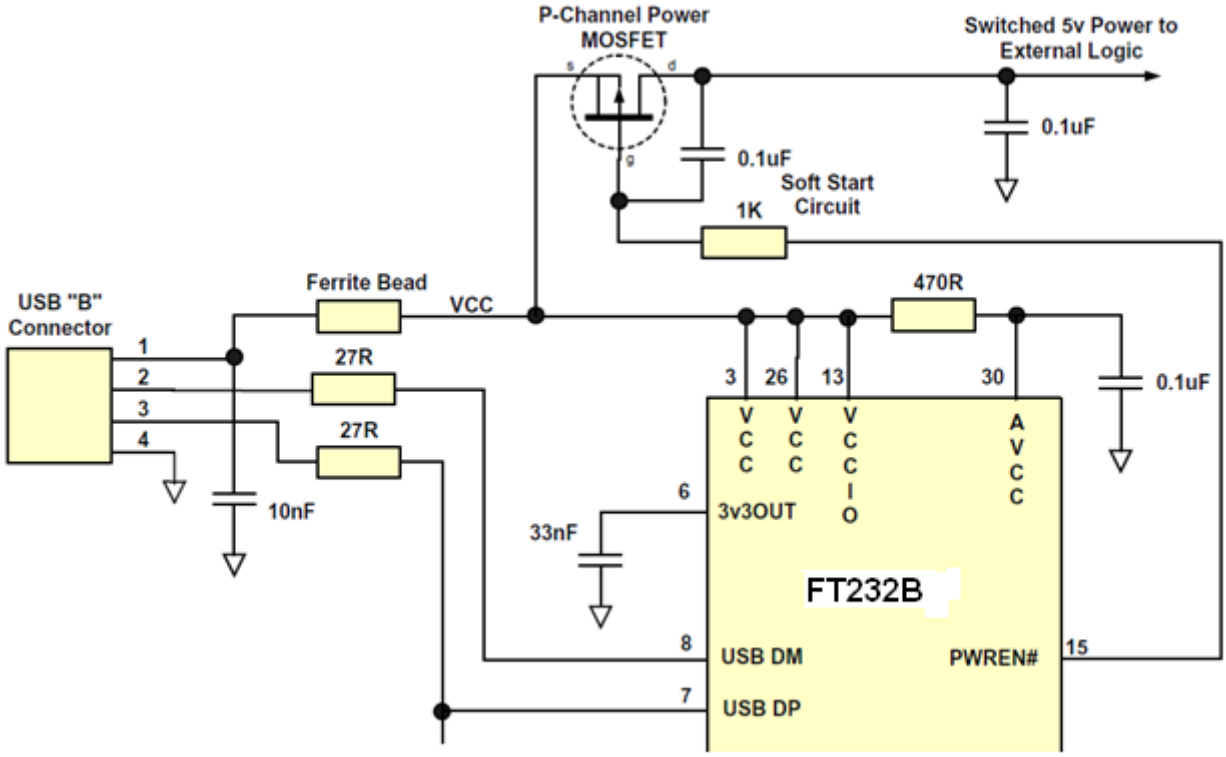



**Figure 6.5 Bus Powered with Power Switching Configuration**

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500uA total suspend current requirement (including external logic). This limit is 2.5mA for devices that support remote wake-up. Some external logic can power itself down into a low current state by monitoring the PWREN# pin. For external logic that cannot power itself down in that way, the FT232B provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 8.3 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device could be a Fairchild NDT456P, or International Rectifier IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1K series resistor and a 0.1 uF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT232B, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5 V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switch i.c. with inbuilt "soft-start" can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs –

a) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.
b) Set the Pull-down on Suspend option in the FT232B's EEPROM.
c) For USB high-power bus powered device (one that consumes greater than 100 mA, and up to 500 mA of current from the USB bus), the power consumption of the device should be set in the max power field in the EEPROM. A high-power bus powered device must use this descriptor in the EEPROM to inform the system of its power requirements.
d) For 3.3V power controlled circuits VCCIO must not be powered down with the external circuitry (PWREN# gets its VCC supply from VCCIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic OR if appropriate power VCCIO from the 3V3OUT pin of the FT232B.

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# 7 Device Configuration Examples

The following sections illustrate device configurations for the FT245BM.

## 7.1 Oscillator Configurations

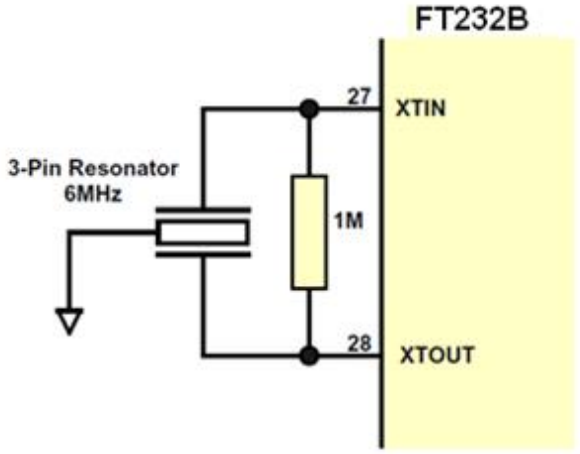



**Figure 7.1 3 Pin Ceramic Resonator Configuration**

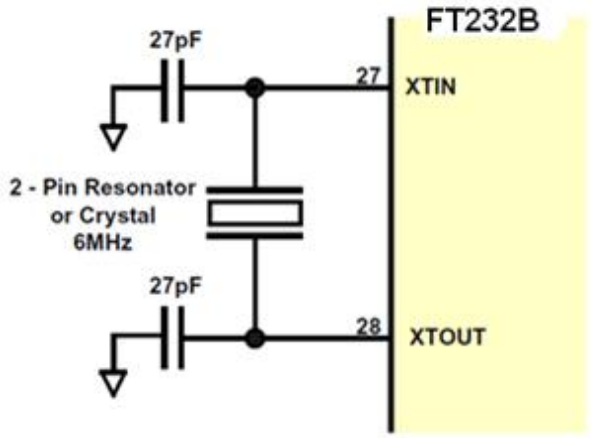



**Figure 7.2 Crystal or 2 Pin Ceramic Resonator Configuration**

Figure 7.1 illustrates how to use the FT232B with a 3-Pin Ceramic Resonator. A suitable part would be a ceramic resonator from Murata's CERALOCK range or equivalent. 3-Pin ceramic resonators have the load capacitors built into the resonator so no external loading capacitors are required. This makes for an economical configuration. The accuracy of this Murata ceramic resonator is +/- 0.1% and it is specifically designed for USB full speed applications. A 1 MegaOhm loading resistor across XTIN and XTOUT is recommended in order to guarantee this level of accuracy.

Figure 7.2 illustrates how to use the FT232B with a 6MHz Crystal or 2-Pin Ceramic Resonator. These devices do not have in-built loading capacitors. They must be added between XTIN, XTOUT and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals and some resonators but do select the value based on the manufacturer's recommendations wherever possible. If using a crystal, use a parallel cut type. If using a resonator, see the previous note on frequency accuracy.

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## 7.2 EEPROM Configuration

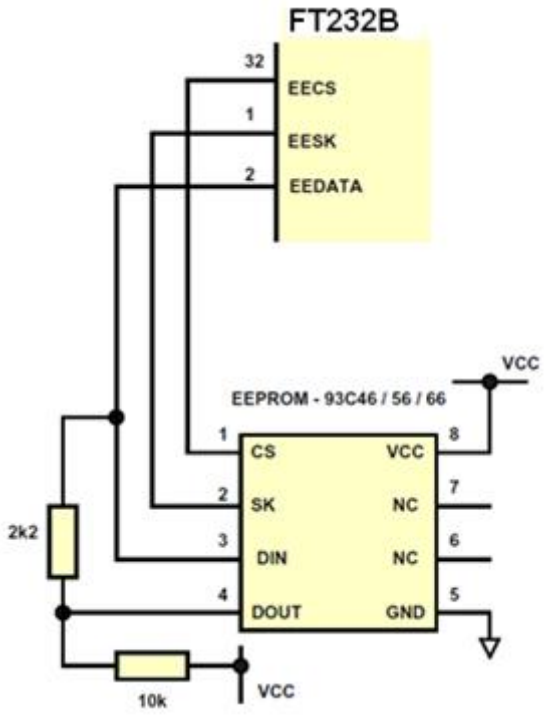



**Figure 7.3 EEPROM Configuration**

Figure 7.3 illustrates how to connect the FT232B to the 93C46 (93C56 or 93C66) EEPROM. EECS (pin 32) is directly connected to the chip select (CS) pin of the EEPROM. EESK (pin 1) is directly connected to the clock (SK) pin of the EEPROM. EEDATA (pin 2) is directly connected to the Data In (Din) pin of the EEPROM. There is a potential condition whereby both the Data Output (Dout) of the EEPROM can drive out at the same time as the EEDATA pin of the FT232B. To prevent potential data clash in this situation, the Dout of the EEPROM is connected to EEDATA of the FT232B via a 2.2K resistor.

Following a power-on reset or a USB reset, the FT232B will scan the EEPROM to find out (a) if an EEPROM is attached to the Device and (b) if the data in the device is valid. If both conditions are true, then the FT232B will use the data in the EEPROM, otherwise it will use its built-in default values. When a valid command is issued to the EEPROM from the FT232B, the EEPROM will acknowledge the command by pulling its Dout pin low. In order to check for this condition, it is necessary to pull Dout high using a 10K resistor. If the command acknowledge doesn't happen then EEDATA will be pulled high by the 10K resistor during this part of the cycle and the device will detect an invalid command or no EEPROM present.

There are two varieties of these EEPROM's from many sources such as Microchip, STMicro, ISSI etc. – one is configured as being 16 bits wide, the other is configured as being 8 bits wide. The FT232B requires EEPROMs with a 16-bit wide configuration such as the Microchip 93LC46B device. The EEPROM must be capable of reading data at a 1Mb clock rate at a supply voltage of 4.35V to 5.25V. Most available parts are capable of this.

Check the manufacturers' data sheet to find out how to connect pins 6 and 7 of the EEPROM. Some devices specify these as no-connect, others use them for selecting 8 / 16 bit mode or for test functions. Some other parts have their pin out rotated by 90° *. It is recommended to* select the required part and its options carefully.

It is possible to "share" the EEPROM between the FT232B and another external device such as an MCU. However, this can only be done when the FT232B is held in the reset condition as it tri-states its EEPROM interface at that time. A typical configuration would use four bit's of an MCU IO Port. One bit would be used to hold the FT232B reset (using RESET#) on power-up, the other three would connect to the EECS, EESK and EEDATA pins of the FT232B in order to read / write data to the EEPROM at this time. Once the MCU has read / written the EEPROM, it would take RESET# high to allow the FT232B to configure itself and enumerate over USB.

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# 8 UART Interface Configurations

The following sections illustrate possible UART configurations for the FT232B.

## 8.1 USB ⇔ RS232 Converter Configuration

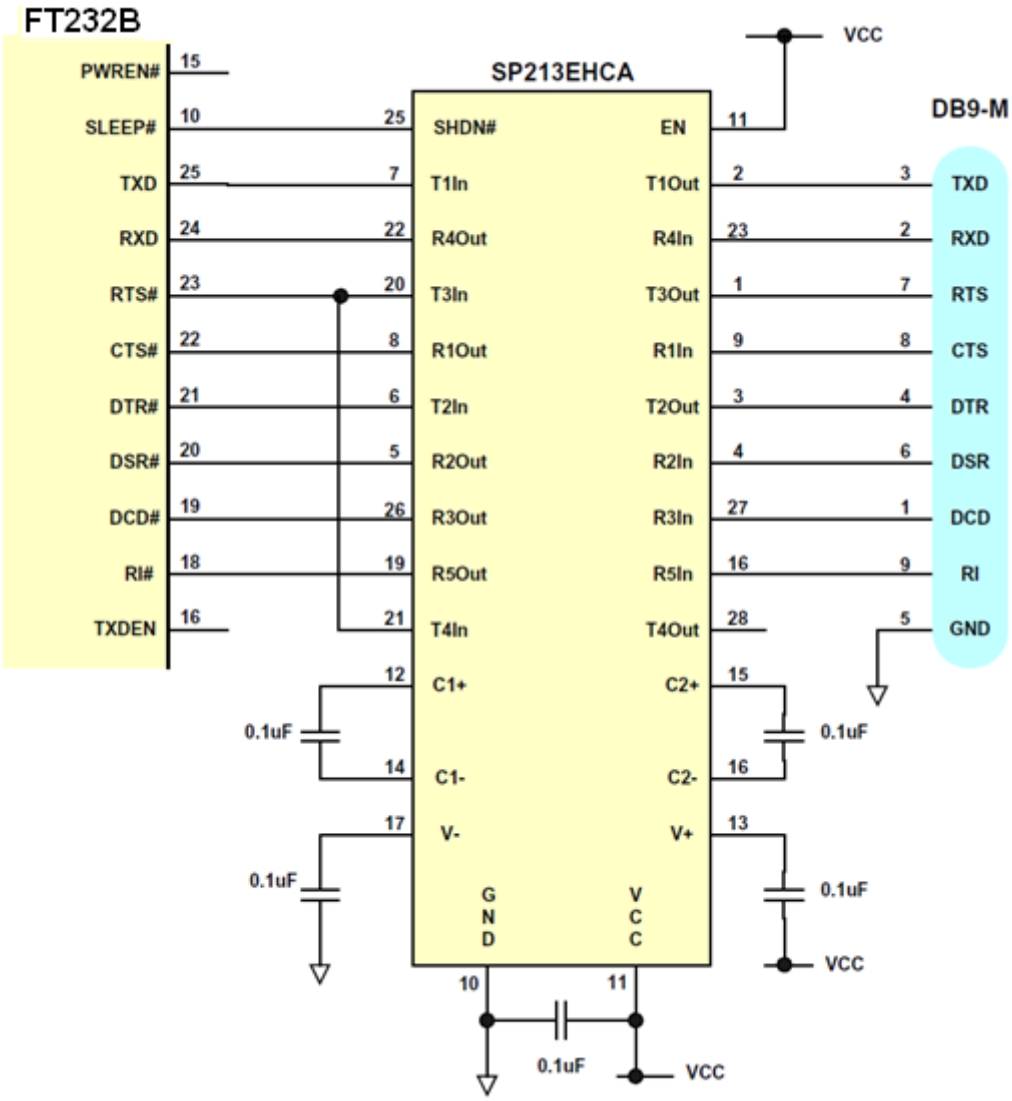



**Figure 8.1 USB-**RS232 Converter Configuration

Figure 7.1 illustrates how to connect the UART interface of the FT232B to a TTL – RS232 Level Converter I.C. to make a USB ⇔ RS232 converter using the popular "213" series of TTL to RS232 level converters. These devices have 4 transmitters and 5 receivers in a 28-pin SSOP package and feature an in-built voltage converter to convert the 5v (nominal) VCC to the ±9 volts required by RS232. An important feature of these devices is the SHDN# pin which can power down the device to a low quiescent current during USB suspend mode.

The device used in the example is a Exar/Sipex SP213EHCA which is capable of RS232 communication at up to 500K baud. If a lower baud rate is acceptable, then several pin compatible alternatives are available such as Sipex SP213ECA , Maxim MAX213CAI and Analog Devices ADM213E which are good for communication at up to 115,200 baud. If a higher baud rate is desired, use a Maxim MAX3245CAI part which is capable of RS232 communication at rates of up to 1M baud. The MAX3245 is not pin compatible with the 213 series devices, also its SHDN pin is active high so connect this to PWREN# instead of SLEEP#.

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## 8.2 USB ⇔ RS422 Converter Configuration

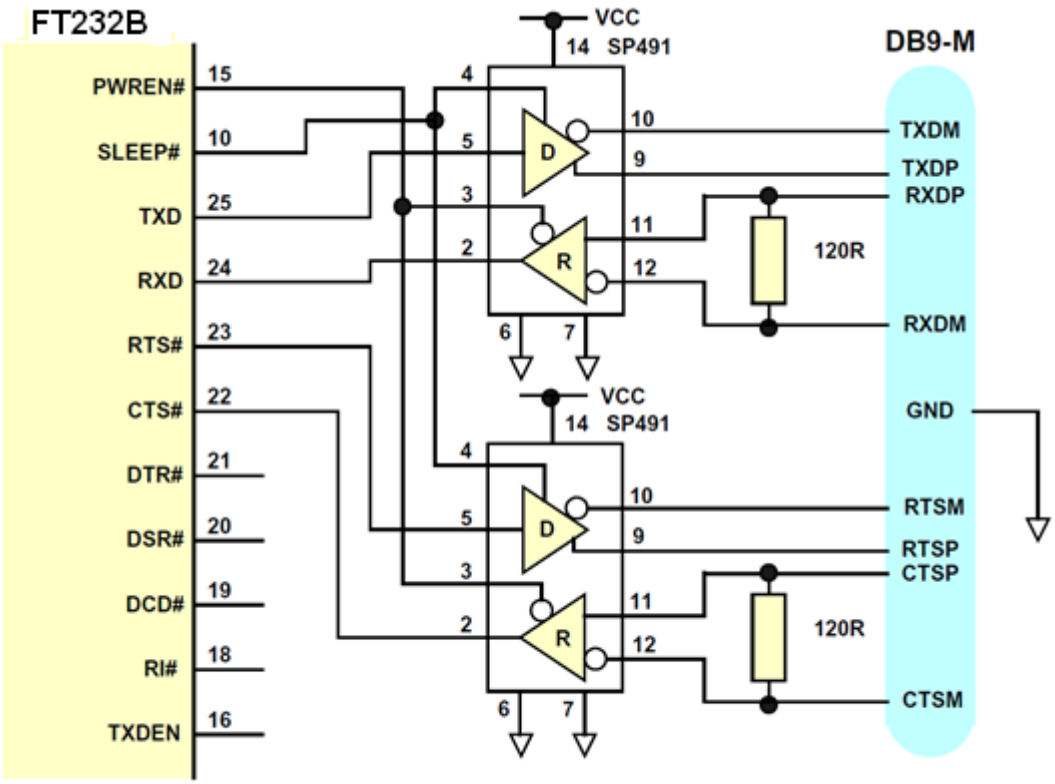



**Figure 8.2 USB-**RS422 Converter Configuration

Figure 8.2 illustrates how to connect the UART interface of the FT232B to a TTL – RS422 Level Converter I.C. to make a USB ⇔ RS422 converter. There are many such level converter devices available – this example uses Exar/Sipex SP491 devices which have enables on both the transmitter and receiver. Because the transmitter enable is active high, it is connected to the SLEEP# pin. The receiver enable is active low and is connected to the PWREN# pin. This ensures that both the transmitters and receivers are enabled when the device is active, and disabled when the device is in USB suspend mode. If the design is USB BUS powered, it may be necessary to use a P-Channel logic level MOSFET (controlled by PWREN#) in the VCC line of the SP491 devices to ensure that the USB standby current of 500uA is met.

The SP491 is good for sending and receiving data at a rate of up to 5M Baud – in this case the maximum rate is limited to 3M Baud by the FT232B

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## 8.3 USB ⇔ RS485 Converter Configuration

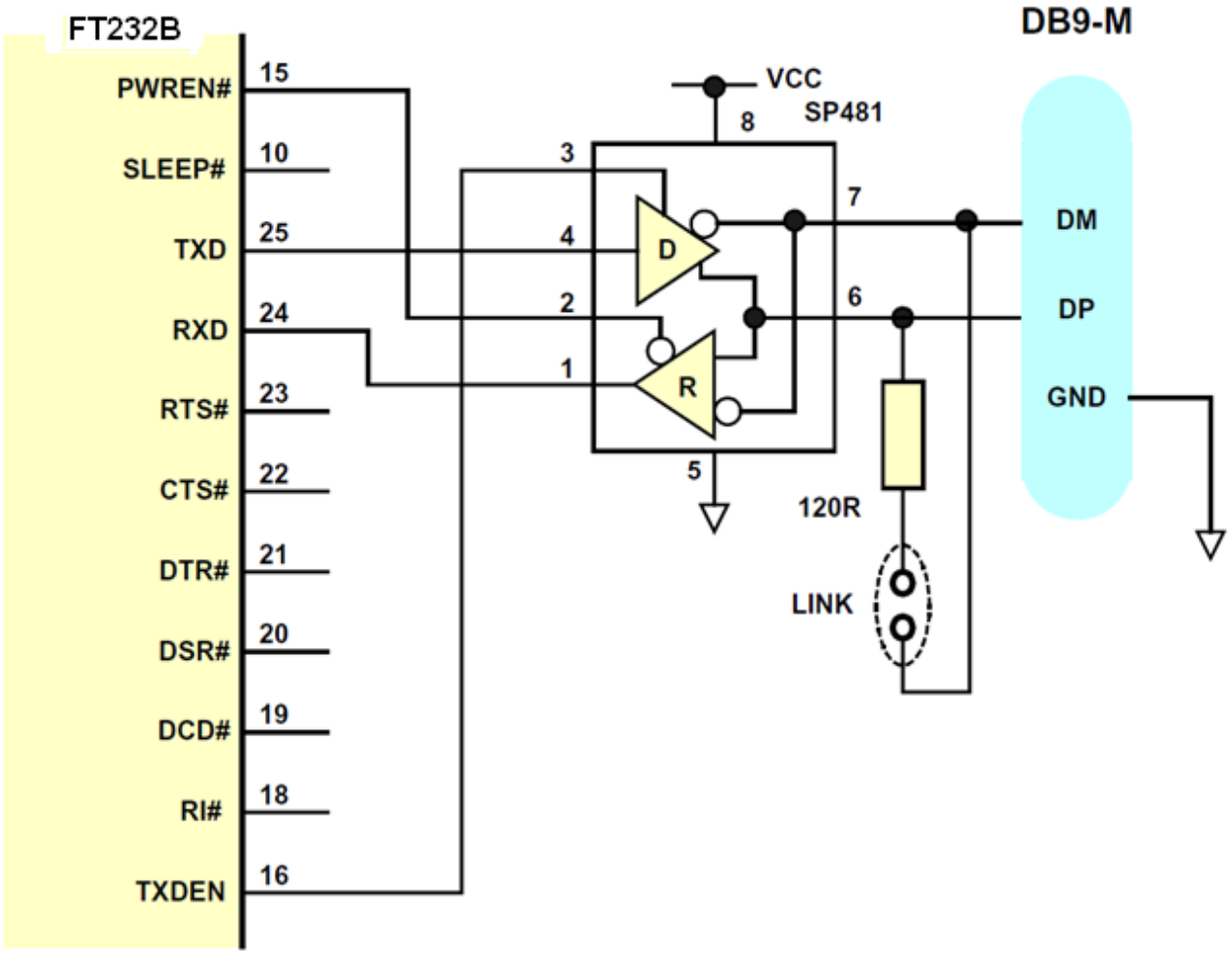



**Figure 8.3 USB-RS485 Converter Configuration**

Figure 7.3 illustrates how to connect the UART interface of the FT232B to a TTL – RS485 Level Converter I.C. to make a USB => RS485 converter. This example uses the Exar/Sipex SP481 device but there are similar parts available from Maxim and Analog Devices amongst others. The SP481 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pin on the FT232B is provided for exactly that purpose and so the transmitter enable is wired to TXDEN. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. A link is provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT232B is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT232B it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT232B is the logical OR of the SP481 receiver output with TXDEN using an HC32 or similar logic gate.

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# 9 LED Interface Configuration

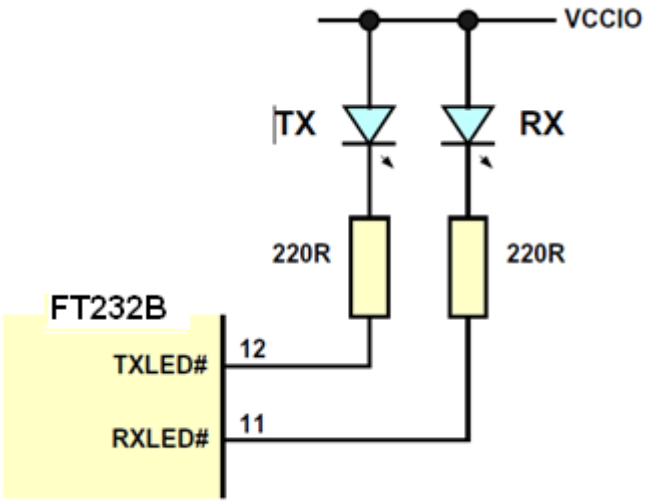



**Figure 9.1 Dual LED Configuration Configuration**

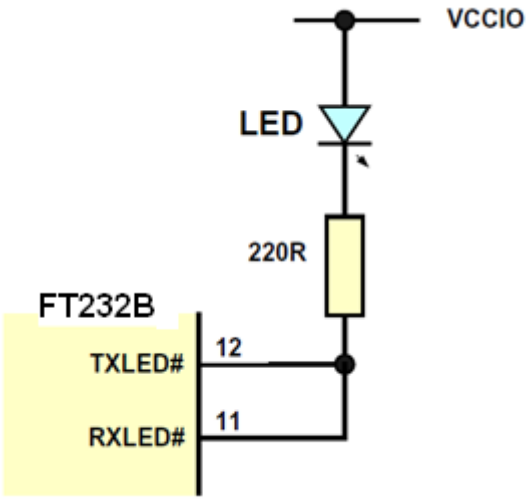



**Figure 9.2 Single LED**

The FT232B has two IO pins dedicated to controlling LED status indicators, one for transmitted data the other for received data. When data is being transmitted / received the respective pins drive from tri-state to low in order to provide indication on the LEDs of data transfer. A digital one-shot timer is used so that even a small percentage of data transfer is visible to the end user.

Figure 9.1 shows a configuration using two individual LED's – one for transmitted data the other for received data.

In figure 9.2, transmit and receive LED indicators are wire-OR'ed together to give a single LED indicator which indicates any transmit or receive data activity.

Another possibility (not shown here) is to use a 3 pin common anode tri-color LED based on the circuit in Figure 9.2 to have a single LED that can display activity in a variety of colors depending on the ratio of transmit activity compared to receive activity.

Note that the LED's are connected to VCCIO.

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# 10 Package Parameters

## 10.1 LQFP Package Dimension

The FT232BL is supplied in a 32 pin LQFP package as standard.

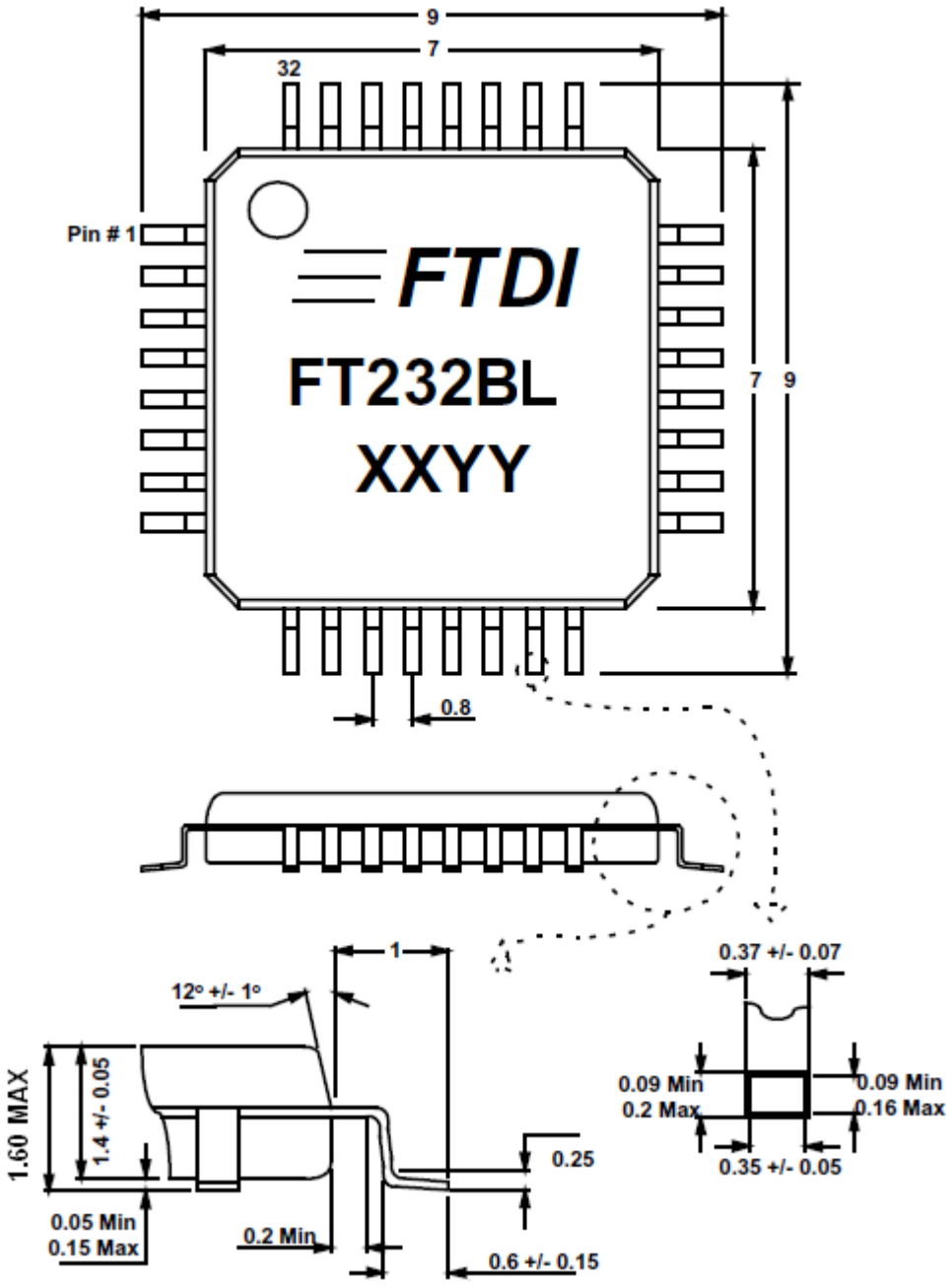



**Figure 10.1 32 LQFP Package Dimensions**

This package has a 7mm x 7mm body (9mm x 9mm including leads) with leads on a 0.8mm pitch. The above drawing shows the LQFP-32 package – all dimensions are in millimeters. Note that there are two date code formats used – XXYY = Date Code where XX = 2 digit year number, YY = 2 digit week number; or XYY-N where X = 1 digit year. Number, YY = 2 digit week number, and –N is an integer.

The FT232BL is fully compliant with the European Union RoHS directive.

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## 10.2 QFN Package Dimension

The FT232BQ is supplied in a 32 pin QFN package as standard.

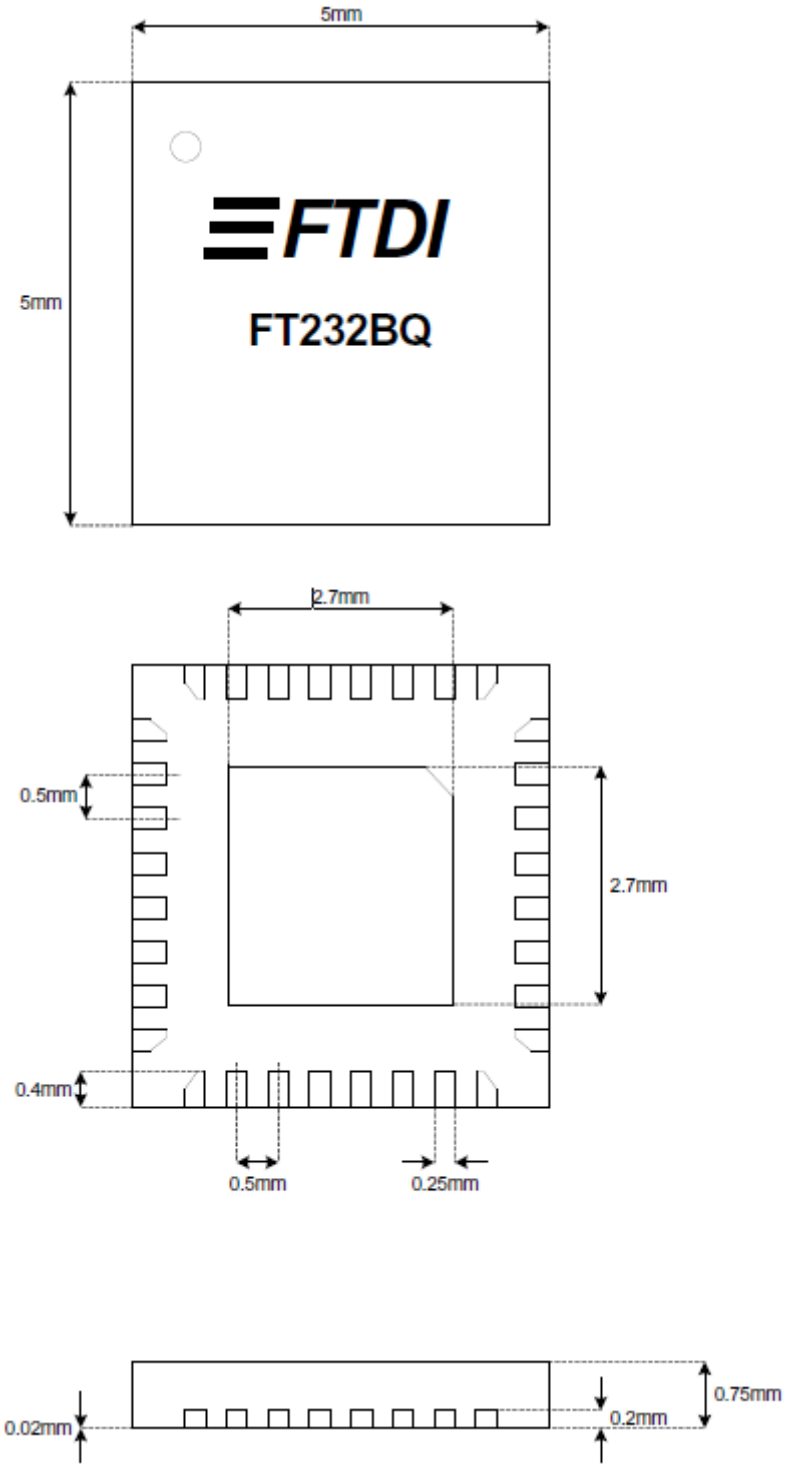



**Figure 10.2 32 LQFP Package Dimensions**

The FT232BQ is supplied in lead (Pb) free, leadless QFN32 package. This package has a 5 mm x 5 mm body with no protruding pins, and is ideal for for projects where package area is critical. In the above drawing all dimensions are in millimetres. Note that two date code formats are used – XXYY = Date Code where XX = 2 digit year number, YY = 2 digit week number; or XYY-1 where X = 1 digit year. Number, YY = 2 digit week number. The FT232BQ is fully compliant with the European Union RoHS directive.

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# Appendix A – References

**Useful Application Notes**

**AN-100, "Using the FT232/FT245R with External Crystal or Oscillator"**

http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

**AN_103, "FTDI Drivers Installation Guide for VISTA".**

http://www.ftdichip.com/Documents/AppNotes/AN_103_FTDI_Drivers_Installation_Guide_for_VISTA(FT_000080).pdf

**AN_104, "FTDI Drivers Installation Guide for Windows XP".**

http://www.ftdichip.com/Documents/AppNotes/AN_104_FTDI_Drivers_Installation_Guide_for_WindowsXP(FT_000093).pdf

**AN_107, "Advanced Driver Options".**

http://www.ftdichip.com/Documents/AppNotes/AN_107_AdvancedDriverOptions_AN_000073.pdf

**AN_120 Aliasing VCP Baud Rates**

http://www.ftdichip.com/Documents/AppNotes/AN_120_Aliasing_VCP_Baud_Rates.pdf

**AN232R-01, "FT232BM/ FT245BM Bit-Bang Mode".**

http://www.ftdichip.com/Documents/AppNotes/AN232B-01_BitBang.pdf

**Configuring FT232R, FT2232 and FT232BM Baud Rates**

http://www.ftdichip.com/Documents/AppNotes/AN232B-05_BaudRates.pdf

**Installation Guides**

http://www.ftdichip.com/Documents/InstallGuides.htm

**Useful Technical Notes**

**TN_100, "USB Vendor ID/Product ID Guidelines"**

http://ftdichip.com/Documents/TechnicalNotes/TN_100_USB_VID-PID_Guidelines.pdf

**TN_102, "OEM Technical Support Requirements for FTDI Products"**

http://ftdichip.com/Documents/TechnicalNotes/TN_102_OEM_Technical_Support_Requirements_for_FTDI_Products.pdf

**TN_104, "Guide to Debugging Customers Failed Driver Installation"**

http://www.ftdichip.com/Documents/TechnicalNotes/TN_104_Guide%20to%20Debugging_Customers_Failed_Driver_%20Installation_%20on_%20Windows.pdf

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# Appendix B – List of Figures and Tables

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# Appendix C – Revision History

| | | |
|---|---|---|
| **Version 1.0** | Initial document created | 30 April 2002. |
| **Version 1.1** | Section 3.2 RESET# Pin description corrected (RESET# does not have an internal 200k pull-up to VCC as previously stated).<br>Section 3.1, figure 2 pin-out corrected (EECS = Pin 32). | 04 August 2002 |
| **Version 1.2** | Pin and package naming made consistent throughout data sheet.<br>Section 1.1 Updated to reflect availability of Mac OS X driver.<br>Section 4.1 Minor corrections.<br>Section 4.2 Minor changes to functional block descriptions of SIE, RESET Generator, and EEPROM interface.<br>Section 3.2 Note added to EEPROM interface group.<br>Section 3.2 RSTOUT# Pin description amended.<br>Section 5.2 Minimum operating supply voltage adjusted.<br>Section 5.2 EESK added to Note 3.<br>Section 5.2 UART IO pin characteristics amended.<br>Section 5.2 RESET#, TEST, EECS, EESK, and EEDATA pin characteristics amended.<br>Section 5.2 RSTOUT pin characteristics amended.<br>Section 7.1 Updated recommended ceramic resonator part number and circuit configuration.<br>Section 6.2 "USB Self Powered Configuration (1)"<br>(original figure 8 removed). Recommended circuit for USB self<br>Powered designs updated. Subsequent figure numbers have<br>changed as a result.<br>Section 6.3.1 Note added to description of Bus powered circuit with 3.3V logic drive / supply voltage.<br>Section 7.6 Self Powered Circuit with 3.3V logic drive / supply voltage added (new figure 16). | 27 October 2003 |
| **Version 1.3** | Section 10 Package drawing amended<br>Section 5.1 Floor Life / Relative Humidity specification added. ESD and Latch Up specifications amended.<br>Section 7.1 Required resonators / crystal accuracy corrected. | 10 December 2003 |
| **Version 1.4** | Grammar Corrections<br>Section 11 FTDI Address Updated<br>Section 4.1 Extended EEPROM Support corrected<br>Section 3.2 VCCIO Pin description amended.<br>Section 8.3 RS485 Example Sipex SP481 part number corrected. | 10 February 2004 |
| **Version 1.5** | Section 3.2 EESK Pin Description amended.<br>Section 6.3.1 Figure 16 PWRCTL Pin number corrected.<br>Section 6.4 Figure 15 PWREN# Pin number corrected. | April 2004 |
| **Version 1.6** | Section 1.1 WinCE drivers now available.<br>Section 10 Date code format updated.<br>Section 5.1 Absolute Maximum Ratings table reformatted. | November 2004 |
| **Version 1.7** | Section 1.1 D2XX drivers for Linux and Windows CE now available<br>Section 10 FT232BL (lead Free) and FT232BQ (lead free QFN package) now available. | February 2005 |
| **Version 1.8** | Section 1.1 Driver OS Support updated.<br>Section 5.1 USB Data line absolute maximum rating added. | December 2005 |
| **Version 1.9** | Reformatted and make one datasheet for two Ics<br>(FT232BL and FT232BQ)<br>Updated to remove references to isochronous support<br>Edited contact details<br>Added Window 7 and Vista support | 9th August 2010 |

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| | | |
|---|---|---|
| **Version 2.0** | Edited title, FT232BQ/BL photo, section in 3.1 and sction1.2 | 15th Sept 2010 |
| **Version 2.1** | Edited Section 6, circuit diagrams, Figure 6.1 and 6.2.<br>Corrected BQ reel quantity from 1,000 to 2,500 | 19th Jan 2011 |
| **Version 2.2** | Corrected Minimum Input Switching Threshold Voltage (table 5.3) | 07th Nov 2011 |

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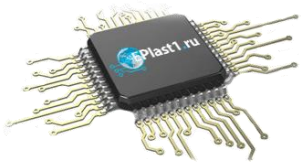
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