DS1803

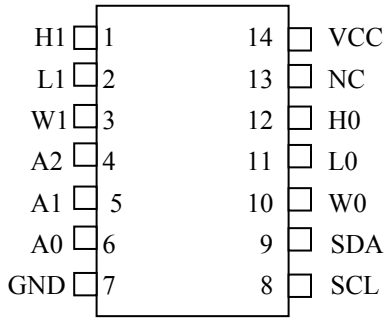
Addressable Dual Digital Potentiometer

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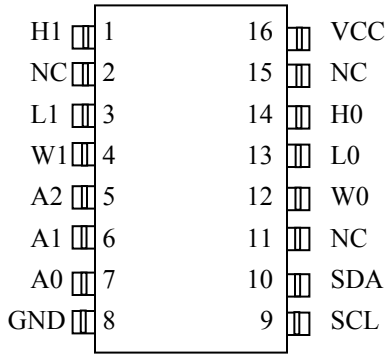
FEATURES

- 3V or 5V Operation
- Ultra-Low Power Consumption
- Two Digitally Controlled, 256-Position Potentiometers
- 14-Pin TSSOP (173 mil) and 16-Pin SO (150 mil) Packaging Available for Surface-Mount Applications
- Addressable Using 3 Address Inputs
- 2-Wire Serial Interface
- Operating Temperature Range:
  - Industrial: -40°C to +85°C
- Standard Resistance Values:
  - DS1803-010 10kΩ
  - DS1803-050 50kΩ
  - DS1803-100 100kΩ

PIN ASSIGNMENT



DS1803 14-PIN TSSOP (173 MIL)



DS1803Z 16-PIN SO (150 MIL)
DS1803 16-PIN DIP (300 MIL)
See Mech. Drawings Section on Website

PIN DESCRIPTION

L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W0,W1	-	Wiper terminal of Resistor
V_{CC}	-	3V/5V Power Supply Input
A0, A1, A2	-	Chip Select Inputs
SDA	-	Serial Data I/O
SCL	-	Serial Clock Input
GND	-	Ground
NC	-	No Connection

DESCRIPTION

The DS1803 addressable dual digital potentiometer features two independently controlled 256-position potentiometers. Device control is achieved through a 2-wire serial interface. Three address pins allow up to 8 DS1803's to share the same 2-wire interface. The exact wiper position of each potentiometer can be written or read. The DS1803 is available in a 16-pin DIP, 16-pin SO, and 14-pin TSSOP package. The device is available in three standard resistance values: 10kΩ, 50kΩ, and 100kΩ and is specified over the industrial temperature range.

DEVICE OPERATION

The DS1803 is an addressable, digitally controlled device which has two 256-position potentiometers. A functional block diagram of the part is shown in Figure 1. Communication and control of the device is accomplished via a 2-wire serial interface. Address inputs A0, A1, and A2 allow up to 8 DS1803s to share the same 2-wire interface.

Each potentiometer is composed of a 256 position resistor array. Two 8-bit registers, each assigned to a respective potentiometer, are used to set the wiper position on the resistor array. The wiper terminal is multiplexed to one of 256 positions on the resistor array based on its corresponding 8-bit register value. For example, the high-end terminals, H0 and H1, have wiper position values FFh while the low-end terminals, L0 and L1, have wiper position values 00h.

The DS1803 is a volatile device that does not maintain the position of the wiper during power-down or loss of power. On power-up, the DS1803 wipers' position will be set to position 00h - the low-end terminals. The user may then set the wiper value to a desired position.

Communication with the DS1803 takes place over the 2-wire serial interface consisting of the bi-directional pin, SDA, and the serial clock input, SCL. Complete details of the 2-wire interface are discussed in the section entitled "2-wire Serial Data Bus."

Application Considerations

The DS1803 is offered in three standard resistor values, which include 10kΩ, 50kΩ, and 100kΩ. The resolution of the potentiometer is defined as $R_{TOT}/255$, where R_{TOT} is the total resistor value of the potentiometer. The DS1803 is designed to operate using 3V or 5V power supplies over the industrial (-40°C to +85°C) temperature range. Maximum input signal levels across the potentiometer cannot exceed the operating power supply of the device.

2-WIRE SERIAL DATA BUS

The DS1803 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1803 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 2).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 2 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ * bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. **Data transfer from a master transmitter to a slave receiver:** The first byte transmitted by the master is the control byte (slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. **Data transfer from a slave transmitter to a master receiver:** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1803 may operate in the following two modes:

1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1803 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

The control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1803, this is 0101 binary. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the devices on the bus are to be accessed. The last bit of the control byte ($R/\overline{W}$*) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Figure 3 shows the control byte for the DS1803.

Following the START condition, the DS1803 monitors the SDA bus for the control byte being transmitted. Upon receiving a matching control byte, the DS1803 outputs an acknowledge signal on the SDA line.

COMMAND AND PROTOCOL

The command and protocol structure of the DS1803 allows the user to read or write the potentiometer(s). The command structures for the part are presented in Figures 4 and 5. Data is transmitted most significant bit (MSB) first. During communication, the receiving unit always generates the acknowledge.

Reading the DS1803

As shown in Figure 4, the DS1803 provides one read command operation. This operation allows the user to read both potentiometers. Specifically, the $R/\overline{W}$ bit of the control byte is set equal to a 1 for a read operation. Communication to read the DS1803 begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1803, the part will respond with an ACKNOWLEDGE. The $R/\overline{W}$ bit of the control byte as stated should be set equal to '1' for reading the DS1803.

When the master has received the ACKNOWLEDGE from the DS1803, the master can then begin to receive potentiometer wiper data. The value of the potentiometer-0 wiper position will be the first returned from the DS1803. Once the eight bits of the potentiometer-0 wiper position has been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. However, if the value of the potentiometer-1 wiper position value is needed, communication transfer can continue by clocking the remaining eight bits of the potentiometer-1 value, followed by an NOT ACKNOWLEDGE. Final communication transfer is terminated by issuing the STOP command.

Writing the DS1803

A data flow diagram for writing the DS1803 is shown in Figure 5. The DS1803 has three write commands. These include write pot-0, write pot-1, and write pot-0/1. The write pot-0 command allows the user to write the value of potentiometer-0 and as an option the value of potentiometer-1. The write-1 command allows the user to write the value of potentiometer-1 only. The last write command, write-0/1, allows the user to write both potentiometers to the same value with one command and one data value being issued.

All the write operations begin with a START condition. Following the START condition, the master device will issue the control byte. The read/write bit of the control byte will be set to '0' for writing the DS1803. Once the control byte has been issued and the master receives the acknowledgment from the DS1803, the command byte is transmitted to the DS1803. As mentioned above, there exist three write

operations that can be used with the DS1803. The binary value of each write command is shown in Figure 5 and also in the Table 1.

2-WIRE COMMAND WORDS Table 1

COMMAND	COMMAND VALUE
Write Potentiometer-0	101010 01
Write Potentiometer-1	101010 10
Write Both Potentiometers	101011 11

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-40° to +85°C; industrial
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Resistors Inputs	L,H,W	GND-0.5		V_{CC}+0.5	V	1

DC ELECTRICAL CONDITIONS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current (Active)	I_{CC}				200	µA	3
Input Leakage	I_{LI}		-1		+1	µA	
Wiper Resistance	R_W			400	1000	ohms	
Wiper Current	I_W				1	mA	
Input Logic 1	V_{IH}		$0.7V_{CC}$		V_{CC}+0.5	V	2
Input Logic 0	V_{IL}		-0.5		$0.3V_{CC}$	V	2
Input Logic Levels A0, A1, A2		Input Logic 1 Input Logic 0	$0.7V_{CC}$ -0.5		V_{CC}+0.5 $0.3V_{CC}$	V	12
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{CC}$	-10		+10	µA	
Standby Current	I_{STBY}			20	40	µA	4
Low Level Output Voltage	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/0}$				10	pF	
Pulse Width of Spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C;V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistor Tolerance		-20		+20	%	17
Absolute Linearity			±0.75		LSB	13
Relative Linearity			±0.3		LSB	14
-3 dB Cutoff Frequency	f_{CUTOFF}				Hz	11
Temperature Coefficient			750		ppm/°C	
Capacitance	C_I			5	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C;V_{CC}=2.7V to 5.5V)

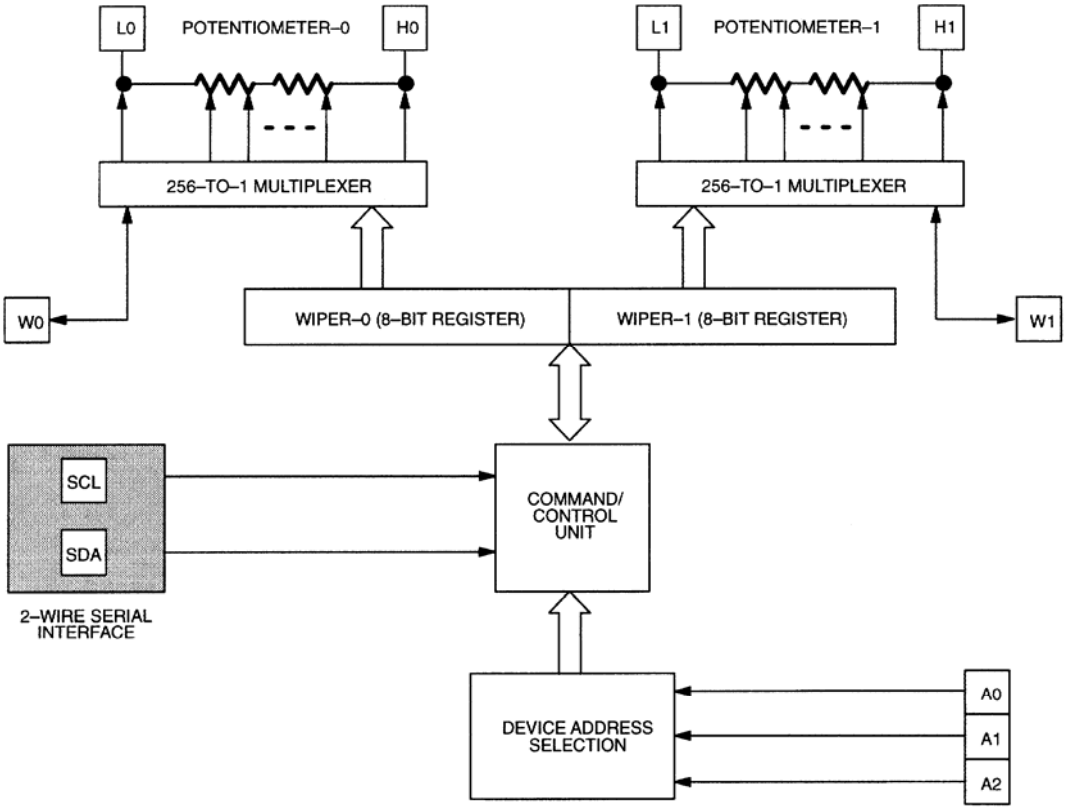
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	0 0		400 100	kHz	15 16
Bus Free Time Between STOP and START Condition	t_{BUF}	1.3 4.7			µs	15 16
Hold Time (Repeated) START Condition	$t_{HD:STA}$	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	0.6 4.0			µs	
Data Hold Time	$t_{HD:DAT}$	0 0		0.9	µs	6,7
Data Setup Time	$t_{SU:DAT}$	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	$20+1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	$20+1C_B$		300 300	ns	9
Setup Time for STOP Condition	$t_{SU:STO}$	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_B			400	pF	9

NOTES:

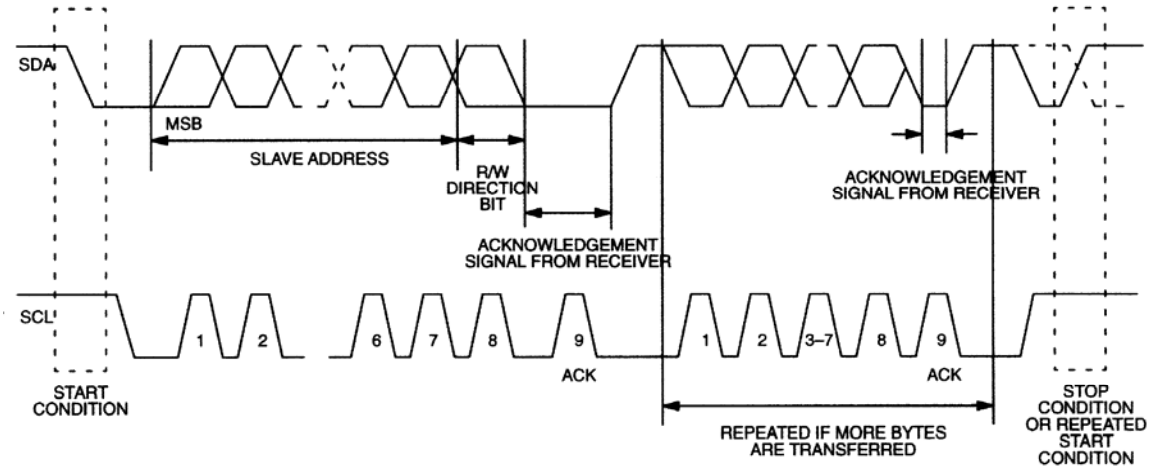
1. All voltages are referenced to ground. Currents flowing into device pins are positive. Currents out of the device pins are negative.
2. I/O pins of fast mode devices will not obstruct SDA and SCL even if V_{CC} is switched off.
3. I_{CC} specified with SDA pin open, SCL = 400 kHz clock rate.
4. I_{STBY} specified with V_{CC} at 5.0V and SDA, SCL = 5.0V.

5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.
9. C_B - total capacitance of one bus line in picofarads, timing referenced to $(0.9)(V_{CC})$ and $(0.1)(V_{CC})$.
10. Typical values are for $t_A = 25°C$ and nominal supply voltage.
11. -3 dB cutoff frequency characteristics for the DS1803 depend on potentiometer total resistance: DS1803-010; 1 MHz, DS1803-50; 200 kHz, DS1803-100; 100 kHz.
12. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.
13. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits are ±1.6 LSB.
14. Relative linearity is used to determine the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
15. Fast mode.
16. Standard mode.
17. Valid at 25°C only.

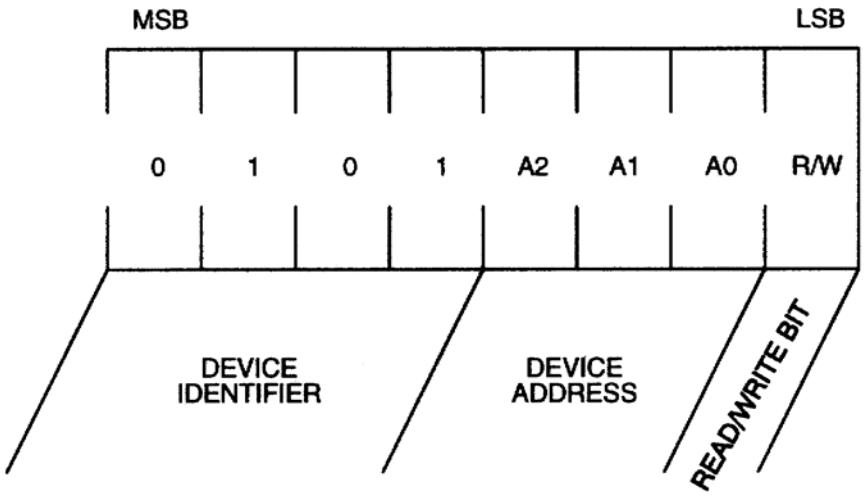
DS1803 BLOCK DIAGRAM Figure 1



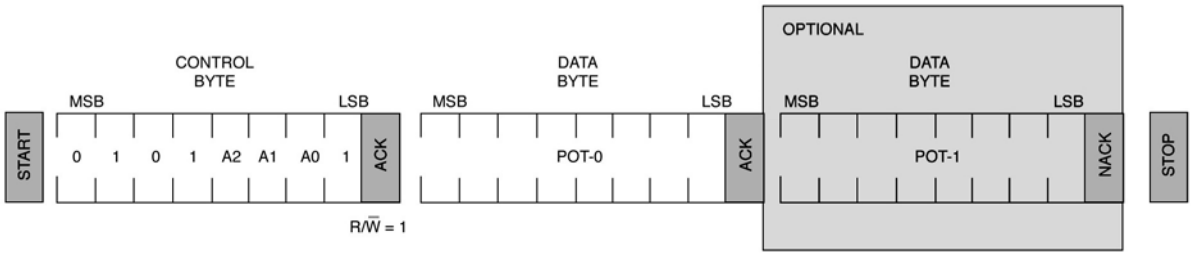
2–WIRE DATA TRANSFER OVERVIEW Figure 2



CONTROL BYTE Figure 3

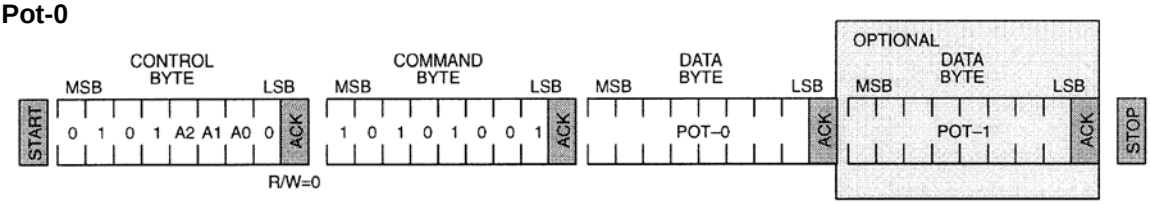


2–WIRE READ PROTOCOL Figure 4

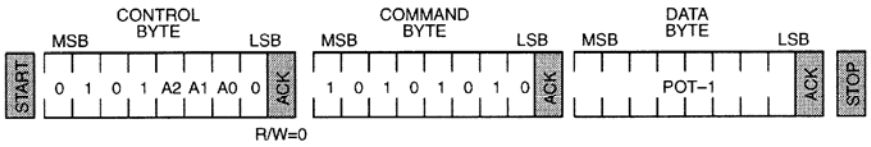


2–WIRE WRITE PROTOCOL Figure 5

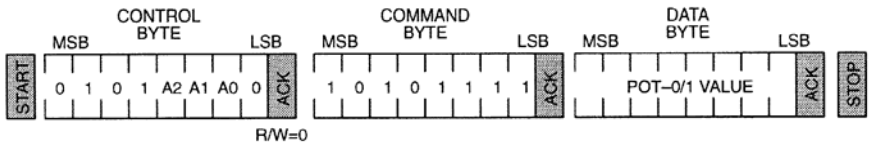
Write Pot-0



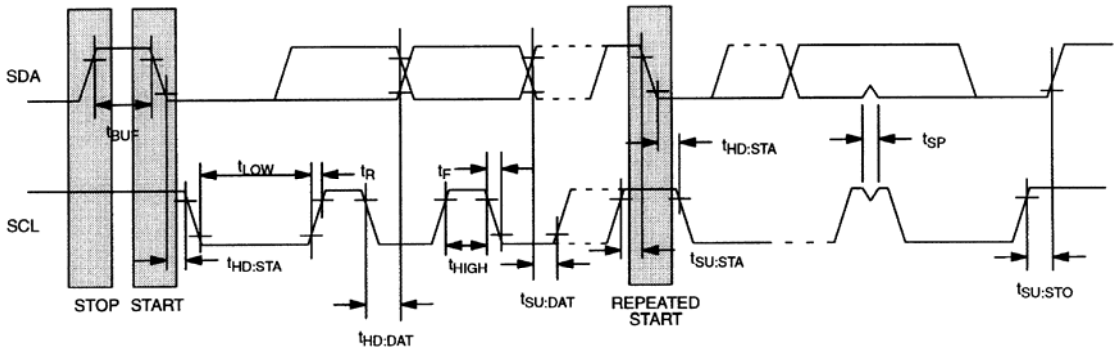
Write Pot–1



Write Pot–0/1 (same value)



TIMING DIAGRAM Figure 6



DS1803 ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	VERSION
DS18030-010	16L DIP	-40°C TO +85°C	10 kΩ
DS18030-050	16L DIP	-40°C TO +85°C	50 kΩ
DS18030-100	16L DIP	-40°C TO +85°C	100 kΩ
DS1803E-010	14L TSSOP (173 MIL)	-40°C TO +85°C	10 kΩ
DS1803E-050	14L TSSOP (173 MIL)	-40°C TO +85°C	50 kΩ
DS1803E-100	14L TSSOP (173 MIL)	-40°C TO +85°C	100 kΩ
DS1803Z-010	16L SOIC (150 MIL)	-40°C TO +85°C	10 kΩ
DS1803Z-050	16L SOIC (150 MIL)	-40°C TO +85°C	50 kΩ
DS1803Z-100	16L SOIC (150 MIL)	-40°C TO +85°C	100 kΩ
DS1803E-010+	14L TSSOP (173 MIL) LEAD FREE	-40°C TO +85°C	10 kΩ
DS1803E-50+	14L TSSOP (173 MIL) LEAD FREE	-40°C TO +85°C	50 kΩ
DS1803E-100+	14L TSSOP (173 MIL) LEAD FREE	-40°C TO +85°C	100 kΩ
DS1803E-010+T&R	14L TSSOP (173 MIL) LEAD FREE T&R	-40°C TO +85°C	10 kΩ
DS1803E-50+T&R	14L TSSOP (173 MIL) LEAD FREE T&R	-40°C TO +85°C	50 kΩ
DS1803Z-010+	16L SOIC (150 MIL) LEAD FREE	-40°C TO +85°C	10 kΩ
DS1803Z-050+	16L SOIC (150 MIL) LEAD FREE	-40°C TO +85°C	50 kΩ
DS1803Z-100+	16L SOIC (150 MIL) LEAD FREE	-40°C TO +85°C	100 kΩ
DS1803Z-010+T&R	16L SOIC (150 MIL) LEAD FREE T&R	-40°C TO +85°C	10 kΩ
DS1803Z-050+T&R	16L SOIC (150 MIL) LEAD FREE T&R	-40°C TO +85°C	50 kΩ
DS1803Z-100+T&R	16L SOIC (150 MIL) LEAD FREE T&R	-40°C TO +85°C	100 kΩ
DS1803-100+T&R	16L DIP T&R	-40°C TO +85°C	100 kΩ
DS1803E-10/T&R	14L TSSOP (173 MIL) T&R	-40°C TO +85°C	10 kΩ
DS1803E-50/T&R	14L TSSOP (173 MIL) T&R	-40°C TO +85°C	50 kΩ
DS1803E-100/T&R	14L TSSOP (173 MIL) T&R	-40°C TO +85°C	100 kΩ
DS1803Z-010/T&R	16L SOIC (150 MIL) T&R	-40°C TO +85°C	10 kΩ
DS1803Z-050/T&R	16L SOIC (150 MIL) T&R	-40°C TO +85°C	50 kΩ
DS1803Z-100/T&R	16L SOIC (150 MIL) T&R	-40°C TO +85°C	100 kΩ

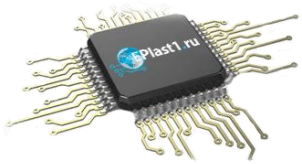
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