OKI Semiconductor

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ML63512A/63514A

4-Bit Microcontroller with Built-in Level Detector, Melody Circuit, and Comparator, Operating at 0.9 V (Min.)

GENERAL DESCRIPTION

The ML63512A/63514A is a CMOS 4-bit microcontroller with built-in level detector and operates at 0.9 V (min.).
The ML63512A/63514A is an M6351x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.
The program memory capacity and data memory capacity of the ML63512A differ from those of the ML63514A.
48-pin TQFP and 64-pin TQFP packages are available for the ML63512A and ML63514A.

FEATURES

- Extensive instruction set
  407 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, jump, conditional branch, call/return, control.

- Wide variety selection of addressing modes
  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.

- Processing speed
  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

- Clock generation circuit
  Low-speed clock : Crystal oscillation or RC oscillation selectable by mask option (30 to 80 kHz)
  High-speed clock : Ceramic oscillation or RC oscillation selectable by mask option (2 MHz max.)

- Program memory space
  ML63512A: 4K words
  ML63514A: 8K words
  Basic instruction length is 16 bits/1 word

- Data memory space
  ML63512A: 128 nibbles
  ML63514A: 256 nibbles

- Stack level

Call stack level	:	16 levels
Register stack level	:	16 levels

- I/O ports

Input ports: Selectable as input with pull-up resistor/high-impedance input
Output ports: N-channel open drain output (can directly drive LEDs)
Input-output ports: Selectable as input with pull-up resistor/high-impedance input
Selectable as N-channel open drain output/CMOS output
Can be interfaced with external peripherals that use a different power supply than this device uses. (Power to the output port is supplied from V_{DDI} (separate power suply))
Number of ports:

(For 48-pin packages)

Input port	:	1 port × 4 bits
Output port	:	1 port × 4 bits
Input-output port	:	6 ports × 4 bits

(For 64-pin packages)

Input port	:	1 port × 4 bits
Output port	:	1 port × 4 bits
Input-output port	:	9 ports × 4 bits

- Melody output function

Melody sound frequency	:	529 to 2979 Hz (@ 32.768 kHz)
Tone length	:	63 varieties
Tempo	:	15 varieties
Melody data	:	Stored in the program memory
Number of ports	:	1 (dedicated pin)
Buzzer driver signal output	:	4 kHz (@ 32.768 kHz)

- Level detector

Conversion time	:	Approx. 183 µs (@ 32.768 kHz)
Dedicated input pins	:	2 pins (switched by software; for the secondary functions of the input ports)
Detection level	:	12 levels

- Comparator

Offset voltage	:	50 mV max. (V_{DD} = 1.5 V)
Comparison time	:	Approx. 183 µs (@ 32.768 kHz)
Number of channels	:	1 (for the secondary functions of the input ports)

- Reset function

Reset through RESETB pin (RESETB pin can be pulled up by mask option)

- Power supply backup

Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
  8-bit timer × 2
  Selectable as auto-reload mode/capture mode/clock frequency measurement mode
  15-bit time base counter × 1
  1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz, 256 Hz, 512 Hz, 1 kHz, and 2 kHz signals can be read (@ 32.768 kHz)

- Serial port

Mode	:	Selectable as UART mode/synchronous mode
UART communication speed	:	2TBCCLK, TBCCLK, 1/2TBCCLK, Timers 0 & 1 overflow 24 kbps Max. (when 2TBCCLK @ 80 kHz selected)
Clock frequency in synchronous mode	:	30 to 80 kHz (internal clock mode), external clock frequency
Data length	:	5 to 8 bits

- Interrupt sources

External interrupt (4 sources)	:	Selectable as rising edge/falling edge/both rising and falling edges
Internal interrupt (10 sources)	:	Time base interrupt × 4 (2, 4, 16, and 32 Hz @ 32.768 kHz) Timer interrupt × 2 Level detector interrupt × 1 Serial port reception interrupt × 1 Serial port transmission interrupt × 1 Melody end interrupt × 1

- Operating Temperature
  –20 to +70°C

- Supply voltage

When backup used	:	0.9 to 1.8 V (Maximum operating frequency 1 MHz)
When backup not used	:	1.8 to 3.5 V (When Level detector or Comparator is used, maximum operating frequency 2 MHz) 1.8 to 5.5 V (When Level detector and Comparator are not used, maximum operating frequency 2 MHz)

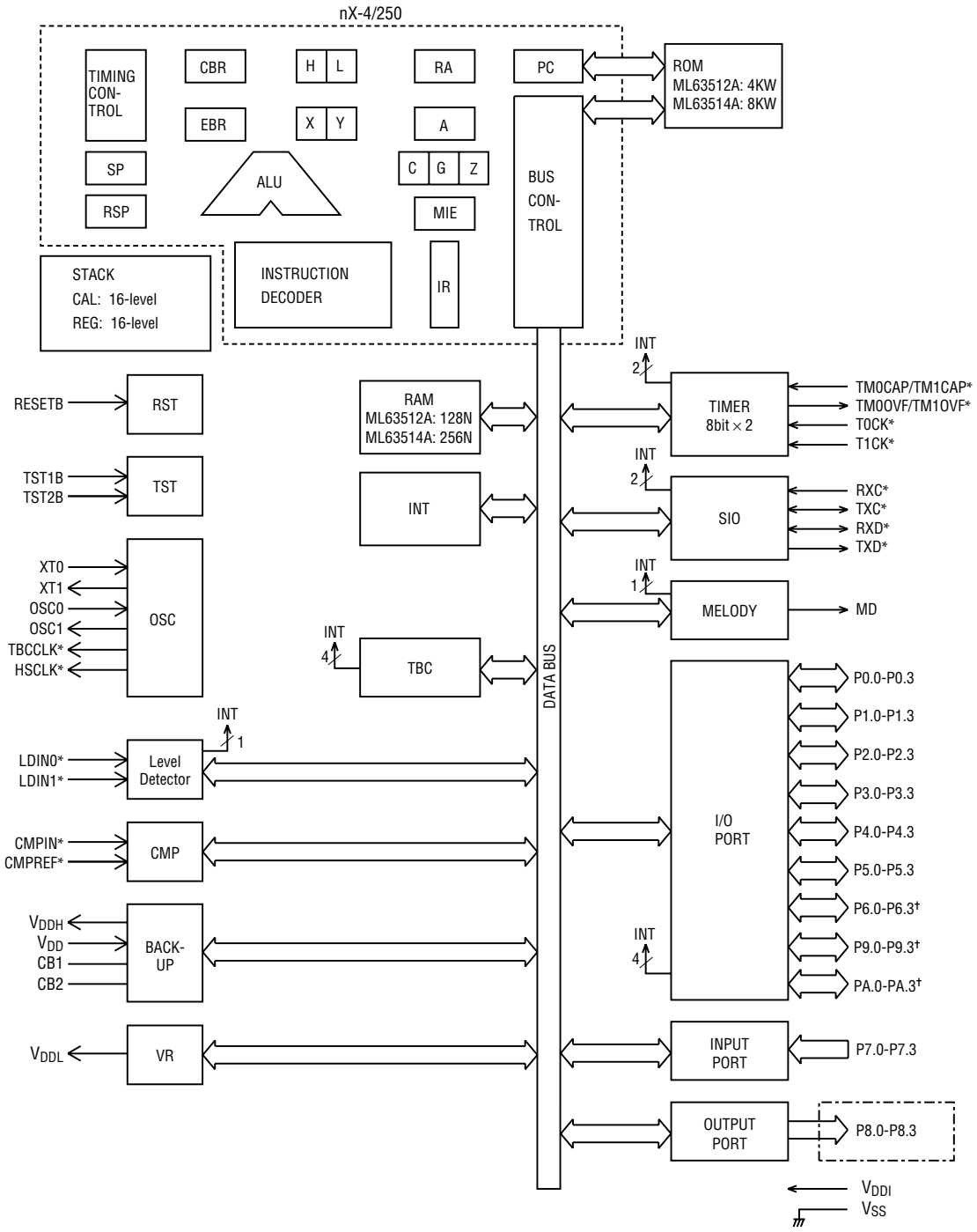
- Package options:

48-pin plastic TQFP (TQFP48-P-0707-0.50-K)	:	(Product name: ML63512A-xxxTB, ML63514A-xxxTB)
64-pin plastic TQFP (TQFP64-P-1010-0.50-K)	:	(Product name: ML63512A-xxxTP, ML63514A-xxxTP)

xxx indicates a code number.

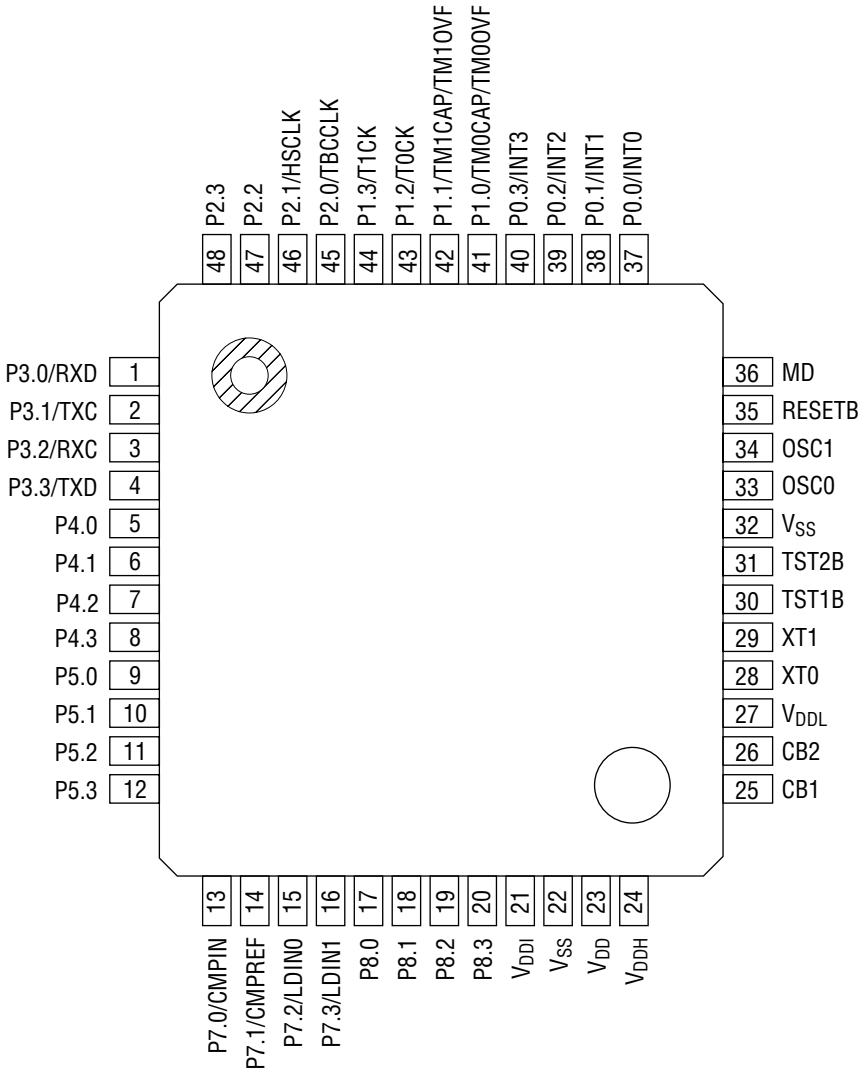
BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function. The power to the circuits corresponding to the signal names inside ⬚ is supplied from V_{DDI} (power supply for interface).



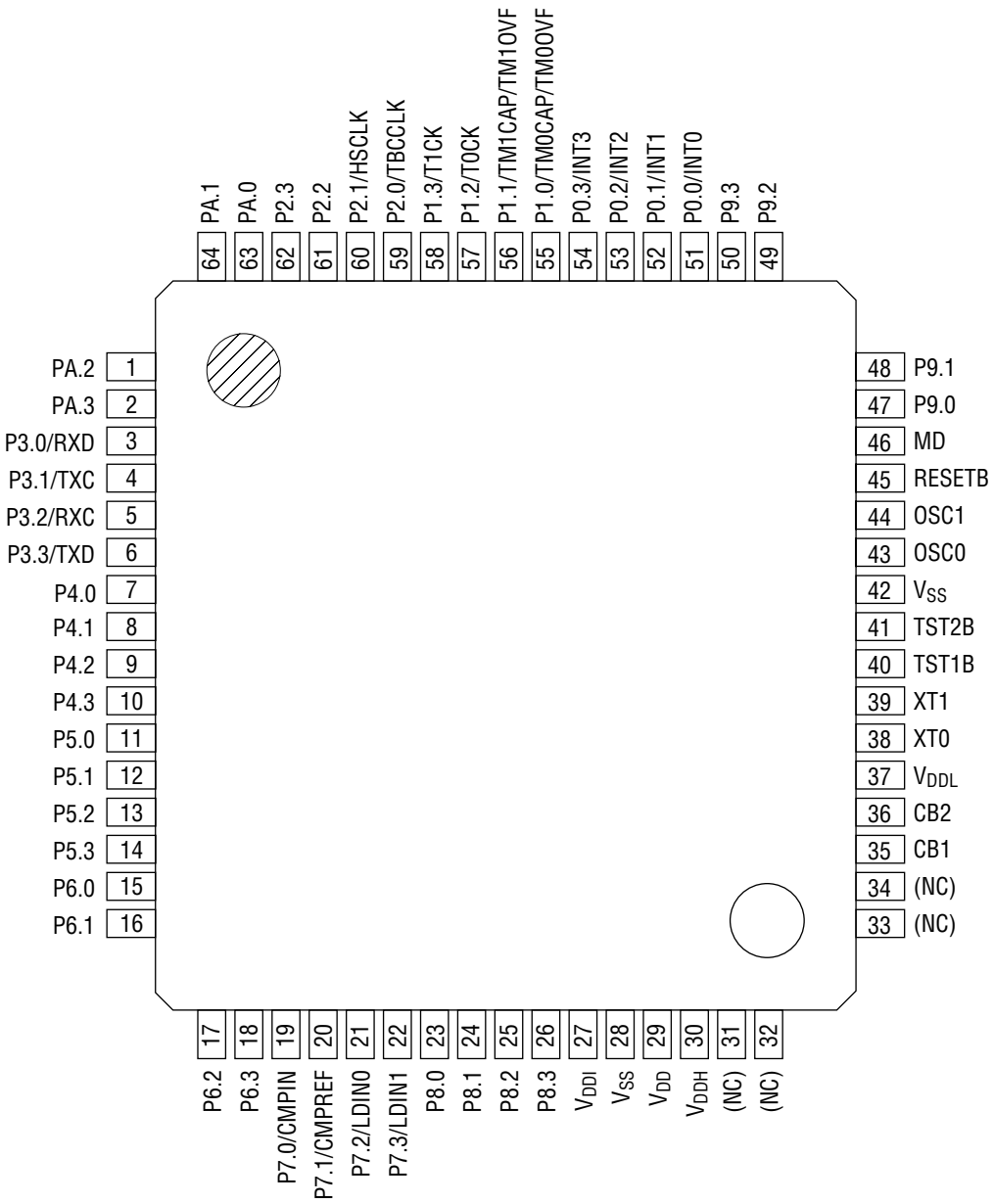
†Port 6 (P6.0 to P6.3), Port 9 (P9.0 to P9.3) and Port A (PA.0 to PA.3) are only provided for the 64-pin packages.

PIN CONFIGURATION (TOP VIEW)



48-Pin Plastic TQFP

PIN CONFIGURATION (TOP VIEW) (continued)



64-Pin Plastic TQFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PIN DESCRIPTIONS

The basic functions of each pin of the ML63512A/63514A are described in Table 1.
A symbol with a slash (/) denotes a pin that has a secondary function.
Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.
For pin, "TB" denotes a 48-pin flat package (48TQFP), and "TP" a 64-pin flat package (64TQFP).

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin		Type	Description
		TB	TP		
Power Supply	V_{DD}	23	29	—	Positive power supply
	V_{SS}	22, 32	28, 42	—	Negative power supply
	V_{DDI}	21	27	—	Positive power supply pin for external interface (PORT8 supply)
	V_{DDL}	27	37	—	Positive power supply pin for internal logic (internally generated). A capacitor C_l (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DDH}	24	30	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor C_h (1.0 μF) should be connected between this pin and V_{SS}.
	CB1	25	35	—	Pins to connect a capacitor for voltage multiplier.
	CB2	26	36	—	A capacitor (1.0 μF) should be connected between CB1 and CB2.
Oscillation	XT0	28	38	I	Low-speed clock oscillation pins. Crystal oscillation or RC oscillation is selected by the mask option. If crystal oscillation is selected, connect a crystal between XT0 and XT1, and connect capacitor (C_G) between XT0 and V_{SS}. If RC oscillation is selected, connect external oscillation resistor (R_{CRL}) between XT0 and XT1.
	XT1	29	39	O	
	OSC0	33	43	I	High-speed clock oscillation pins. Ceramic oscillation or RC oscillation is selected by the mask option. If ceramic oscillation is selected, connect a ceramic resonator between OSC0 and OSC1, and connect capacitor (C_{L0}, C_{L1}) between OSC0 and V_{SS}, OSC1 and V_{SS}. If RC oscillation is selected, connect external oscillation resistor (R_{CRH}) between OSC0 and OSC1.
	OSC1	34	44	O	
Test	TST1B	30	40	I	Input pins for testing.
	TST2B	31	41	I	A pull-up resistor is internally connected to these pins.
Reset	RESETB	35	45	I	Reset input pin. Setting this pin to "L" level puts this device into a reset state. Then, setting this pin to "H" level starts executing an instruction from address 0000H. An internal or external pull-up resistor is selected by mask option.
Melody	MD	36	46	O	Melody output pin (non-inverted output)

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin		Type	Description
		TB	TP		
Port	P0.0/INT0	37	51	I/O	4-bit input-output ports. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit.
	P0.1/INT1	38	52		
	P0.2/INT2	39	53		
	P0.3/INT3	40	54		
	P1.0/ TM0CAP/ TM0OVF	41	55	I/O	
	P1.1/ TM1CAP/ TM1OVF	42	56		
	P1.2/T0CK	43	57		
	P1.3/T1CK	44	58		
	P2.0/TBCCLK	45	59	I/O	
	P2.1/HSCLK	46	60		
	P2.2	47	61		
	P2.3	48	62		
	P3.0/RXD	1	3	I/O	
	P3.1/TXC	2	4		
	P3.2/RXC	3	5		
	P3.3/TXD	4	6		
	P4.0	5	7	I/O	
	P4.1	6	8		
	P4.2	7	9		
	P4.3	8	10		
	P5.0	9	11	I/O	
	P5.1	10	12		
	P5.2	11	13		
	P5.3	12	14		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin		Type	Description
		TB	TP		
Port	P6.0	—	15	I/O	4-bit input-output port. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit. Note that these pins are available for only a 64-pin package.
	P6.1	—	16		
	P6.2	—	17		
	P6.3	—	18		
	P7.0/CMPIN	13	19	I	4-bit input port. Pull-up resistor input or high-impedance input is selectable for each bit.
	P7.1/CMPREF	14	20		
	P7.2/LDIN0	15	21		
	P7.3/LDIN1	16	22		
	P8.0	17	23	O	4-bit output port. N-channel open drain output.
	P8.1	18	24		
	P8.2	19	25		
	P8.3	20	26		
	P9.0	—	47	I/O	4-bit input-output ports. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit. Note that these pins are available for only a 64-pin package.
	P9.1	—	48		
	P9.2	—	49		
	P9.3	—	50		
	PA.0	—	63	I/O	
	PA.1	—	64		
	PA.2	—	1		
	PA.3	—	2		

Table 2 shows the secondary functions of each pin of the ML63512A/63514A.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin		Type	Description
		TB	TP		
External Interrupt	P0.0/INT0	37	51	I	External 0 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.1/INT1	38	52	I	External 1 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.2/INT2	39	53	I	External 2 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.3/INT3	40	54	I	External 3 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
Capture	P1.0/TM0CAP	41	55	I	Timer 0 (TM0) capture trigger input pin.
	P1.1/TM1CAP	42	56	I	Timer 1 (TM1) capture trigger input pin.
Timer	P1.0/TM0OVF	41	55	O	Timer 0 (TM0) overflow flag output pin.
	P1.1/TM1OVF	42	56	O	Timer 1 (TM1) overflow flag output pin.
	P1.2/T0CK	43	57	I	Timer 0 (TM0) external clock input pin.
	P1.3/T1CK	44	58	I	Timer 1 (TM1) external clock input pin.
Oscillation Output	P2.0/TBCCLK	45	59	O	Low-speed oscillation clock output pin.
	P2.1/HSCLK	46	60	O	High-speed oscillation clock output pin.
Serial Port	P3.0/RXD	1	3	I	Serial port receive data input pin.
	P3.1/TXC	2	4	I/O	Sync serial port clock input-output pin. Transmit sync clock input-output pin when a serial port is used synchronously. Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	P3.2/RXC	3	5	I/O	Sync serial port clock input-output pin. Receive sync clock input-output pin when a serial port is used synchronously. Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	P3.3/TXD	4	6	O	Serial port transmit data output pin.
Comparator	P7.0/CMPIN	13	19	I	Comparator analog input pin.
	P7.1/CMPREF	14	20	I	Comparator reference voltage input pin.
Level Detector	P7.2/LDIN0	15	21	I	Level detector analog input pin.
	P7.3/LDIN1	16	22	I	Level detector analog input pin.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD}	Ta = 25°C	–0.3 to +5.8	V
Power Supply Voltage 2	V_{DDI}	Ta = 25°C	–0.3 to +5.8	V
Power Supply Voltage 3	V_{DDH}	Ta = 25°C	–0.3 to +5.8	V
Power Supply Voltage 4	V_{DDL}	Ta = 25°C	–0.3 to +5.8	V
Input Voltage 1	V_{IN1}	V_{DD} Input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} Input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD} Output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DDI} Output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DDH} Output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C
Power Dissipation	P_D	Ta = 25°C	60	mW

RECOMMENDED OPERATING CONDITIONS

• When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	0.9 to 1.8	V
	V_{DDI}	—	0.9 to 3.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 80	kHz
Low-Speed RC Oscillator Frequency	f_{CRL}	R_{CRL} = 1 MΩ ±10%	32	kHz
External High-Speed RC Oscillator Resistance	R_{CRH}	V_{DD} = 0.9 to 1.8 V	100 to 300	kΩ

• When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	1.8 to 3.5	V
		When Level detector and Comparator are not used	1.8 to 5.5	
	V_{DDI}	—	1.8 to 5.5	
Crystal Oscillation Frequency	f_{XT}	—	30 to 80	kHz
Low-Speed RC Oscillator Frequency	f_{CRL}	R_{CRL} = 1 MΩ ±10%	32	kHz
External High-Speed RC Oscillator Resistance	R_{CRH}	V_{DD} = 1.8 to 5.5 V	15 to 300	kΩ
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 2.2 to 5.5 V	300k to 1M	Hz
		V_{DD} = 2.7 to 5.5 V	200k to 2M	

ELECTRICAL CHARACTERISTICS

DC Characteristics

• When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state High-speed oscillation stop Level detector stop	Ta = 25°C	4.8	5.3	5.8	µA	1
			Ta = –20 to +50°C	—	5.3	9.0		
			Ta = –20 to +70°C	—	5.3	15.0		
Supply Current 2	I_{DD2}	CPU operating High-speed oscillation stop Level detector stop	Ta = 25°C	12.0	13.0	14.0	µA	
			Ta = –20 to +50°C	—	13.0	16.0		
			Ta = –20 to +70°C	—	13.0	24.0		
Supply Current 3	I_{DD3}	CPU operating at low speed High-speed oscillation stop Level detector active (for a soft duty of about 3%)		—	10.0	35.0	µA	
Supply Current 4	I_{DD4}	CPU operating at high speed High-speed RC oscillation R_{CRH} = 100 kΩ		—	550.0	750.0	µA	

• When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state High-speed oscillation stop Level detector stop	Ta = 25°C	2.1	2.4	2.7	µA	1
			Ta = –20 to +50°C	—	2.4	7.0		
			Ta = –20 to +70°C	—	2.4	10.0		
Supply Current 2	I_{DD2}	CPU operating High-speed oscillation stop Level detector stop	Ta = 25°C	5.0	6.0	7.0	µA	
			Ta = –20 to +50°C	—	6.0	9.0		
			Ta = –20 to +70°C	—	6.0	15.0		
Supply Current 3	I_{DD3}	CPU operating at low speed High-speed oscillation stop Level detector active (for a soft duty of about 3%)		—	6.0	25.0	µA	
Supply Current 4	I_{DD4}	CPU operating at high speed High-speed RC oscillation R_{CRH} = 100 kΩ		—	410.0	550.0	µA	
Supply Current 5	I_{DD5}	CPU operating at high speed High-speed ceramic oscillation (ceramic oscillation, 2 MHz)		—	850.0	1000.0	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDH} Voltage	V_{DDH}	High-speed clock stop V_{DD} = 1.5 V	2.8	—	3.0	V	1
		High-speed clock oscillation (RC oscillation, R_{CRH} = 100 kΩ)	2.0	—	—	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock stop	1.0	1.5	2.0	V	
		High-speed clock oscillation	2.0	—	2.7	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.2	—	—	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	—	0.9	—	—	V	
External Crystal Oscillator Capacitance	C_G	—	5.0	—	25.0	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20.0	25.0	30.0	pF	
Internal Low-Speed RC Oscillator Capacitance	C_{XT}	—	10.0	15.0	20.0	pF	
Internal High-Speed RC Oscillator Capacitance	C_{OS}	—	8.0	12.0	16.0	pF	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	C_{IN}	—	—	—	5.0	pF	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P6.0 to P6.3) (P9.0 to P9.3) (PA.0 to PA.3) (MD)	I_{OH1}	V_{OH1} = V_{DD} – 0.5 V	V_{DD} = 1.5 V	–2.5	–1.3	–0.2	mA	2
			V_{DD} = 3.0 V	–6.0	–3.5	–1.0	mA	
			V_{DD} = 5.0 V	–8.5	–5.0	–1.5	mA	
	I_{OL1}	V_{OL1} = 0.5 V	V_{DD} = 1.5 V	0.2	1.3	2.5	mA	
			V_{DD} = 3.0 V	1.0	3.0	6.0	mA	
			V_{DD} = 5.0 V	1.5	3.7	8.5	mA	
Output Current 2 (P8.0 to P8.3)	I_{OH2Z}	V_{OH2} = V_{DD}		—	—	1.0	µA	
	I_{OL2}	V_{OL2} = 0.5 V	V_{DDI} = 1.5 V	3.0	7.5	14.0	mA	
			V_{DDI} = 3.0 V	6.0	12.0	20.0	mA	
			V_{DDI} = 5.0 V	8.0	15.0	28.0	mA	
Output Current 3 (OSC1)	I_{OH3R}	V_{OH3R} = V_{DDH} – 0.5 V	V_{DD} = V_{DDH} = 3.0 V	–2.5	–1.5	–0.2	mA	
			V_{DD} = V_{DDH} = 5.0 V	–3.5	–1.8	–0.5	mA	
	I_{OL3R}	V_{OL3R} = 0.5 V	V_{DD} = V_{DDH} = 3.0 V	0.2	1.5	2.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	0.5	1.8	3.5	mA	
	I_{OH3C}	V_{OH3C} = V_{DDH} – 0.5 V	V_{DD} = V_{DDH} = 3.0 V	–300	–160	–60	µA	
			V_{DD} = V_{DDH} = 5.0 V	–400	–240	–100	µA	
	I_{OL3C}	V_{OL3C} = 0.5 V	V_{DD} = V_{DDH} = 3.0 V	60	170	300	µA	
			V_{DD} = V_{DDH} = 5.0 V	100	210	400	µA	
Output Leakage (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P6.0 to P6.3) (P8.0 to P8.3) (P9.0 to P9.3) (PA.0 to PA.3)	I_{OOH}	V_{OH} = V_{DD}		—	—	1.0	µA	
	I_{OOL}	V_{OL} = V_{SS}		–1.0	—	—	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

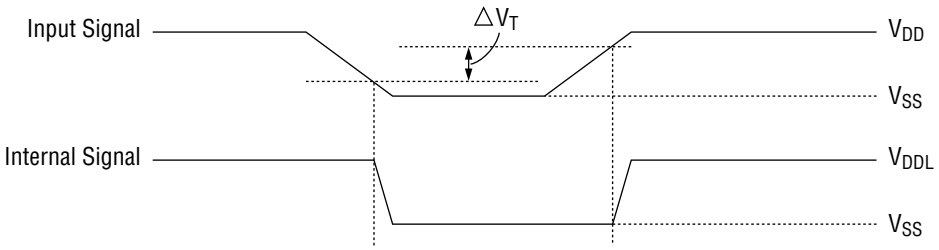
Parameter (Pin Name)	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	I_{IH1U}	V_{IH1} = V_{DD} (when pulled up)		—	—	1.0	μA	3
	I_{IL1U}	V_{IL1} = V_{SS} (when pulled up)	V_{DD} = 1.5 V	–8.0	–4.0	–1.0	μA	
			V_{DD} = 3.0 V	–60.0	–30.0	–10.0	μA	
			V_{DD} = 5.0 V	–150.0	–90.0	–23.0	μA	
	I_{IH1Z}	V_{IH1} = V_{DD} (in a high-impedance state)		—	—	1.0	μA	
	I_{IL1Z}	V_{IL1} = V_{SS} (in a high-impedance state)		–1.0	—	—	μA	
Input Current 2 (RESETB)	I_{IH2}	V_{IH2} = V_{DD}		—	—	1.0	μA	
	I_{IL2}	V_{IL2} = V_{SS} (when pulled up)	V_{DD} = 1.5 V	–45.0	–20.0	–2.0	μA	
			V_{DD} = 3.0 V	–260.0	–120.0	–30.0	μA	
			V_{DD} = 5.0 V	–870.0	–300.0	–70.0	μA	
Input Current 3 (OSC0)	I_{IL3}	V_{IL3} = V_{SS} (when pulled up)	V_{DD} = V_{DDH} = 3.0 V	–350.0	–170.0	–30.0	μA	
			V_{DD} = V_{DDH} = 5.0 V	–750.0	–450.0	–200.0	μA	
	I_{IH3R}	V_{IH3} = V_{DDH}		—	—	1.0	μA	
	I_{IL3R}	V_{IL3} = V_{SS}		–1.0	—	—	μA	
Input Current 4 (TST1B, TST2B)	I_{IH4}	V_{IH4} = V_{DD}		—	—	0.1	μA	
	I_{IL4}	V_{IL4} = V_{SS} (when pulled up)	V_{DD} = 1.5 V	–120.0	–60.0	–10.0	μA	
			V_{DD} = 3.0 V	–600.0	–350.0	–100.0	μA	
			V_{DD} = 5.0 V	–1320.0	–770.0	–220.0	μA	

DC Characteristics (continued)

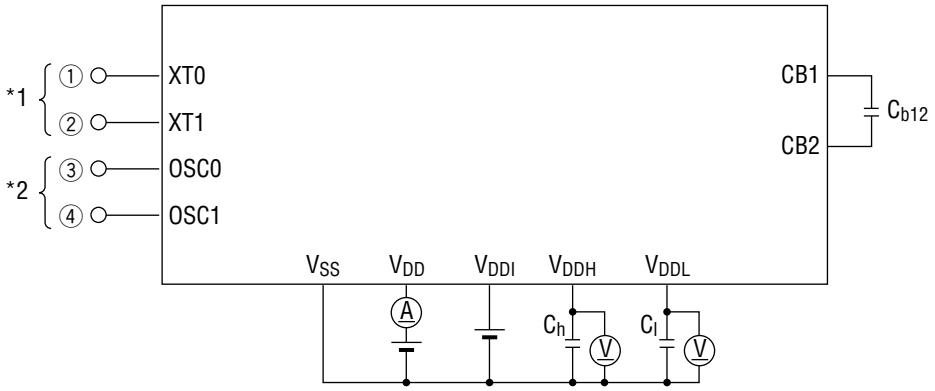
(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	V_{IH1}	V_{DD} = 1.5 V	1.2	—	1.5	V	4
		V_{DD} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = 5.0 V	4.0	—	5.0	V	
	V_{IL1}	V_{DD} = 1.5 V	0.0	—	0.3	V	
		V_{DD} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = 5.0 V	0.0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL2}	V_{DD} = V_{DDH} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Input Voltage 3 (RESETB) (TST1B, TST2B)	V_{IH3}	V_{DD} = 1.5 V	1.35	—	1.50	V	
		V_{DD} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = 5.0 V	4.0	—	5.0	V	
	V_{IL3}	V_{DD} = 1.5 V	0.00	—	0.15	V	
		V_{DD} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = 5.0 V	0.0	—	1.0	V	
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3) (RESETB) (TST1B, TST2B)	$\triangle V_T$	V_{DD} = 1.5 V	0.05	0.10	0.30	V	
		V_{DD} = 3.0 V	0.2	0.5	1.0	V	
		V_{DD} = 5.0 V	0.25	1.00	1.50	V	

Hysteresis width



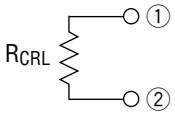
Measuring circuit 1



C_G : 15 pF
C_{b12}, C_h : 1 μF
C_I : 0.1 μF
C_O : 12 pF
Ceramic Resonator : CSA2.00MG (2 MHz)
CSB1000J (1 MHz)
(Murata MFG.-make)
C_{L0} : 30 pF
C_{L1} : 30 pF

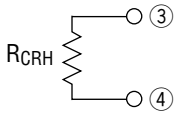
*1

RC oscillator

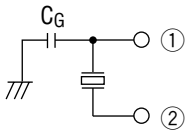


*2

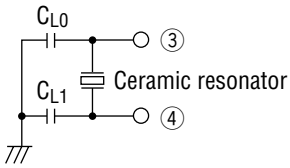
RC oscillator



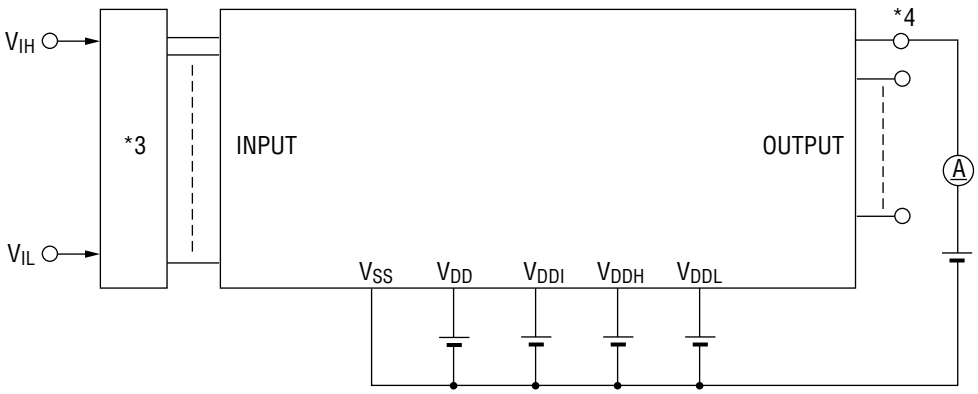
Crystal oscillator



Ceramic oscillator

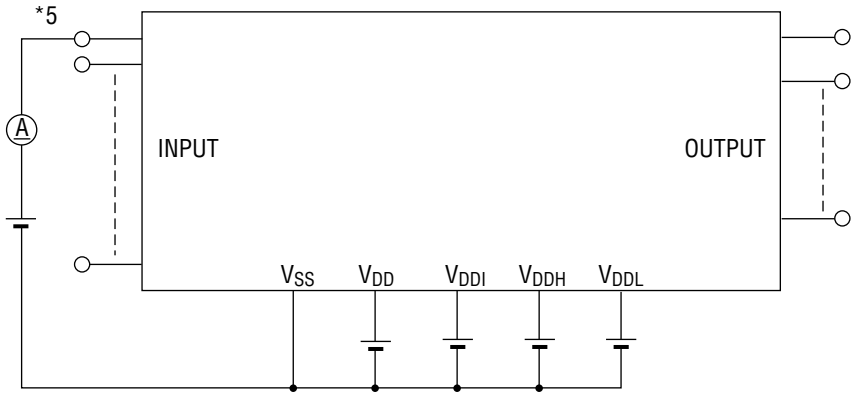


Measuring circuit 2

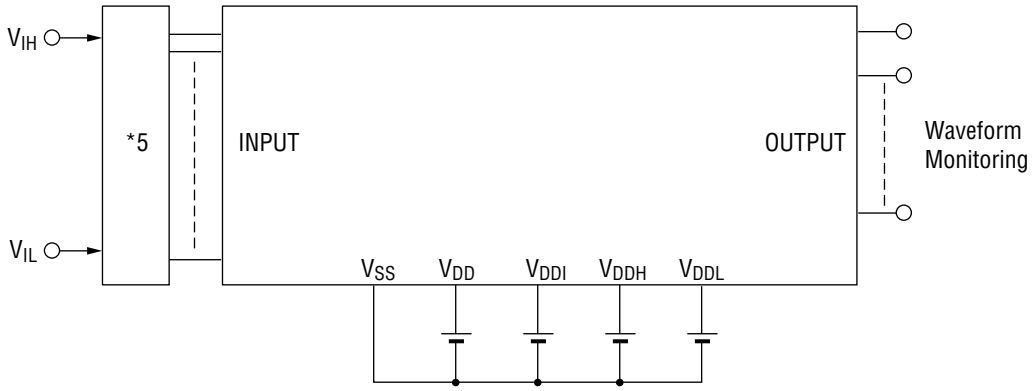


*3 Input logic circuit to determine the specified measuring conditions.
*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

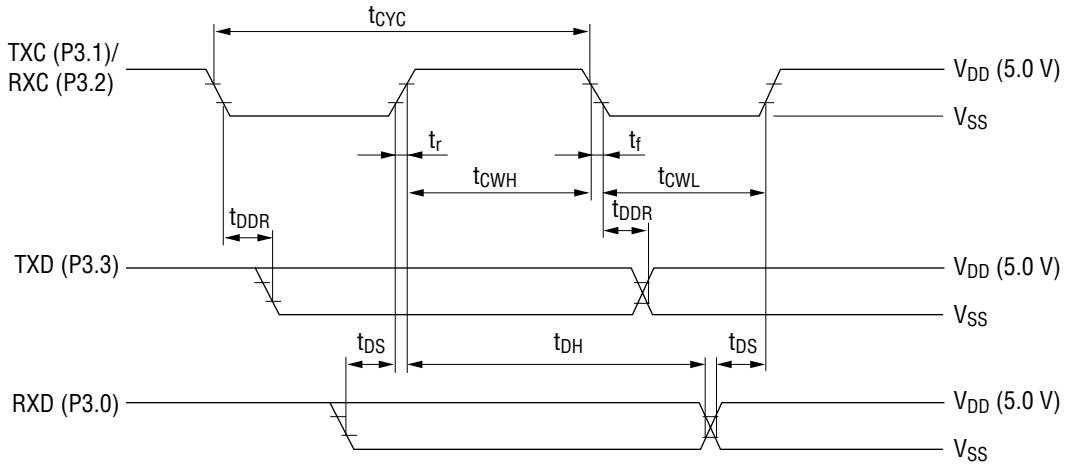
AC Characteristics (Serial Interface, Serial Port)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 0.9 to 5.5 V, Ta = –20 to +70°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$t_{CYC1(O)}$	CPU operating at 32.768 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU operating at 2 MHz V_{DD} = V_{DDH} = 2.7 to 5.5 V	—	0.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous communication timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT}-T_{CR}$	T_{BRT}	$T_{BRT}+T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT}\times0.97$	R_{BRT}	$R_{BRT}\times1.03$	s

f_{BRT}: Baud rates (2TBCCLK, TBCCLK, 1/2TBCCLK, Timer 0/1 overflow)

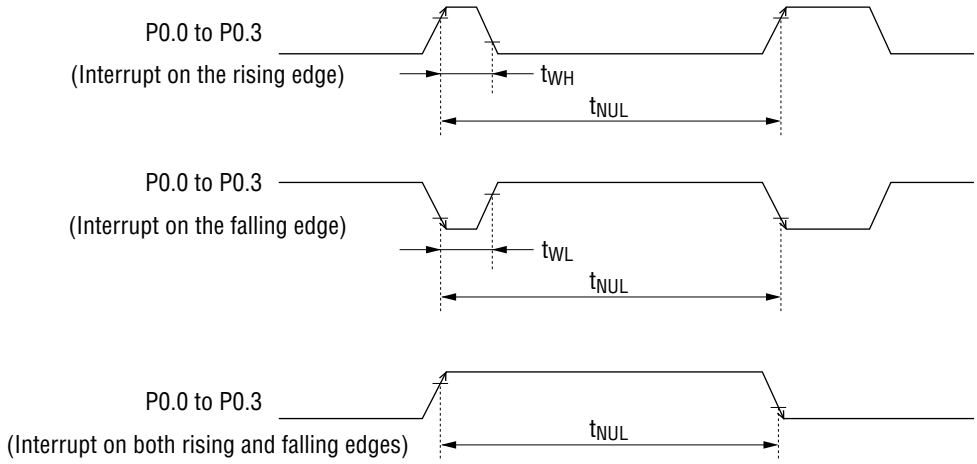
UART communication timing
("H" level = 4.0 V, "L" level = 1.0 V)

AC Characteristics

(V_{DD} = V_{DDI} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to + 70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External Interrupt Enable Pulse Width (Rising Edge)	t_{WH}	—	20	—	—	ns
External Interrupt Enable Pulse Width (Falling Edge)	t_{WL}	—	20	—	—	ns
External Interrupt Disable Time	t_{NUL}	Interrupt enable, MIE = 1 CPU operating under the NOP instruction System clock: 32.768 kHz	13.0	—	65.1	µs

AC characteristics timing



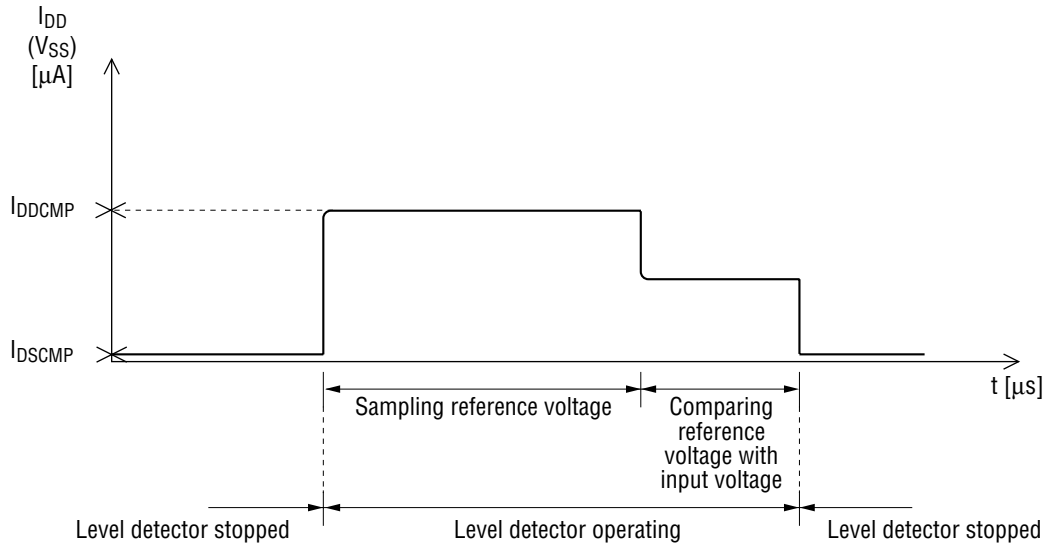
Comparator Electrical Characteristics

(V_{DD} = 0.9 V, V_{SS} = 0 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Comparator Offset Voltage	V_{coff}	—	—	—	30	mV	CMPIN CMPREF
Comparator Input Voltage	V_{cin}	—	V_{SS}	—	V_{DD}	V	
Comparator Conversion Time	T_C	System clock: 32.768 kHz	—	183	—	µs	
Comparator Supply Current	I_{DDCMP}	Comparator operating	—	30	90	µA	
	I_{DSCMP}	Comparator stopped	—	—	0.1	µA	

Conceptual diagram of comparator supply current

The conceptual diagram of the comparator supply current I_{DDCMP} and I_{DSCMP} is shown below.



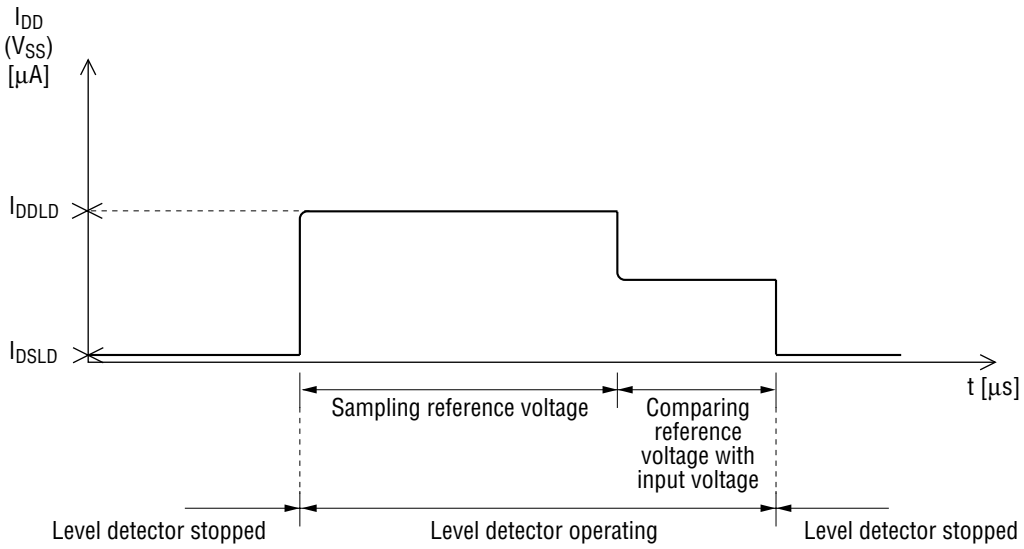
Level Detector Electrical Characteristics

(V_{DD} = 0.9 V, V_{SS} = 0 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Level Detector Input Voltage	V_{LD}	—	V_{SS}	—	V_{DD}	V	LDIN0, 1
Level Detector Conversion Time	T_C	System clock: 32.768 kHz	—	183	—	µs	
Level Dtector Supply Current	I_{DDLD}	Level detector operating	—	80	130	µA	
	I_{DSLD}	Level detector stopped	—	—	0.1	µA	

Conceptual diagram of level detector supply current

The conceptual diagram of the level detector supply current I_{DDLD} and I_{DSLD} is shown below.



Level Detector Input Levels and Output Codes

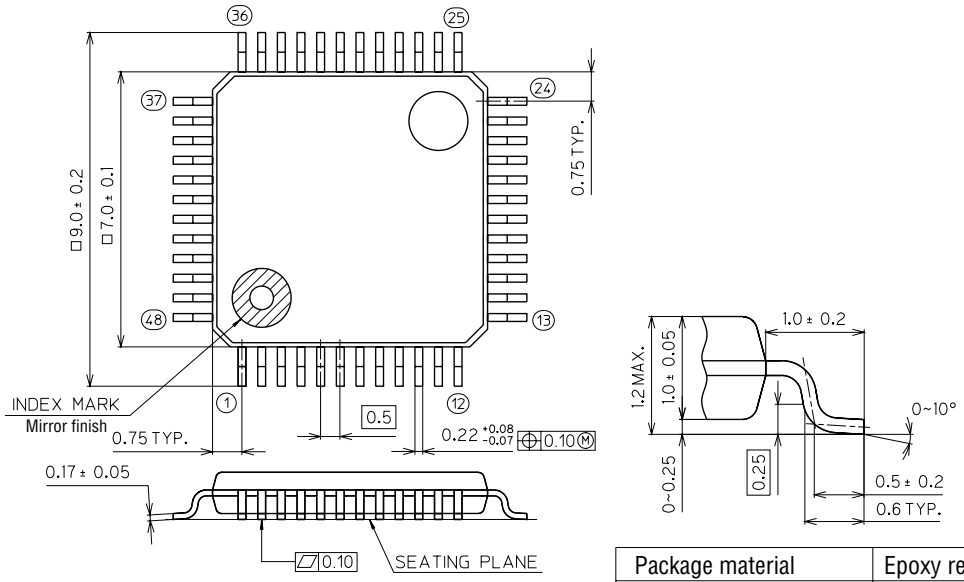
(V_{DD} = 0.9 to 1.8 V: when backup is used, V_{DD} = 1.8 to 3.5 V: when backup is not used; V_{SS} = 0 V, Ta = –20 to +70°C)

Input Level [V]		Level Detector	LDOUT			
Min.	Max.	Operation State	bit 3	bit 2	bit 1	bit 0
$1440/1500 \times V_{DD}$	V_{DD}	OFF state	1	1	1	1
$1306/1500 \times V_{DD}$	$1366/1500 \times V_{DD}$	ON state	1	0	1	1
$1190/1500 \times V_{DD}$	$1250/1500 \times V_{DD}$		1	0	1	0
$1074/1500 \times V_{DD}$	$1134/1500 \times V_{DD}$		1	0	0	1
$958/1500 \times V_{DD}$	$1018/1500 \times V_{DD}$		1	0	0	0
$842/1500 \times V_{DD}$	$902/1500 \times V_{DD}$		0	1	1	1
$726/1500 \times V_{DD}$	$786/1500 \times V_{DD}$		0	1	1	0
$610/1500 \times V_{DD}$	$670/1500 \times V_{DD}$		0	1	0	1
$494/1500 \times V_{DD}$	$554/1500 \times V_{DD}$		0	1	0	0
$378/1500 \times V_{DD}$	$438/1500 \times V_{DD}$		0	0	1	1
$262/1500 \times V_{DD}$	$322/1500 \times V_{DD}$		0	0	1	0
$146/1500 \times V_{DD}$	$206/1500 \times V_{DD}$		0	0	0	1
V_{SS}	$88/1500 \times V_{DD}$		0	0	0	0

PACKAGE DIMENSIONS

(Unit : mm)

TQFP48-P-0707-0.50-K



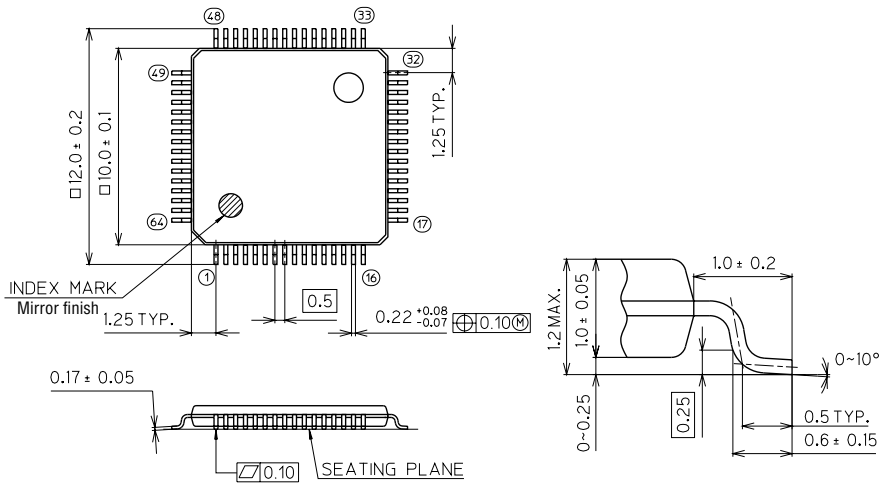
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.13 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TQFP64-P-1010-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.26 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.