1.5-Gbps LVDS/LVPECL/CML-TO-CML TRANSLATOR/REPEATER

FEATURES

- **Provides Level Translation From LVDS or LVPECL to CML, Repeating From CML to CML**
- **Signaling Rates(1) up to 1.5 Gbps**
- **CML Compatible Output Directly Drives Devices With 3.3-V, 2.5-V, or 1.8-V Supplies**
- **Total Jitter < 70 ps**
- **Low 100 ps (Max) Part-To-Part Skew**
- **Wide Common-Mode Receiver Capability Allows Direct Coupling of Input Signals**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Propagation Delay Times, 800 ps Maximum**
- **3.3-V Supply Operation**
- **Available in SOIC and MSOP Packages**

APPLICATIONS

- **Level Translation**
- **622-MHz Central Office Clock Distribution**
- **High-Speed Network Routing**
- **Wireless Basestations**
- **Low Jitter Clock Repeater**(1)

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

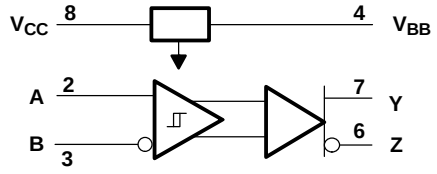
DESCRIPTION

This high-speed translator/repeater is designed for signaling rates up to 1.5 Gbps to support various high-speed network routing applications. The driver output is compatible with current-mode logic (CML) levels, and directly drives 50-Ω or 25-Ω loads connected to 1.8-V, 2.5-V, or 3.3-V nominal supplies. The capability for direct connection to the loads may eliminate the need for coupling capacitors. The receiver input is compatible with LVDS (TIA/EIA-644), LVPECL, and CML signaling levels. The receiver tolerates a wide common-mode voltage range, and may also be directly coupled to the signal source. The internal data path from input to output is fully differential for low noise generation and low pulse-width distortion.

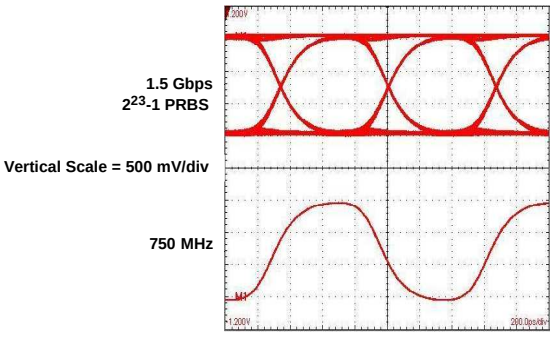
The V_{BB} pin is an internally generated voltage supply to allow operation with a single-ended LVPECL input. For single-ended LVPECL input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. When used, decouple V_{BB} with a 0.01-µF capacitor and limit the current sourcing or sinking to 400 µA. When not used, V_{BB} should be left open.

This device is characterized for operation from –40°C to 85°C.

FUNCTIONAL DIAGRAM



EYE PATTERN



V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 3.3 V, R_T = 50 Ω

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002–TBD, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	STATUS
SN65CML100D	CML100	SOIC	Production
SN65CML100DGK	NWB	MSOP	Production

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

				UNIT
V_{CC}	Supply voltage range(2)			–0.5 V to 4 V
I_{BB}	Sink/source			±0.5 mA
	Voltage range, (A, B, Y, Z)			0 V to 4.3 V
	Electrostatic discharge	Human Body Model (3)	A, B, Y, Z, and GND	±5 kV
			All pins	±2 kV
		Charged-Device Model(4)	All pins	±1500 V
	Continuous power dissipation			See Dissipation Rating Table
T_{stg}	Storage temperature range			–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{TT}	Terminator supply voltage	3.3-V nominal supply at terminator	3	3.3	3.6	V
		2.5-V nominal supply at terminator	2.375	2.5	2.625	
		1.8-V nominal supply at terminator	1.7		1.9	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		1	V
	Input voltage (any combination of common-mode or input signals)		0		4	V
V_{BB}	Output current				400	µA
T_A	Operating free-air temperature		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGK	425 mW	3.4 mW/°C	221 mW
D	725 mW	5.8 mW/°C	377 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

DEVICE CHARACTERISTICS

PARAMETER		MIN	NOM	MAX	UNIT
I_{CC}	Supply current, device only		9	12	mA
V_{BB}	Switching reference voltage (1)	1890	1950	2010	mV

(1) V_{BB} parameter varies 1:1 with V_{CC}

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$			25		mV
I_I	Input current (A or B inputs)	V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_I = 4 V, Second input at 1.2 V			33	
$I_{I(OFF)}$	Power off input current (A or B inputs)	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_{CC} = 1.5 V, V_I = 4 V, Second input at 1.2 V			33	
I_{IO}	Input offset current ($\lvert I_{IA} - I_{IB} \rvert$)	$V_{IA} = V_{IB}$, $0 \le V_{IA} \le 4$ V	–6		6	µA
C_i	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{OH}	Output high voltage (2)	R_T = 50 Ω, V_{TT} = 3 V to 3.6 V or V_{TT} = 2.5 V ±5%, See Figure 2	V_{TT}–60	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage (2)		V_{TT}–1100	V_{TT}–800	V_{TT}–640	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		640	780	1000	mV
V_{OH}	Output high voltage (3)	R_T = 25 Ω, V_{TT} = 3 V to 3.6 V or V_{TT} = 2.5 V ±5%, See Figure 2	V_{TT}–60	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage (3)		V_{TT}–550	V_{TT}–400	V_{TT}–320	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		320	390	500	mV
V_{OH}	Output high voltage (2)	R_T = 50 Ω, V_{TT} = 1.8 V ±5%, See Figure 2	V_{TT}–170	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage (2)		V_{TT}–1100	V_{TT}–800	V_{TT}–640	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		570	780	1000	mV
V_{OH}	Output high voltage (3)	R_T = 25 Ω, V_{TT} = 1.8 V ±5%, See Figure 2	V_{TT}–85	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage (3)		V_{TT}–500	V_{TT}–400	V_{TT}–320	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		285	390	500	mV
C_o	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Outputs are terminated through 50-Ω resistors to V_{TT}, CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT}.
(3) Outputs are terminated through 25-Ω resistors to V_{TT}; CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT}.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_T = 50 Ω or R_T = 25 Ω, SeeFigure 4	250		800	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		800	ps
t_r	Differential output signal rise time (20%–80%)				300	ps
t_f	Differential output signal fall time (20%–80%)				300	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)(2)			0	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)	V_{ID} = 0.2 V			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5)		1	5	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak)(4)	750 MHz clock input(6)		8	27	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	1.5 Gbps 2^{23}-1 PRBS input(7)		30	70	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^7–1 PRBS input(8)		25	65	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL}.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devicesoperate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter parameters are ensured by design and characterization. Measurements are made with a Tektronix TDS6604 oscilloscope runningTektronix TDSJIT3 software. Agilent E4862B stimulus system jitter 2 ps $t_{jit(per)}$, 16 ps $t_{jit(cc)}$, 25 ps $t_{jit(pp)}$, and 10 ps $t_{jit(det)}$ has beensubtracted from the values.
(5) V_{ID} = 200 mV, 50% duty cycle, V_{IC} = 1.2 V, $t_r = t_f \leq 25$ ns (20% to 80%), measured over 1000 samples.
(6) V_{ID} = 200 mV, 50% duty cycle, V_{IC} = 1.2 V, $t_r = t_f \leq 25$ ns (20% to 80%).
(7) V_{ID} = 200 mV, V_{IC} = 1.2 V, $t_r = t_f \leq 0.25$ ns (20% to 80%), measured over 100k samples.
(8) V_{ID} = 200 mV, V_{IC} = 1.2 V, $t_r = t_f \leq 0.25$ ns (20% to 80%). Deterministic jitter is sum of pattern dependent jitter and pulse width distortion.

PARAMETER MEASUREMENT INFORMATION

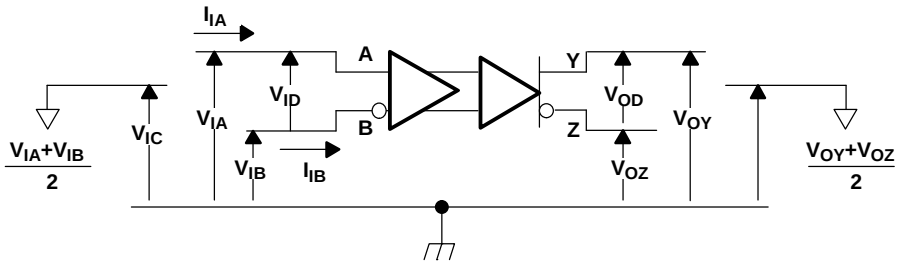


Figure 1. Voltage and Current Definitions

Table 1. Maximum Receiver Input Voltage Threshold

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.5 V	H
0.0 V	0.1 V	–100 mV	0.5 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level

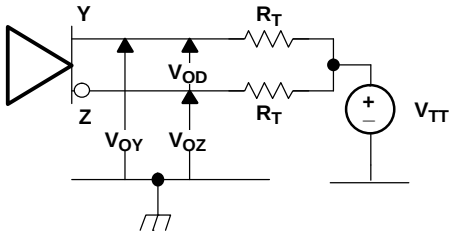


Figure 2. Output Voltage Test Circuit

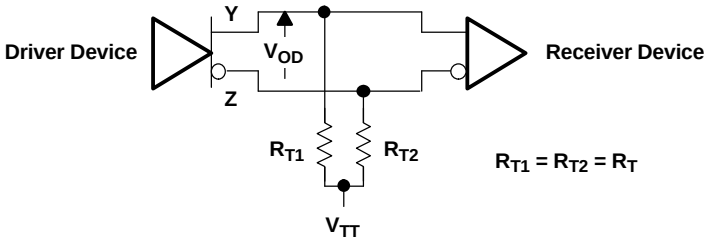
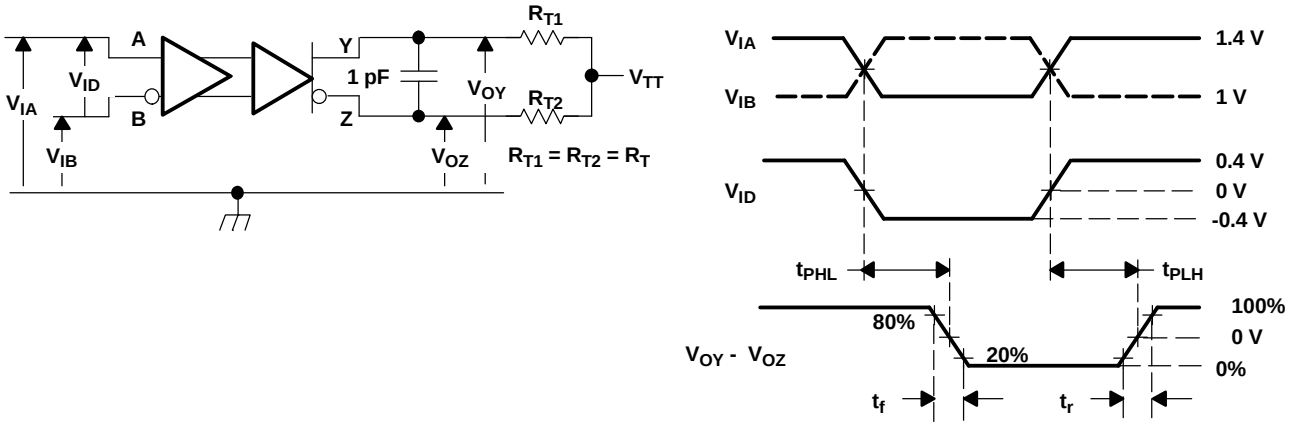


Figure 3. Typical Termination for Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 4. Timing Test Circuit and Waveforms

PIN ASSIGNMENTS

D AND DGK PACKAGE
(TOP VIEW)

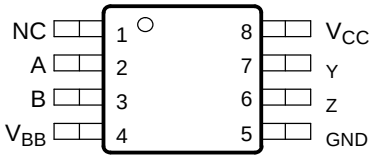


Table 2. PIN DESCRIPTIONS

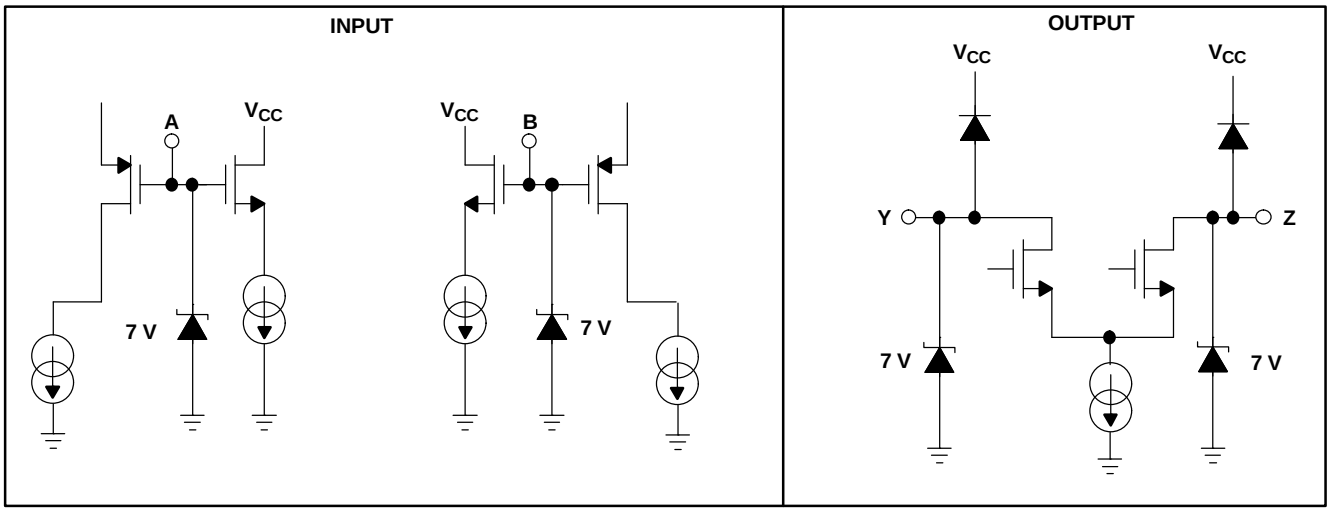
PIN	FUNCTION
A, B	Differential inputs
Y, Z	Differential outputs
V_{BB}	Reference voltage output
V_{CC}	Power supply
GND	Ground
NC	No connect

Table 3. FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS(1)	
$V_{ID} = V_A – V_B$	Y	Z
$V_{ID} \geq 100$ mV	H	L
–100 mV < V_{ID} < 100 mV	?	?
$V_{ID} \leq$ –100 mV	L	H
Open	?	?

(1) H = high level, L = low level, ? = intermediate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

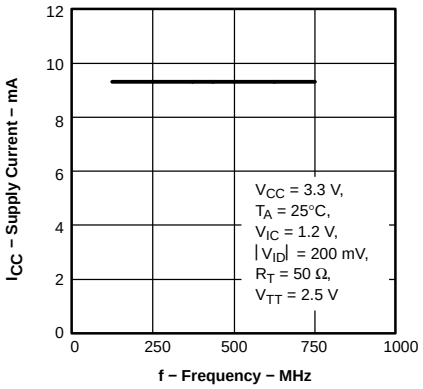


Figure 5.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

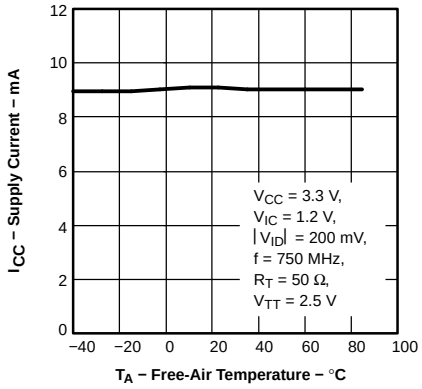


Figure 6.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

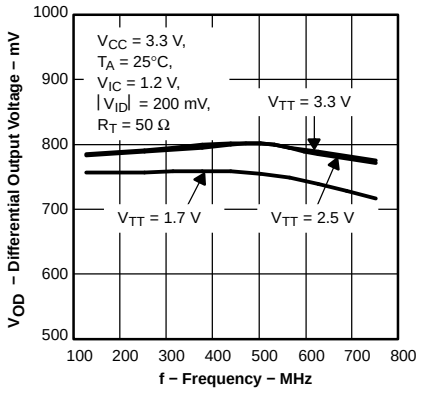


Figure 7.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

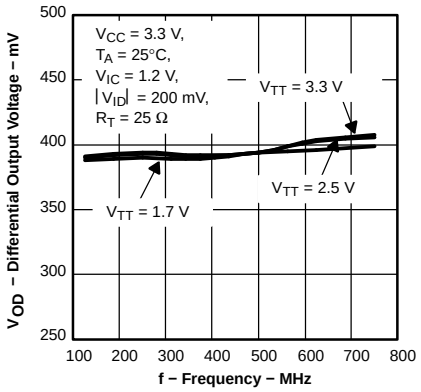


Figure 8.

PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

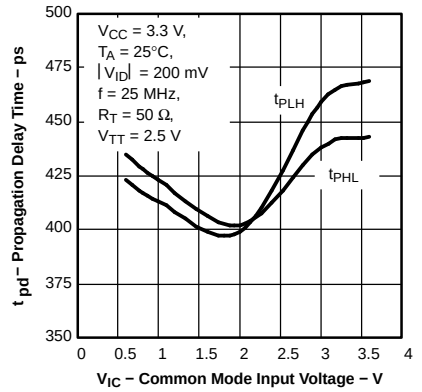


Figure 9.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

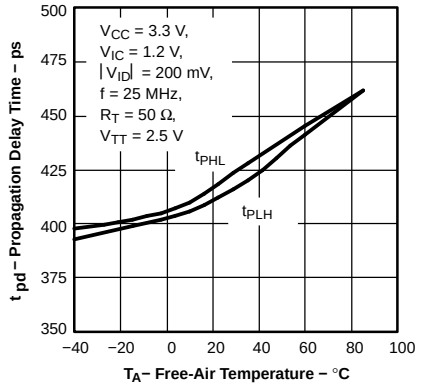


Figure 10.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

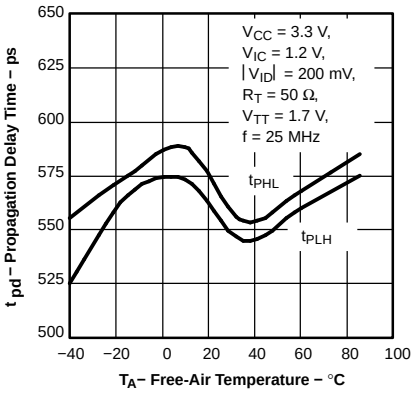


Figure 11.

PEAK-TO-PEAK JITTER vs FREQUENCY

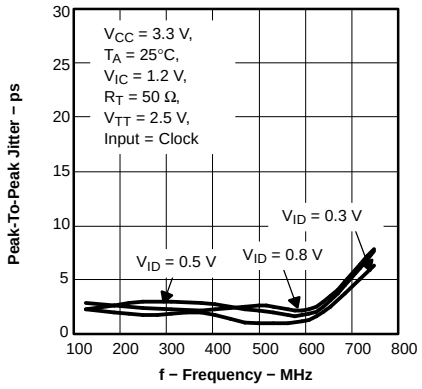


Figure 12.

PEAK-TO-PEAK JITTER vs DATA RATE

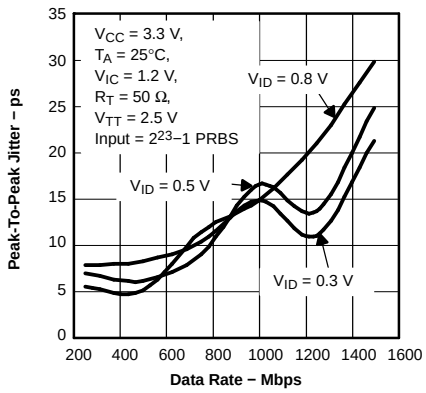


Figure 13.

PEAK-TO-PEAK JITTER vs COMMON MODE INPUT VOLTAGE

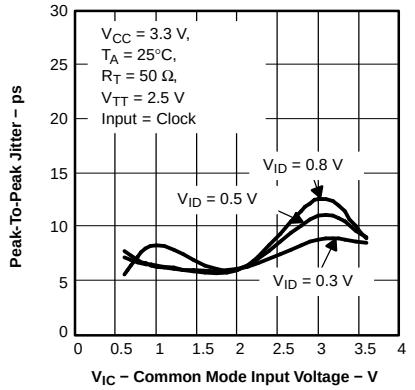


Figure 14.

PEAK-TO-PEAK JITTER vs COMMON MODE INPUT VOLTAGE

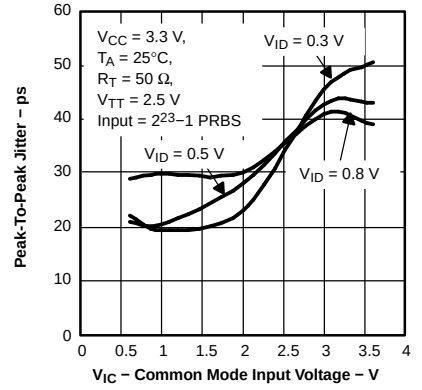


Figure 15.

PEAK-TO-PEAK JITTER vs DATA RATE

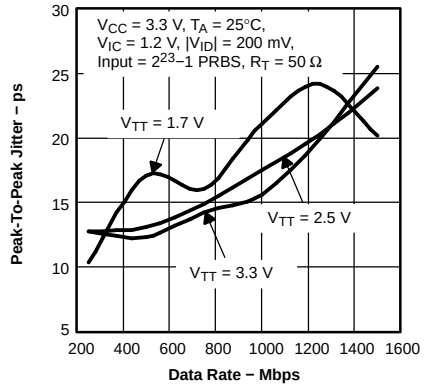


Figure 16.

PEAK-TO-PEAK JITTER vs DATA RATE

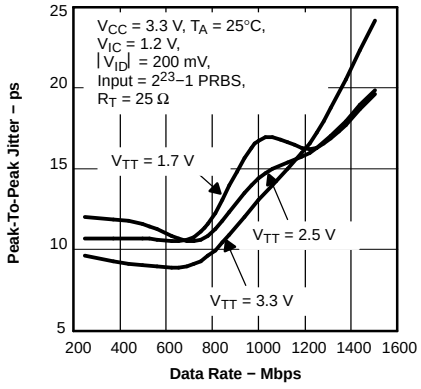
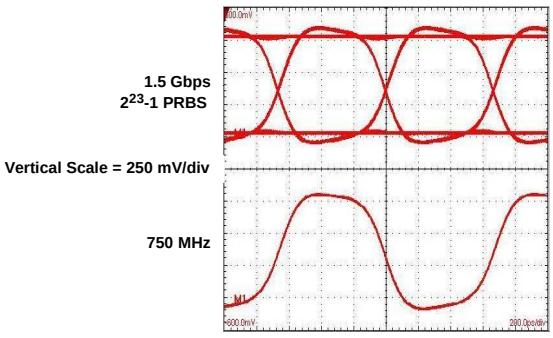


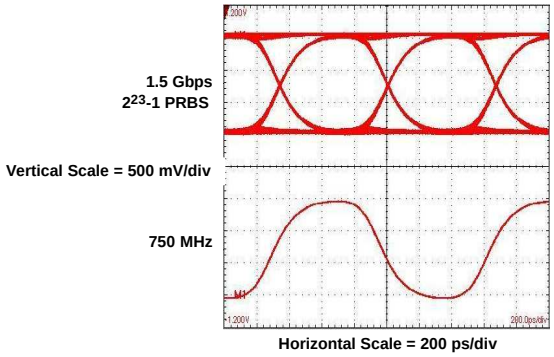
Figure 17.



V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 3.3 V, R_T = 25 Ω

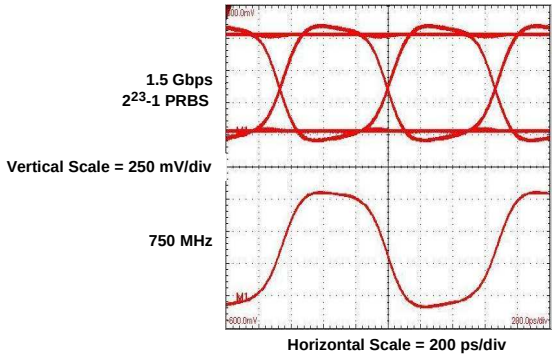
Figure 18.

TYPICAL CHARACTERISTICS (continued)



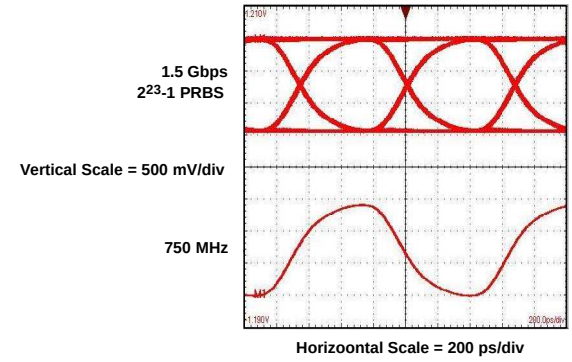
V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 2.5 V, R_T = 50 Ω

Figure 19.



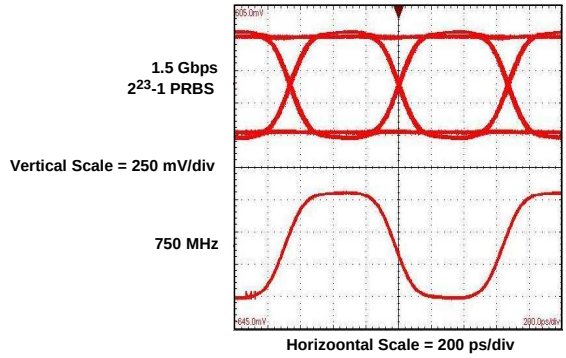
V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 2.5 V, R_T = 25 Ω

Figure 20.



V_{CC} = 3.3 V, T_A = 25°C, V_{IC} = 1.2 V, $|V_{ID}|$ = 200 mV, V_{TT} = 1.7 V, R_T = 50 Ω

Figure 21.



V_{CC} = 3.3 V, T_A = 25°C, V_{IC} = 1.2 V, $|V_{ID}|$ = 200 mV, V_{TT} = 1.7 V, R_T = 25 Ω

Figure 22.

TYPICAL CHARACTERISTICS (continued)

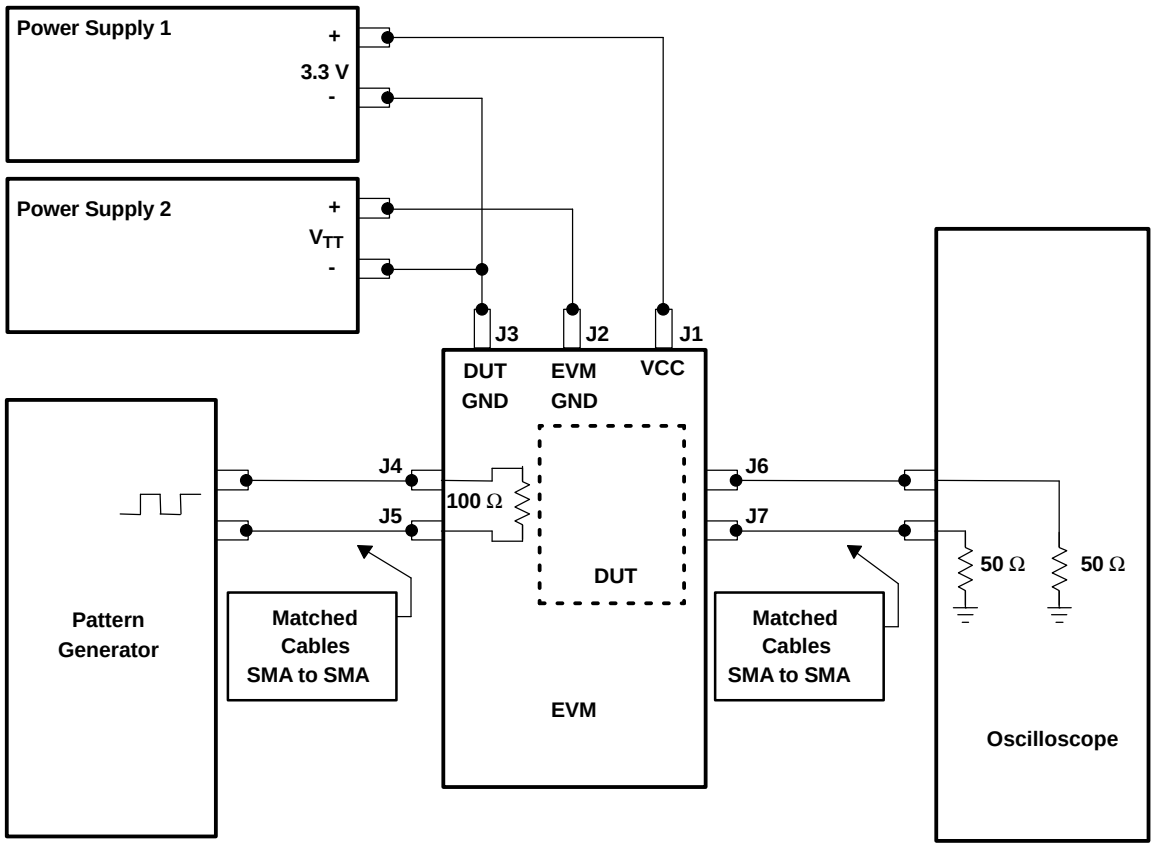


Figure 23. Jitter Setup Connections for SN65CML100

APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. When V_{BB} is used, decouple V_{BB} via a 0.01-µF capacitor and limit the current sourcing or sinking to 0.4 mA. When not used, V_{BB} should be left open.

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

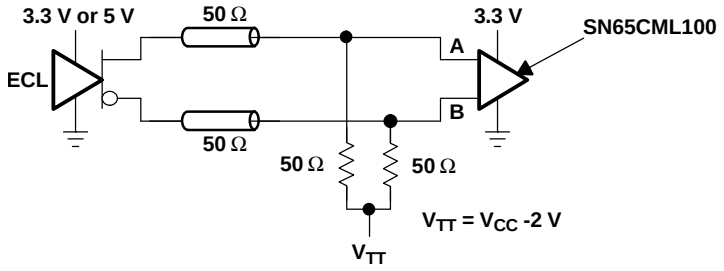


Figure 24. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

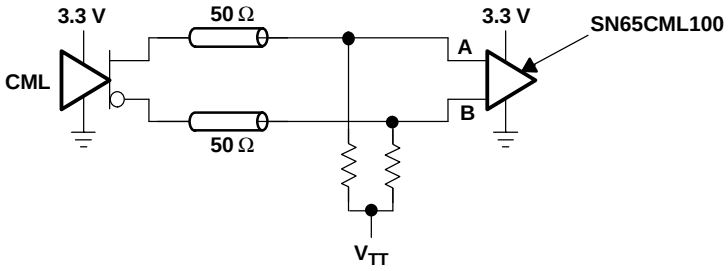


Figure 25. Current-Mode Logic (CML)

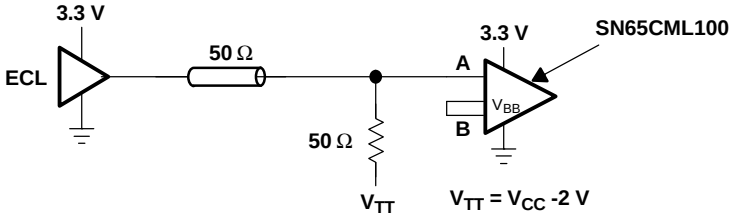


Figure 26. Single-Ended (LVPECL)

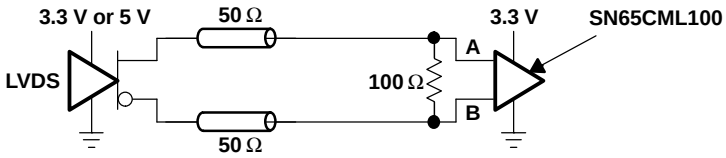


Figure 27. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65CML100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100	Samples
SN65CML100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100	Samples
SN65CML100DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB	Samples
SN65CML100DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB	Samples
SN65CML100DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB	Samples
SN65CML100DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWB	Samples
SN65CML100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100	Samples
SN65CML100DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CML100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

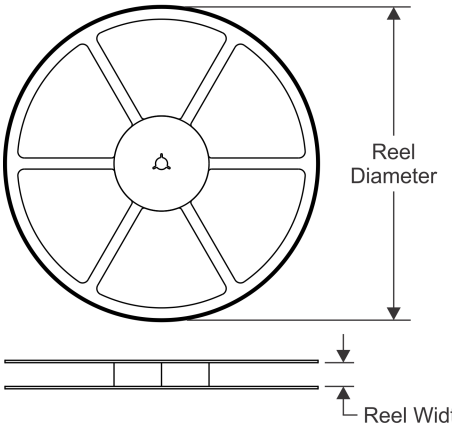
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

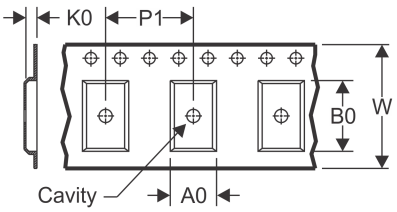
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

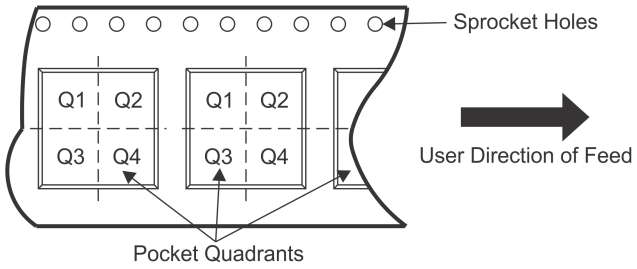


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

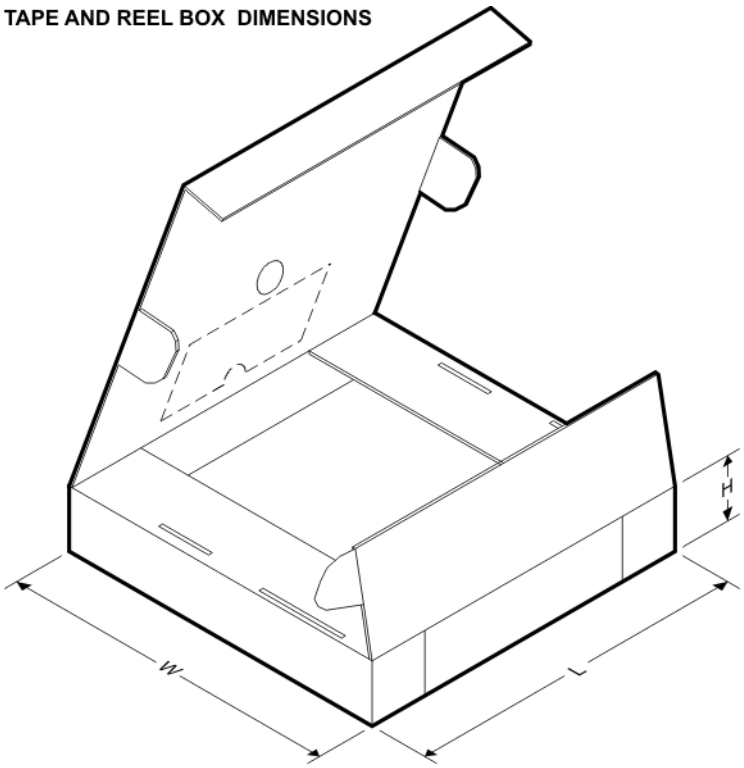
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65CML100DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65CML100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

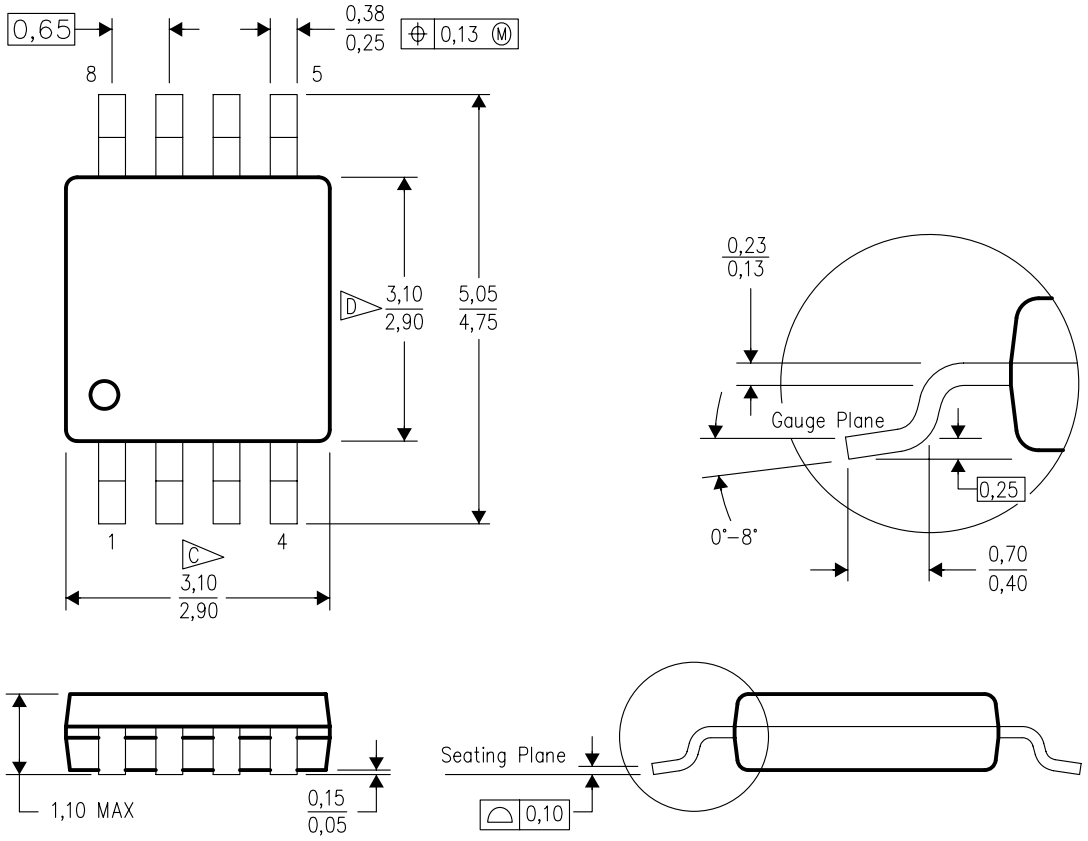
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65CML100DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65CML100DR	SOIC	D	8	2500	340.5	338.1	20.6

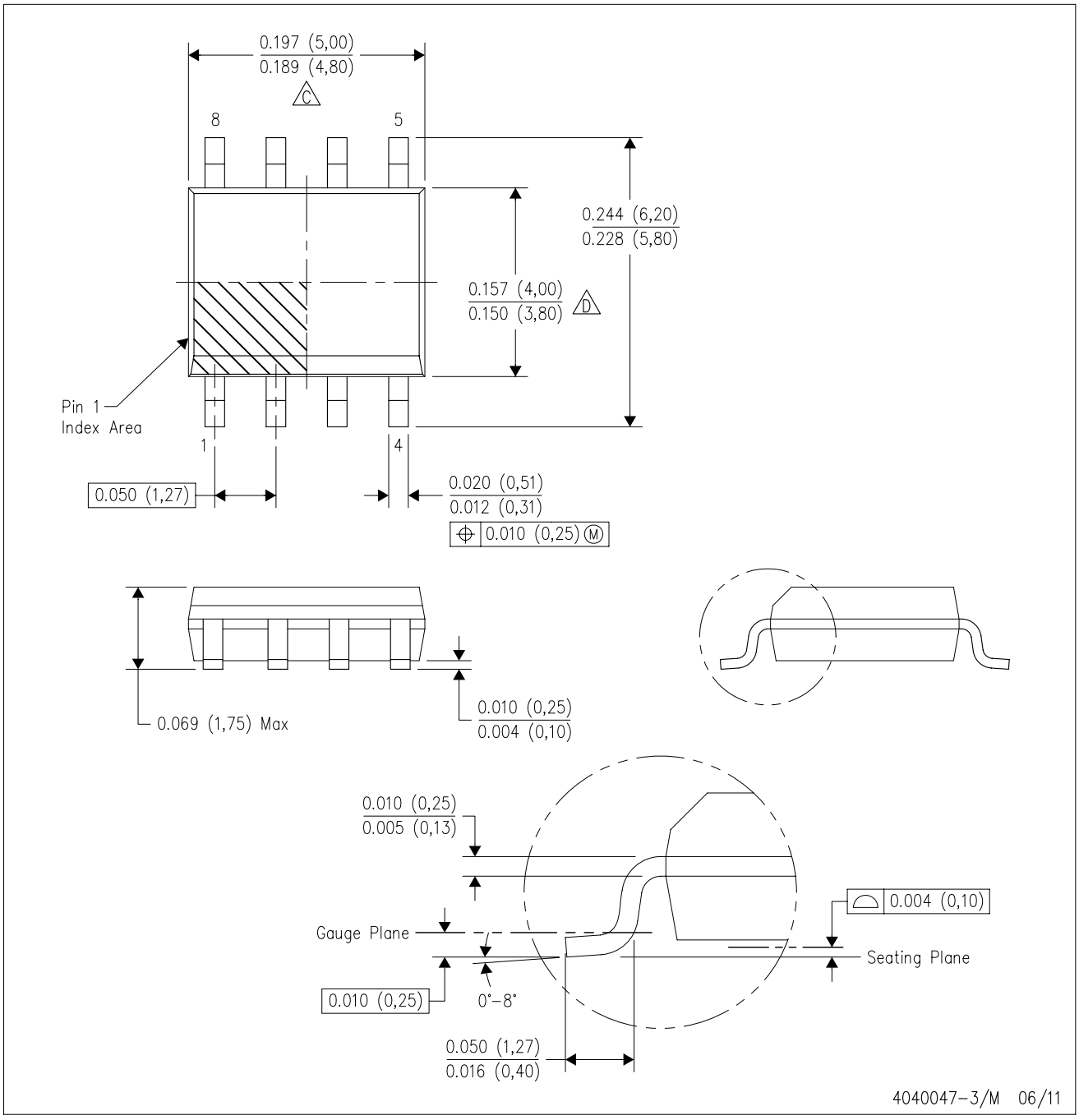
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

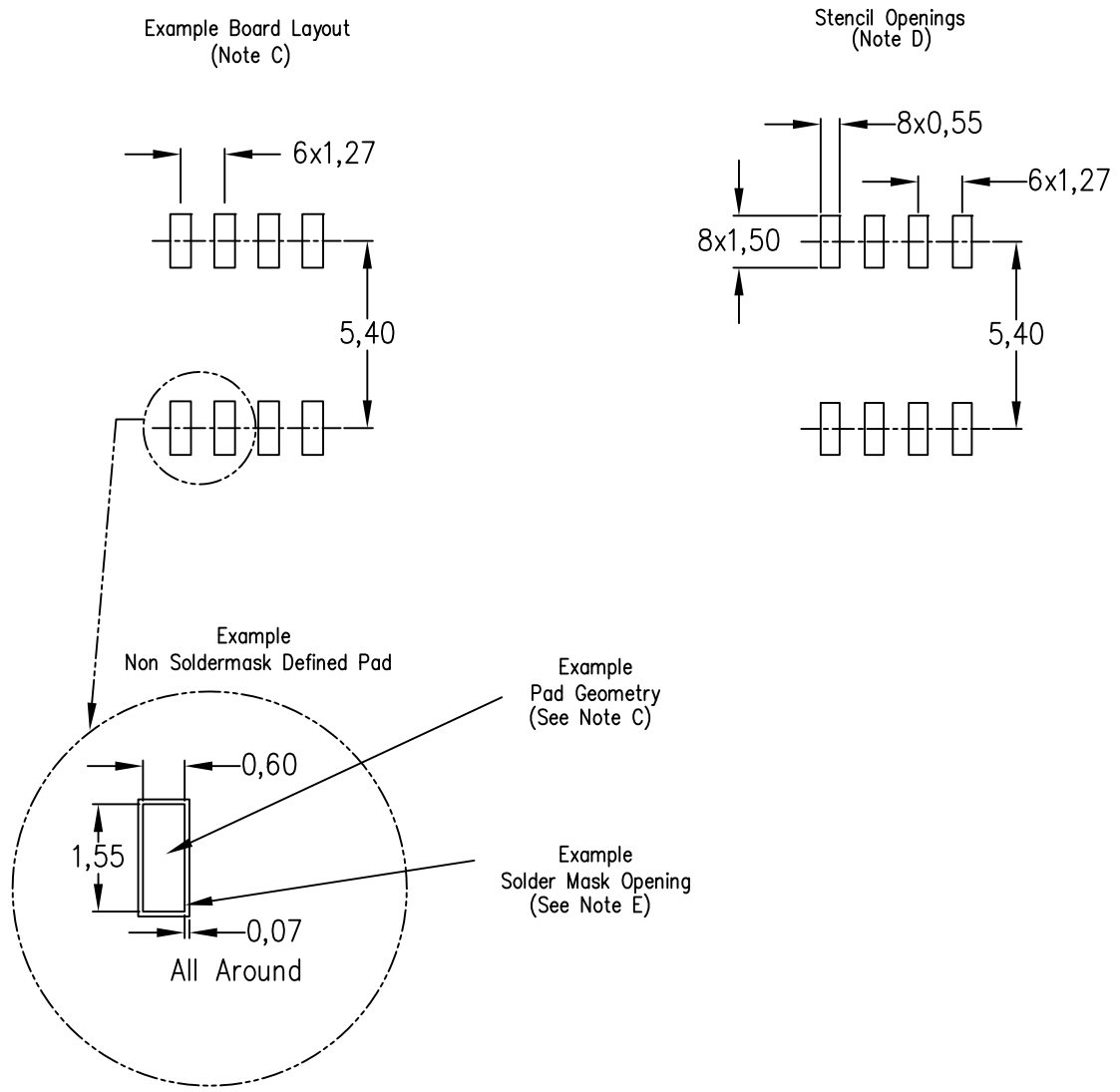
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated

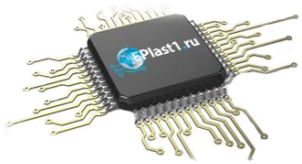
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.