Software-Selectable Multiprotocol Transceiver with Termination

FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- TUV Telecom Services Inc. Certified NET1, NET2 and TBR2 Compliant
- On-Chip Cable Termination
- **Pin Compatible with LTC1543**
- Complete DTE or DCE Port with LTC1544
- Operates from Single 5V Supply
- Small Footprint

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

DESCRIPTION

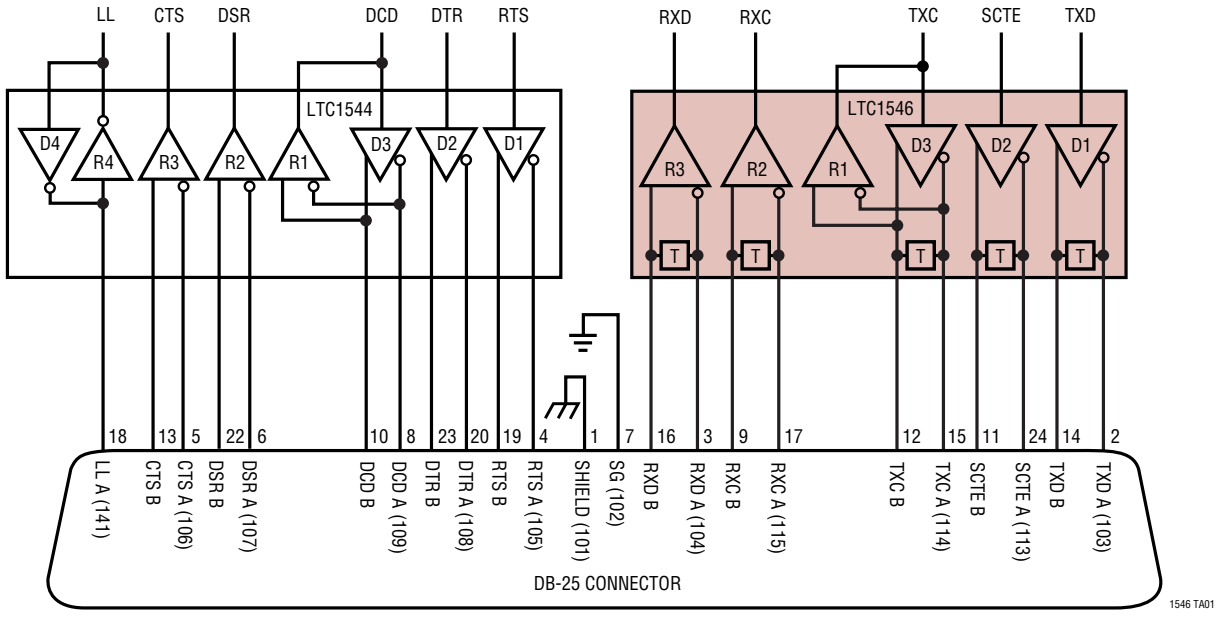
The LTC®1546 is a 3-driver/3-receiver multiprotocol transceiver with on-chip cable termination. When combined with the LTC1544, this chip set forms a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. All necessary cable termination is provided inside the LTC1546. In most applications, the LTC1546 replaces both an LTC1543 and an LTC1344A without any changes to the PC board.

The LTC1546 runs from a single 5V supply using an internal charge pump that requires only five space-saving surface mounted capacitors. The LTC1546 is available in a 28-lead SSOP surface mount package.

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TYPICAL APPLICATION

Complete DTE or DCE Multiprotocol Serial Interface with DB-25 Connector



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 6.5V

Input Voltage

Transmitters ..... –0.3V to (V_{CC} + 0.3V)

Receivers ..... –18V to 18V

Logic Pins ..... –0.3V to (V_{CC} + 0.3V)

Output Voltage

Transmitters ..... (V_{EE} – 0.3V) to (V_{DD} + 0.3V)

Receivers ..... –0.3V to (V_{CC} + 0.3V)

V_{EE} ..... –10V to 0.3V

V_{DD} ..... –0.3V to 10V

Short-Circuit Duration

Transmitter Output ..... Indefinite

Receiver Output ..... Indefinite

V_{EE} ..... 30 sec

Operating Temperature Range

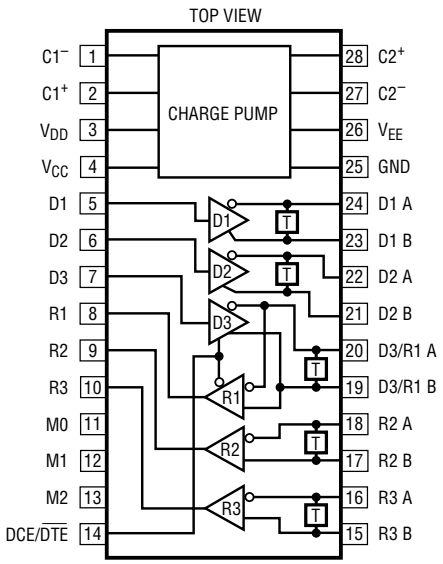
LTC1546C ..... 0°C to 70°C

LTC1546I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 90°C/W*

*θ_{JA} SOLDERED TO A CIRCUIT BOARD IS TYPICALLY 60°C/W

ORDER PART NUMBER
LTC1546CG
LTC1546IG

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, No Load			14		mA
		RS530, RS530-A, X.21 Modes, Full Load	●		100	130	mA
		V.35 Mode	●		126	170	mA
		V.28 Mode, No Load			20		mA
		V.28 Mode, Full Load	●		35	75	mA
		No-Cable Mode	●		60	500	µA
P_D	Internal Power Dissipation (DCE Mode)	RS530, RS530-A, X.21 Modes, Full Load			410		mW
		V.35 Mode, Full Load			625		mW
		V.28 Mode, Full Load			150		mW
V^+	Positive Charge Pump Output Voltage	V.11 or V.28 Mode, No Load	●	8.0	9.3		V
		V.35 Mode	●	7.0	8.0		V
		V.28 Mode, with Load	●	8.0	8.7		V
		V.28 Mode, with Load, I_{DD} = 10mA			6.5		V
V^-	Negative Charge Pump Output Voltage	V.28 Mode, No Load			–9.6		V
		V.28 Mode, Full Load	●	–7.5	–8.5		V
		V.35 Mode	●	–5.5	–6.5		V
		RS530, RS530-A, X.21 Modes, Full Load	●	–4.5	–6.0		V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{OSC}	Charge Pump Oscillator Frequency				500		kHz
t_r	Charge Pump Rise Time	No-Cable Mode/Power-Off to Normal Operation			2		ms
Logic Inputs and Outputs							
V_{IH}	Logic Input High Voltage		●	2			V
V_{IL}	Logic Input Low Voltage		●			0.8	V
I_{IN}	Logic Input Current	D1, D2, D3 M0, M1, M2, DCE = GND M0, M1, M2, DCE = V_{CC}	● ● ●	 –120 	 –75 	±10 –30 ±10	µA µA µA
V_{OH}	Output High Voltage	I_O = –3mA	●	3	4.5		V
V_{OL}	Output Low Voltage	I_O = 3mA	●		0.3	0.45	V
I_{OSR}	Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	–50		50	mA
I_{OZR}	Three-State Output Current	M0 = M1 = M2 = V_{CC}, 0V ≤ V_O ≤ V_{CC}			±1		µA
V.11 Driver							
V_{ODO}	Open Circuit Differential Output Voltage	R_L = 1.95k (Figure 1)	●			±5	V
V_{ODL}	Loaded Differential Output Voltage	R_L = 50Ω (Figure 1) R_L = 50Ω (Figure 1)	 ●	0.5V_{ODO} ±2		0.67V_{ODO}	V V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			3	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	V_{OUT} = GND				±150	mA
I_{OZ}	Output Leakage Current	$\|V_A\|$ and $\|V_B\|$ ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 2, 13)	●	2	15	25	ns
t_{PLH}	Input to Output Rising	(Figures 2, 13)	●	15	40	65	ns
t_{PHL}	Input to Output Falling	(Figures 2, 13)	●	15	40	65	ns
Δt	Input to Output Difference, $\|t_{PLH} - t_{PHL}\|$	(Figures 2, 13)	●	0	3	12	ns
t_{SKEW}	Output to Output Skew	(Figures 2, 13)			3		ns
V.11 Receiver							
V_{TH}	Input Threshold Voltage	–7V ≤ V_{CM} ≤ 7V	●	–0.2		0.2	V
ΔV_{TH}	Input Hysteresis	–7V ≤ V_{CM} ≤ 7V	●		15	40	mV
R_{IN}	Input Impedance	–7V ≤ V_{CM} ≤ 7V (Figure 3)	●	100	103		Ω
t_r, t_f	Rise or Fall Time	C_L = 50pF (Figures 4, 14)			15		ns
t_{PLH}	Input to Output Rising	C_L = 50pF (Figures 4, 14)	●		50	90	ns
t_{PHL}	Input to Output Falling	C_L = 50pF (Figures 4, 14)	●		50	90	ns
Δt	Input to Output Difference, $\|t_{PLH} - t_{PHL}\|$	C_L = 50pF (Figures 4, 14)	●	0	4	25	ns
V.35 Driver							
V_{OD}	Differential Output Voltage	Open Circuit, R_L = 1.95k (Figure 5) With Load, –4V ≤ V_{CM} ≤ 4V (Figure 6)	●	 ±0.44	 ±0.55	±1.2 ±0.66	V V
V_{OA}, V_{OB}	Single-Ended Output Voltage	Open Circuit, R_L = 1.95k (Figure 5)	●			±1.2	V
V_{OC}	Transmitter Output Offset	R_L = 50Ω (Figure 5)	●			±0.6	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OH}	Transmitter Output High Current	V_A, V_B = 0V	●	–13	–11	–9.0	mA
I_{OL}	Transmitter Output Low Current	V_A, V_B = 0V	●	9.0	11	13	mA
I_{OZ}	Transmitter Output Leakage Current	$\|V_A\|$ and $\|V_B\| \le 0.25V$	●		±1	±100	µA
R_{OD}	Transmitter Differential Mode Impedance		●	50	100	150	Ω
R_{OC}	Transmitter Common Mode Impedance	$-2V \le V_{CM} \le 2V$ (Figure 7)		135	150	165	Ω
t_r, t_f	Rise or Fall Time	(Figures 8, 13)			5		ns
t_{PLH}	Input to Output	(Figures 8, 13)	●	15	35	65	ns
t_{PHL}	Input to Output	(Figures 8, 13)	●	15	35	65	ns
Δt	Input to Output Difference, $\|t_{PLH} - t_{PHL}\|$	(Figures 8, 13)	●		0	16	ns
t_{SKEW}	Output to Output Skew	(Figures 8, 13)			4		ns
V.35 Receiver							
V_{TH}	Differential Receiver Input Threshold Voltage	$-2V \le V_{CM} \le 2V$ (Figure 9)	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$-2V \le V_{CM} \le 2V$ (Figure 9)	●		15	40	mV
R_{ID}	Receiver Differential Mode Impedance	$-2V \le V_{CM} \le 2V$	●	90	103	110	Ω
R_{IC}	Receiver Common Mode Impedance	$-2V \le V_{CM} \le 2V$ (Figure 10)		135	150	165	Ω
t_r, t_f	Rise or Fall Time	C_L = 50pF (Figures 4, 14)			15		ns
t_{PLH}	Input to Output	C_L = 50pF (Figures 4, 14)	●		50	90	ns
t_{PHL}	Input to Output	C_L = 50pF (Figures 4, 14)	●		50	90	ns
Δt	Input to Output Difference, $\|t_{PLH} - t_{PHL}\|$	C_L = 50pF (Figures 4, 14)	●	0	4	25	ns
V.28 Driver							
V_O	Output Voltage	Open Circuit R_L = 3k (Figure 11)	● ●	 ±5	 ±8.5	±10 	V V
I_{SS}	Short-Circuit Current	V_{OUT} = GND	●			±150	mA
R_{OZ}	Power-Off Resistance	$-2V < V_O < 2V$, Power Off or No-Cable Mode	●	300			Ω
SR	Slew Rate	R_L = 7k, C_L = 0 (Figures 11, 15)	●	4		30	V/µs
t_{PLH}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 11, 15)	●		1.5	2.5	µs
t_{PHL}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 11, 15)	●		1.5	2.5	µs
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage	(Figure 12)	●		1.2	0.8	V
V_{TLH}	Input High Threshold Voltage	(Figure 12)	●	2	1.2		V
ΔV_{TH}	Receiver Input Hysteresis	(Figure 12)	●	0	0.05	0.3	V
R_{IN}	Receiver Input Impedance	$-15V \le V_A \le 15V$	●	3	5	7	kΩ
t_r, t_f	Rise or Fall Time	C_L = 50pF (Figures 12, 16)			15		ns
t_{PLH}	Input to Output	C_L = 50pF (Figures 12, 16)	●		60	300	ns
t_{PHL}	Input to Output	C_L = 50pF (Figures 12, 16)	●		160	300	ns

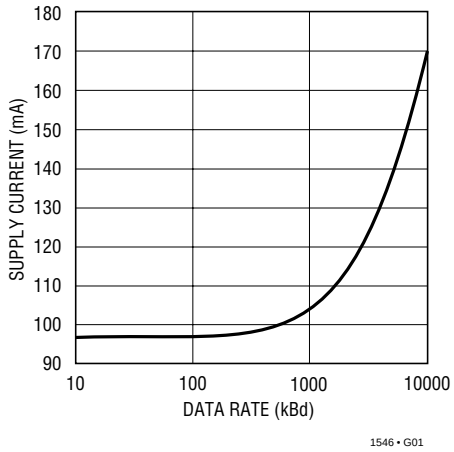
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

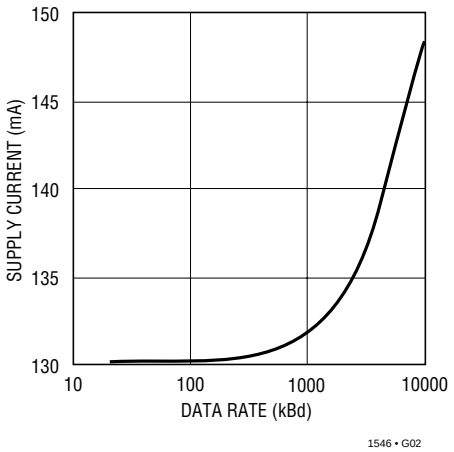
Note 3: All typicals are given for V_{CC} = 5V, C1 = C2 = C_{VCC} = C_{VDD} = 1µF, C_{VEE} = 3.3µF and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

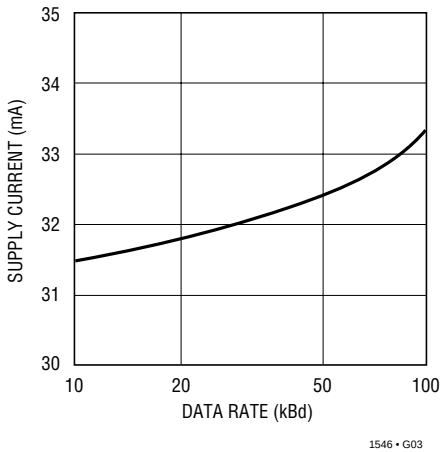
V.11 Mode
Supply Current vs Data Rate



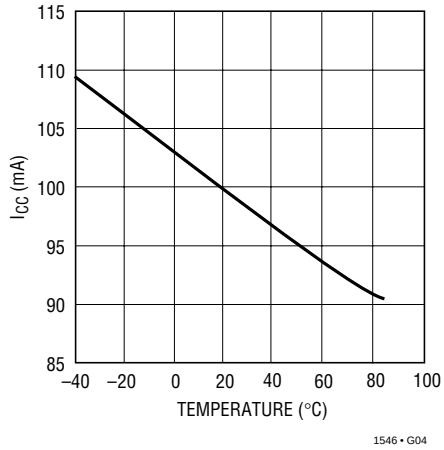
V.35 Mode
Supply Current vs Data Rate



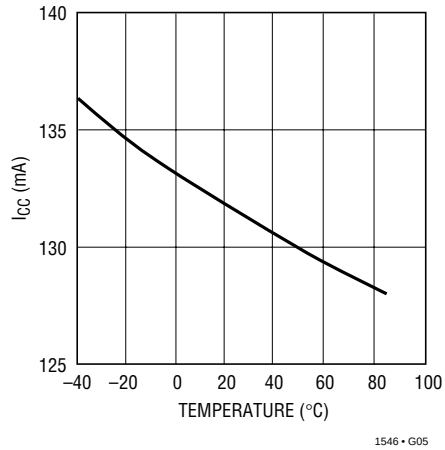
V.28 Mode
Supply Current vs Data Rate



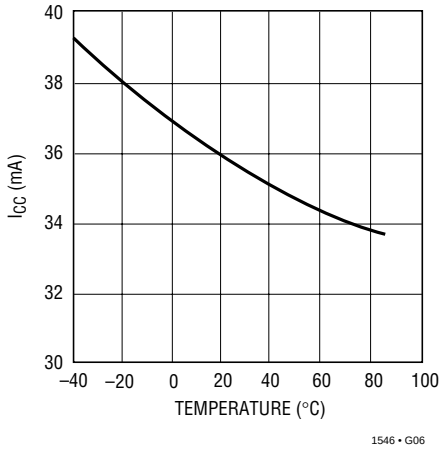
V.11 Mode
I_{CC} vs Temperature



V.35 Mode
I_{CC} vs Temperature



V.28 Mode
I_{CC} vs Temperature



PIN FUNCTIONS

$C1^-$ (Pin 1): Capacitor C1 Negative Terminal. Connect a 1µF capacitor between $C1^+$ and $C1^-$.

$C1^+$ (Pin 2): Capacitor C1 Positive Terminal. Connect a 1µF capacitor between $C1^+$ and $C1^-$.

V_{DD} (Pin 3): Generated Positive Supply Voltage for V.28. Connect a 1µF capacitor to ground.

V_{CC} (Pin 4): Positive Supply Voltage Input. $4.75V \leq V_{CC} \leq 5.25V$. Bypass with a 1µF capacitor to ground.

D1 (Pin 5): TTL Level Driver 1 Input.

D2 (Pin 6): TTL Level Driver 2 Input.

D3 (Pin 7): TTL Level Driver 3 Input.

R1 (Pin 8): CMOS Level Receiver 1 Output.

R2 (Pin 9): CMOS Level Receiver 2 Output.

R3 (Pin 10): CMOS Level Receiver 3 Output.

M0 (Pin 11): TTL Level Mode Select Input 0 with Pull-Up to V_{CC}. See Table 1.

M1 (Pin 12): TTL Level Mode Select Input 1 with Pull-Up to V_{CC}. See Table 1.

M2 (Pin 13): TTL Level Mode Select Input 2 with Pull-Up to V_{CC}. See Table 1.

$\overline{\text{DCE}}$/DTE (Pin 14): TTL Level Mode Select Input with Pull-Up to V_{CC}. See Table 1.

PIN FUNCTIONS

R3 B (Pin 15): Receiver 3 Noninverting Input.

R3 A (Pin 16): Receiver 3 Inverting Input.

R2 B (Pin 17): Receiver 2 Noninverting Input.

R2 A (Pin 18): Receiver 2 Inverting Input.

D3/R1 B (Pin 19): Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

D3/R1 A (Pin 20): Receiver 1 Inverting Input and Driver 3 Inverting Output.

D2 B (Pin 21): Driver 2 Noninverting Output.

D2 A (Pin 22): Driver 2 Inverting Output.

D1 B (Pin 23): Driver 1 Noninverting Output.

D1 A (Pin 24): Driver 1 Inverting Output.

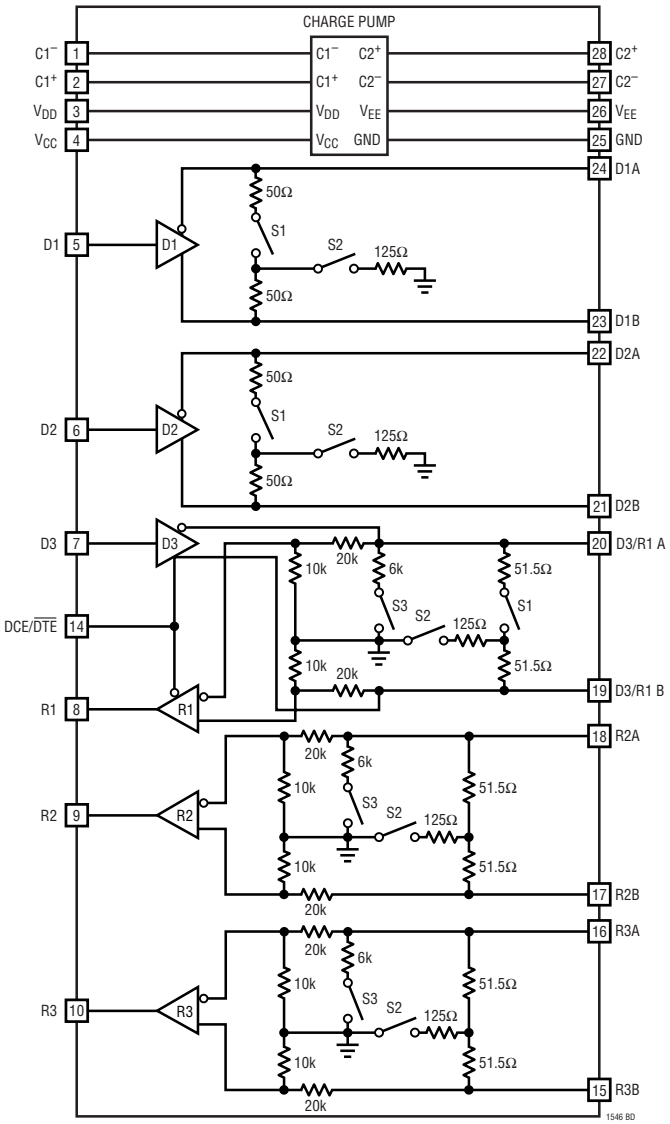
GND (Pin 25): Ground.

V_{EE} (Pin 26): Negative Supply Voltage. Connect a 3.3µF capacitor to GND.

$C2^-$ (Pin 27): Capacitor C2 Negative Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

$C2^+$ (Pin 28): Capacitor C2 Positive Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

BLOCK DIAGRAM



TEST CIRCUITS

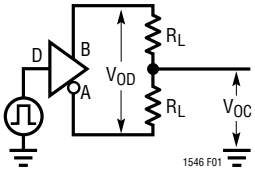


Figure 1. V.11 Driver DC Test Circuit

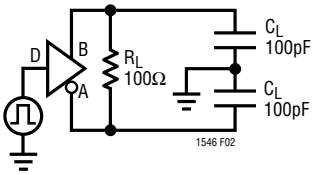


Figure 2. V.11 Driver AC Test Circuit

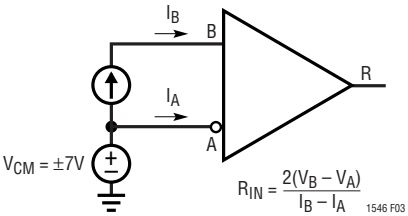


Figure 3. Input Impedance Test Circuit

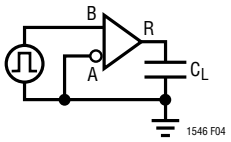


Figure 4. V.11, V.35 Receiver AC Test Circuit

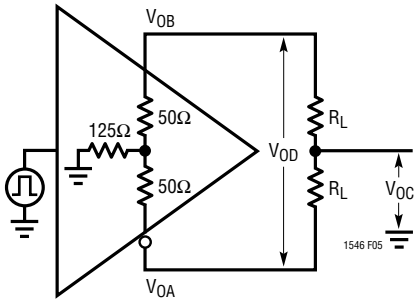


Figure 5. V.35 Driver Open-Circuit Test

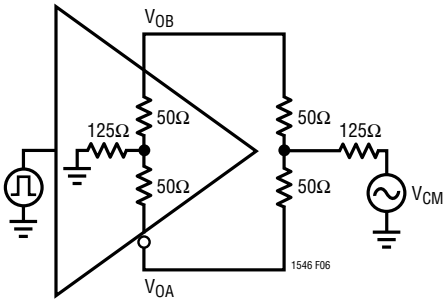


Figure 6. V.35 Driver Test Circuit

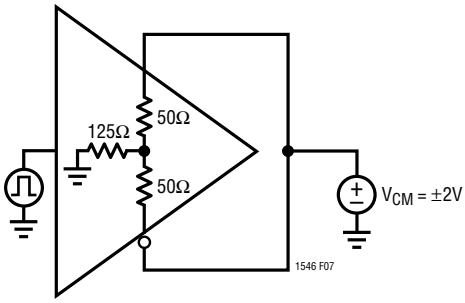


Figure 7. V.35 Driver Common Mode Impedance Test Circuit

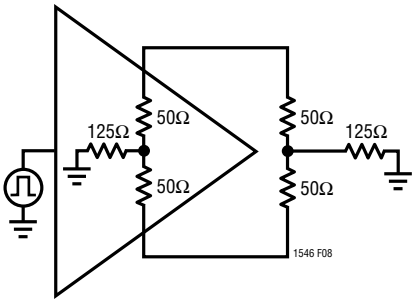


Figure 8. V.35 Driver AC Test Circuit

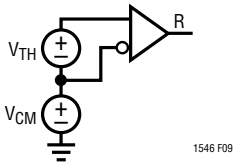


Figure 9. V.35 Receiver DC Test Circuit

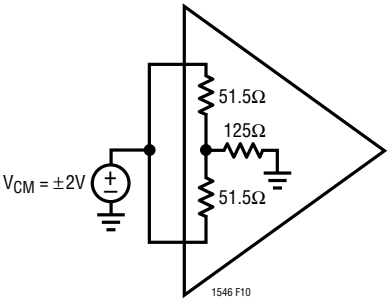


Figure 10. Receiver Common Mode Impedance Test Circuit

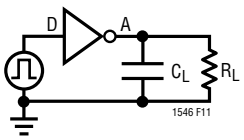


Figure 11. V.28 Driver Test Circuit

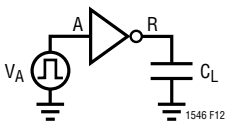


Figure 12. V.28 Receiver Test Circuit

MODE SELECTION

Table 1

LTC1546 MODE NAME	M2	M1	M0	DCE/$\overline{\text{DTE}}$	D1	D2	D3	R1	R2	R3
Not Used (Default V.11)	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No Cable	1	1	1	0	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No Cable	1	1	1	1	Z	Z	Z	Z	Z	Z

SWITCHING TIME WAVEFORMS

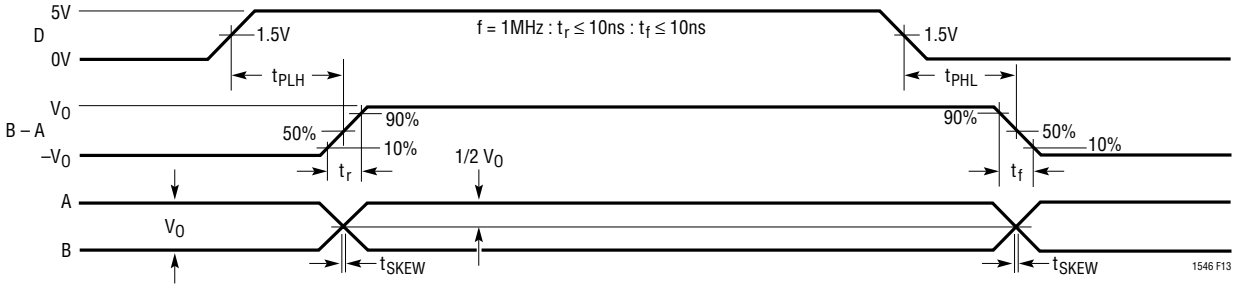


Figure 13. V.11, V.35 Driver Propagation Delays

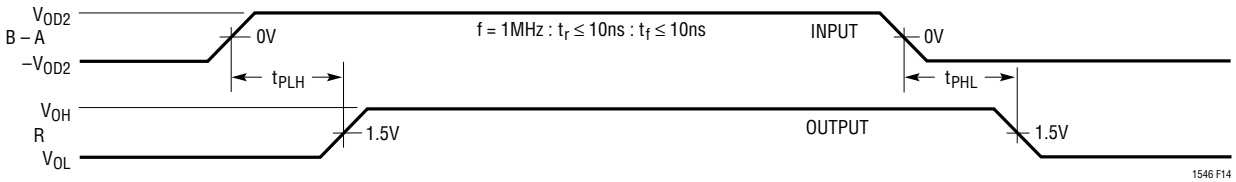


Figure 14. V.11, V.35 Receiver Propagation Delays

SWITCHING TIME WAVEFORMS

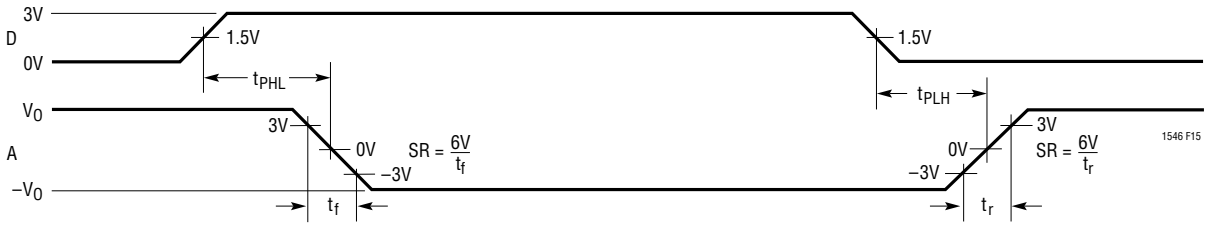


Figure 15. V.28 Driver Propagation Delays



Figure 16. V.28 Receiver Propagation Delays

APPLICATIONS INFORMATION

Overview

The LTC1546 and LTC1544 form a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. Cable termination is provided on-chip, eliminating the need for discrete termination designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 17. The LTC1546 half of each port is used to generate and appropriately terminate the clock and data signals. The LTC1544 is used to generate the control signals along with LL (Local Loopback).

Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see Table 1).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 18. The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.

When the cable is removed, leaving all mode pins unconnected, the LTC1546/LTC1544 will enter no-cable mode. In this mode the LTC1546/LTC1544 supply current drops to less than 500µA and the LTC1546/LTC1544 driver outputs are forced into a high impedance state. At the same time, the R2 and R3 receivers of the LTC1546 are differentially terminated with 103Ω and the other receivers on the LTC1546 and LTC1544 are terminated with 30kΩ to ground.

APPLICATIONS INFORMATION

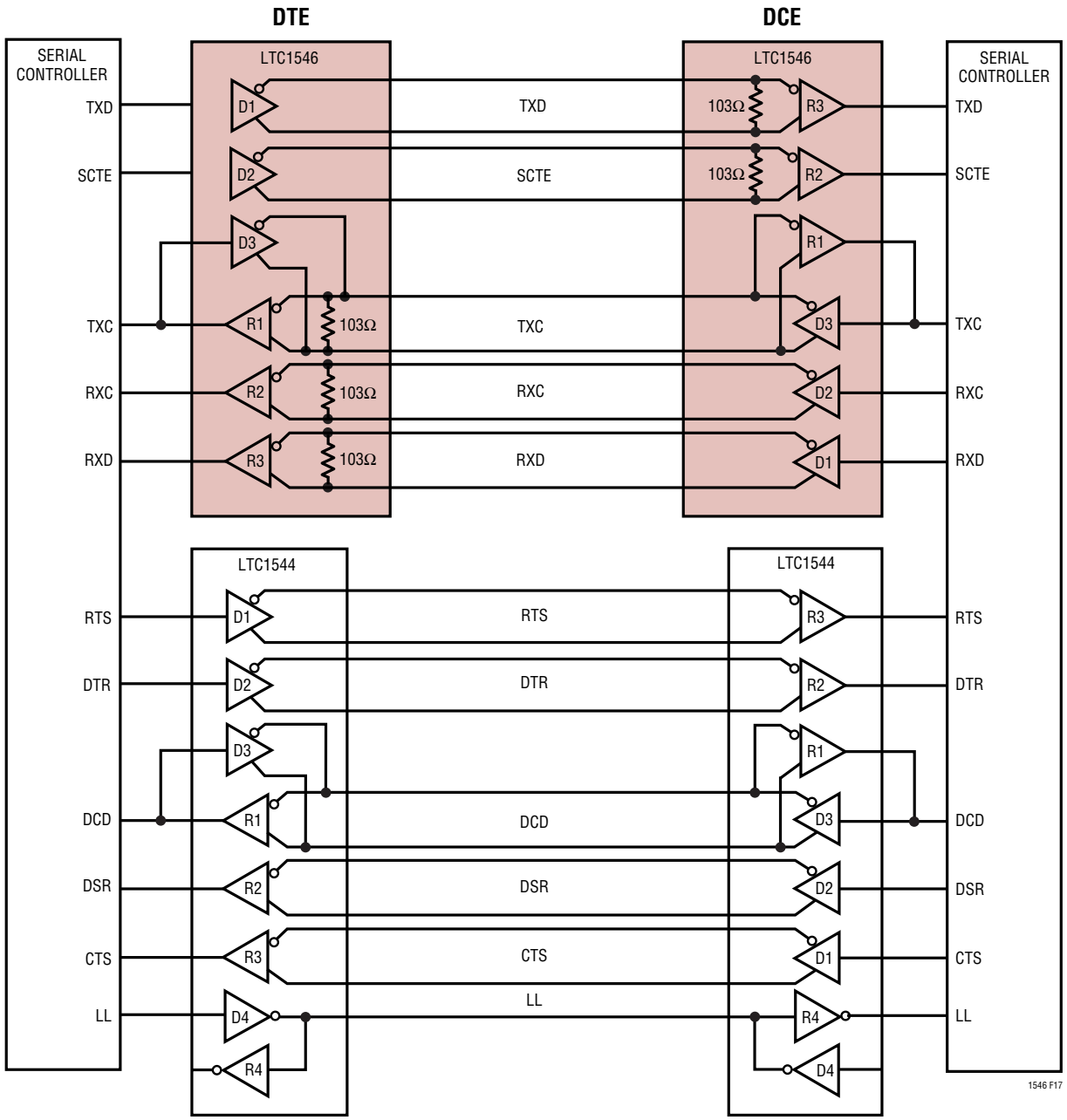


Figure 17. Complete Multiprotocol Interface in EIA530 Mode

Cable Termination

Traditional implementations used expensive relays to switch resistors or required the user to change termination modules every time a new interface standard was selected. Switching the terminations with FETs is difficult because the FETs must remain off when the signal voltage is beyond the supply voltage. Alternatively, custom cables may contain termination in the cable head or route signals to various terminations on the board.

The LTC1546/LTC1544 chipset solves the cable termination switching problem by automatically providing the appropriate termination and switching on-chip for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

APPLICATIONS INFORMATION

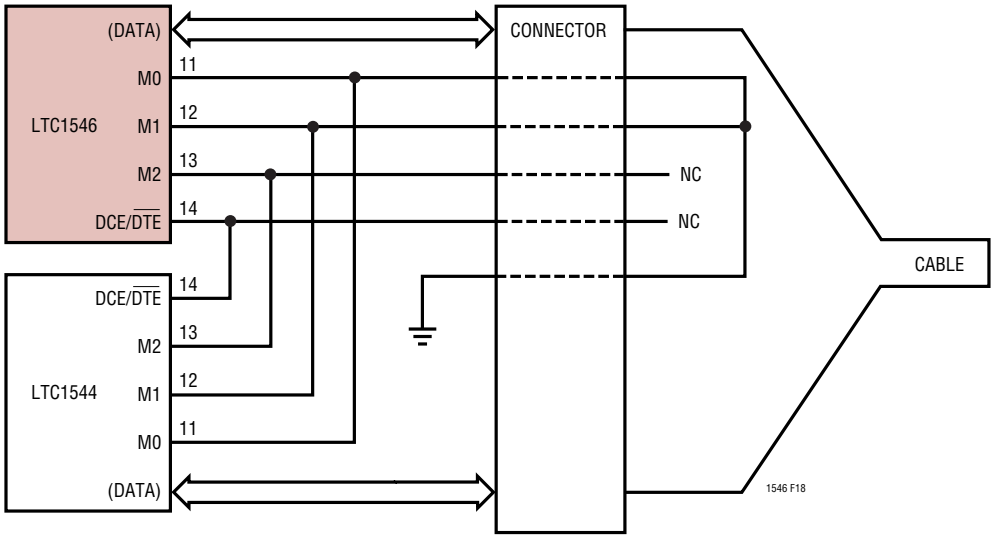


Figure 18: Single Port DCE V.35 Mode Selection in the Cable

V.10 (RS423) Interface

All V.10 drivers and receivers necessary for the RS449, EIA530, EIA530-A, V.36 and X.21 protocols are implemented on the LTC1544.

A typical V.10 unbalanced interface is shown in Figure 19. A V.10 single-ended generator with output A and ground C is connected to a differential receiver with input A' connected to A, and ground C' connected via the signal return to ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 20.

The V.10 receiver configuration in the LTC1544 is shown in Figure 21. In V.10 mode, switch S3 inside the LTC1544 is turned off. The noninverting input is disconnected inside the LTC1544 receiver and connected to ground. The cable termination is then the 30k input impedance to ground of the LTC1544 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 22. A V.11 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.11

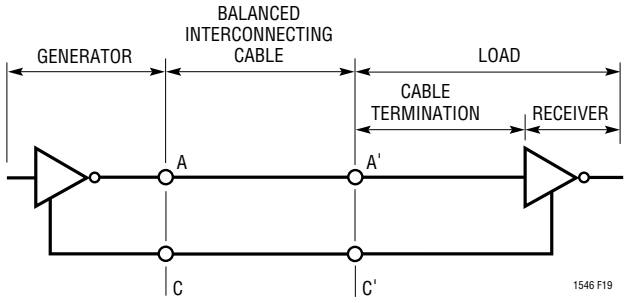


Figure 19. Typical V.10 Interface

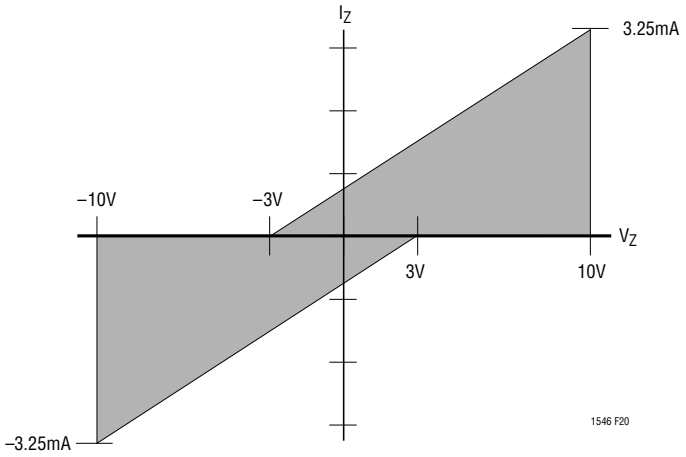


Figure 20. V.10 Receiver Input Impedance

APPLICATIONS INFORMATION

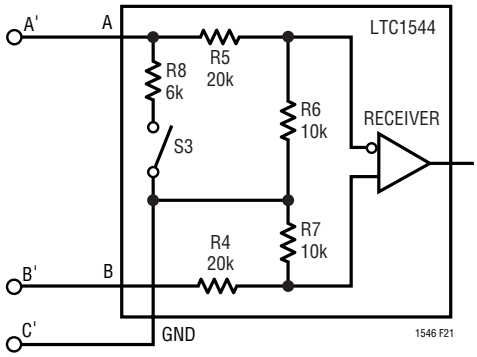


Figure 21. V.10 Receiver Configuration

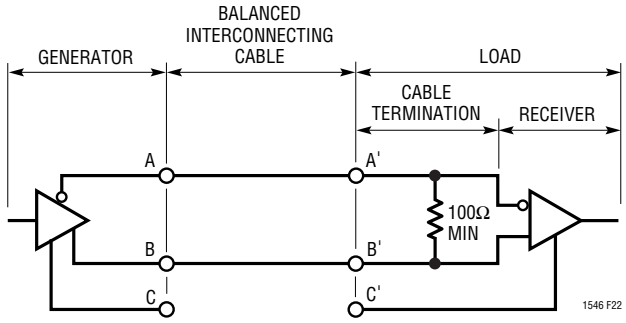


Figure 22. Typical V.11 Interface

interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is essential to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 20.

In V.11 mode, all switches are off except S1 of the LTC1546's receivers which connects a 103Ω differential termination impedance to the cable as shown in Figure 23[1]. The LTC1544 only handles control signals, so no termination other than its V.11 receivers' 30k input impedance is necessary.

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 24. A V.28 single-ended generator with output A and ground C is connected to a single-ended receiver with input A'

[1]Actually, there is no switch S1 in receivers R2 and R3. However, for simplicity, all termination networks on the LTC1546 can be treated identically if it is assumed that an S1 switch exists and is always closed on the R2 and R3 receivers.

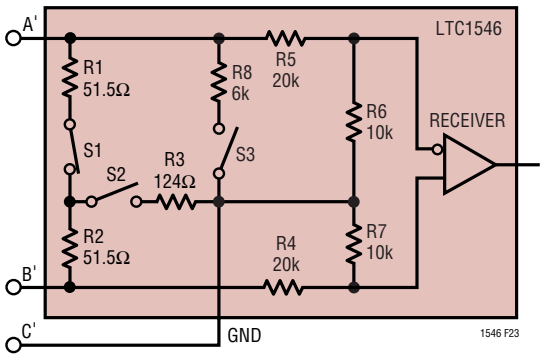


Figure 23. V.11 Receiver Configuration

connected to A and ground C' connected via the signal return to ground C.

In V.28 mode, S3 is closed inside the LTC1546/LTC1544 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 25. Proper termination is only provided when the B input of the receivers is floating, since S1 of the LTC1546's R2 and R3 receivers remains on in V.28 mode[1]. The noninverting input is disconnected inside the LTC1546/LTC1544 receiver and connected to a TTL level reference voltage to give a 1.4V receiver trip point.

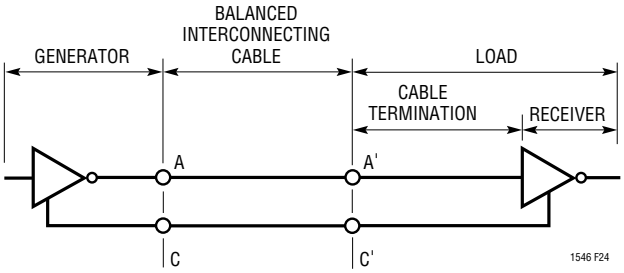


Figure 24. Typical V.28 Interface

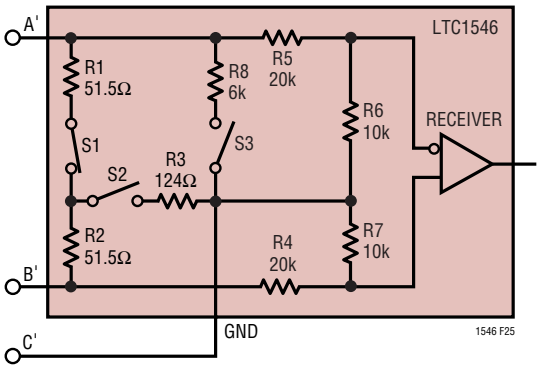


Figure 25. V.28 Receiver Configuration

APPLICATIONS INFORMATION

V.35 Interface

A typical V.35 balanced interface is shown in Figure 26. A V.35 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground (C') must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1546 are on, connecting a T network impedance as shown in Figure 27. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground (C) must be 150Ω ±15Ω.

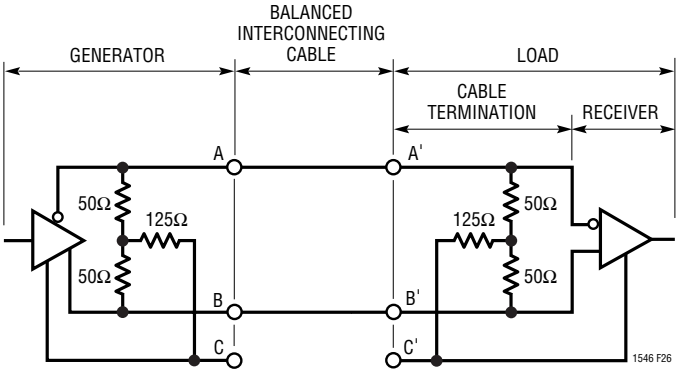


Figure 26. Typical V.35 Interface

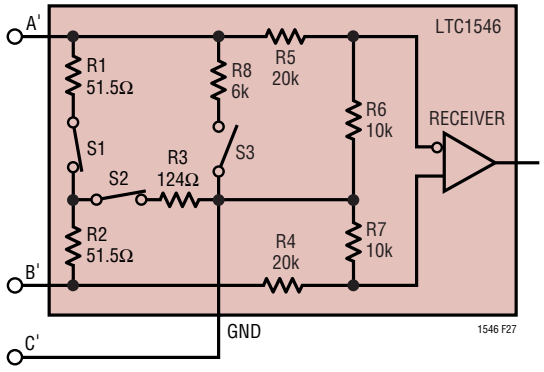


Figure 27. V.35 Receiver Configuration

No-Cable Mode

The no-cable mode (M0 = M1 = M2 = 1) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 200µA. Note that the LTC1546's R2 and R3 receivers continue to be terminated by a 103Ω differential impedance.

Charge Pump

The LTC1546 uses an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 28. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about –7.5V on V_{EE}. Four 1µF surface mounted tantalum or ceramic capacitors are required for C1, C2, C3 and C4. The V_{EE} capacitor C5 should be a minimum of 3.3µF. All capacitors are 16V and should be placed as close as possible to the LTC1546 to reduce EMI.

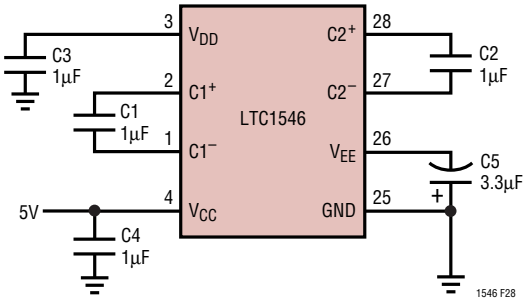


Figure 28. Charge Pump

Receiver Fail-Safe

All LTC1546/LTC1544 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or are shorted together by a termination resistor, the receiver output will always be forced to a logic high.

DTE vs DCE Operation

The DCE/$\overline{\text{DTE}}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC1546, and Driver 3/Receiver 1 and Driver 4/Receiver 4 in the LTC1544. The INVERT pin in the LTC1544 allows the Driver 4/Receiver 4 enable to be high or low true polarity.

APPLICATIONS INFORMATION

The LTC1546/LTC1544 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC1546/LTC1544 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 29. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 30.

A port with one DB-25 connector, that can be configured for either DTE or DCE operation is shown in Figure 31. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via the LTC1546's Driver 1. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

Multiprotocol Interface with RL, LL, TM and a DB-25 Connector

If the RL, LL and TM signals are implemented, there are not enough drivers and receivers available in the LTC1546/LTC1544. In Figure 32, the required control signals are handled by the LTC1545. The LTC1545 has an additional single-ended driver/receiver pair that can handle two more optional control signals such as TM and RL.

Cable-Selectable Multiprotocol Interface

A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 33. The select lines M0, M1 and DCE/$\overline{\text{DTE}}$ are brought out to the connector. The mode is selected by the cable by wiring M0 (connector Pin 18) and M1 (connector Pin 21) and DCE/$\overline{\text{DTE}}$ (connector Pin 25) to ground (connector Pin 7) or letting them float. If M0, M1 or DCE/$\overline{\text{DTE}}$ is floating, internal pull-up current sources will pull the signals to V_{CC}. The select bit M2 is hard wired to V_{CC}. When the cable is pulled out, the interface will go into the no-cable mode.

Compliance Testing

The LTC1546/LTC1544 chipset has been tested by TUV Telecom Services Inc. and passed the NET1, NET2 and TBR2 requirements. Copies of the test reports are available from LTC or TUV Telecom Services.

The titles of the reports are:

NET1 and NET2: Test Report No. NET2/091301/99.

TBR2: Test Report No. CRT2/091301/99.

The address of TUV Telecom Services Inc. is:

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Type Approval Division
1775 Old Highway 8, Ste 107
St. Paul, MN 55112 USA
TEL: +1 (612) 639-0775
FAX: +1 (612) 639-0873

TYPICAL APPLICATIONS

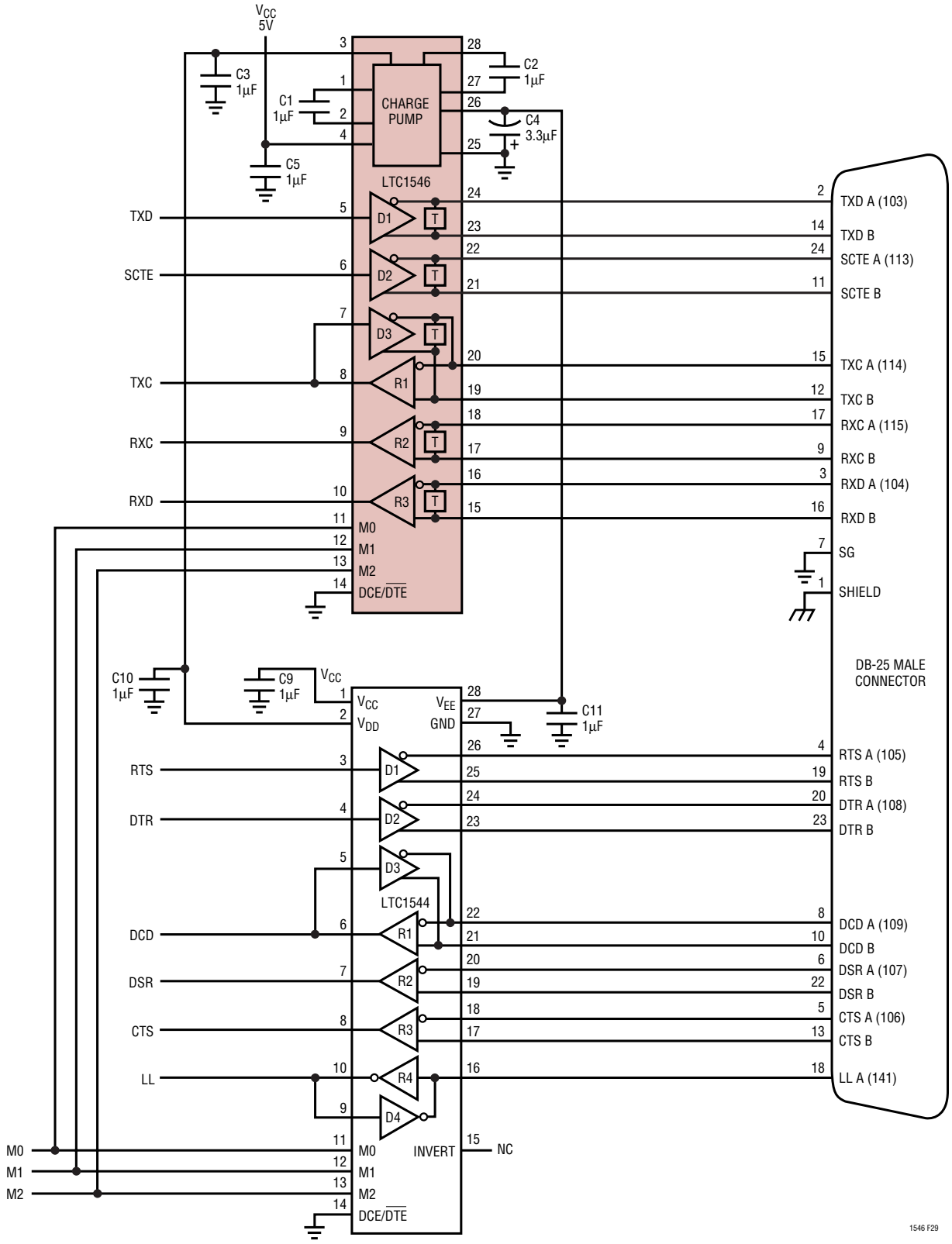


Figure 29. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

TYPICAL APPLICATIONS

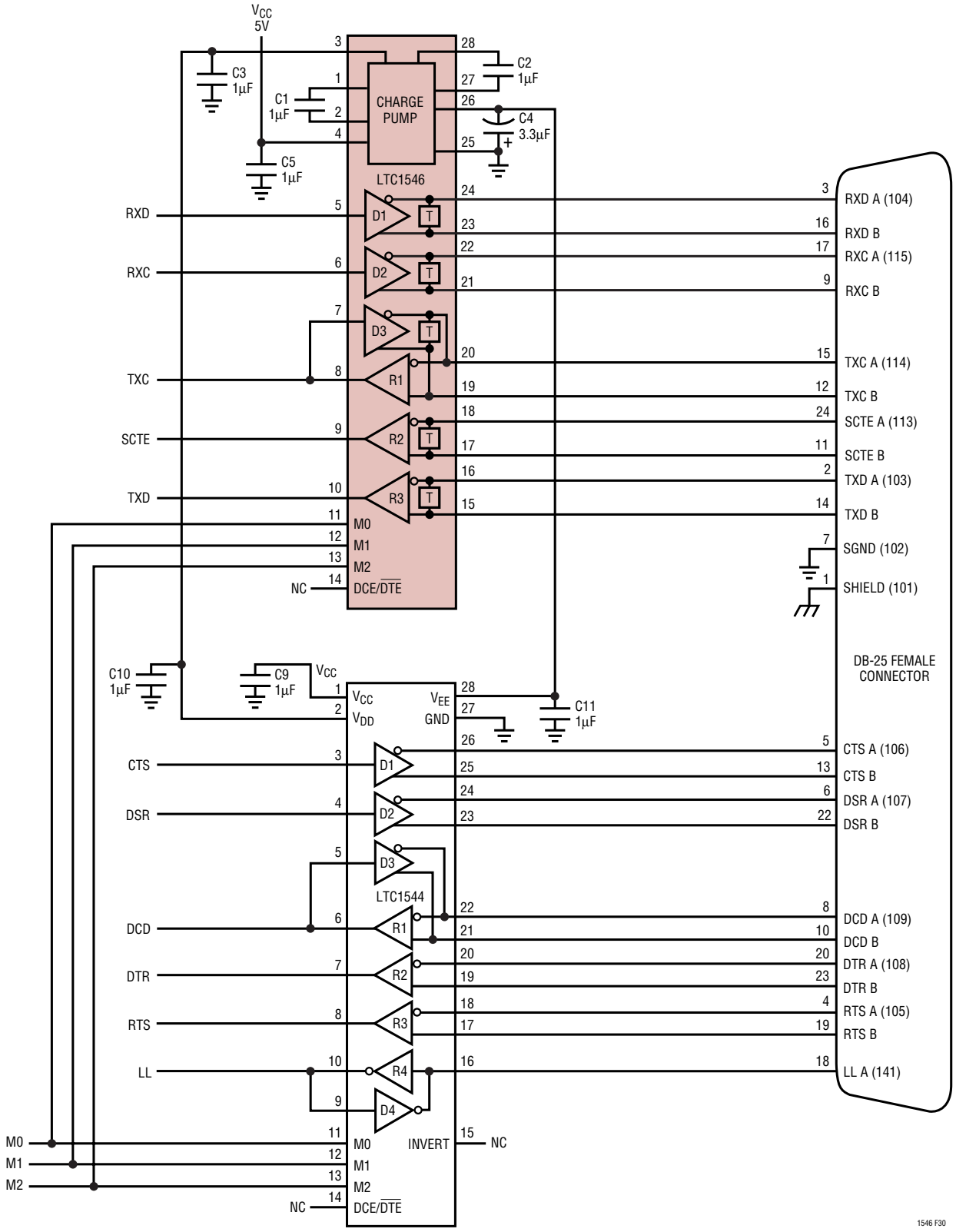


Figure 30. Controller-Selectable DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

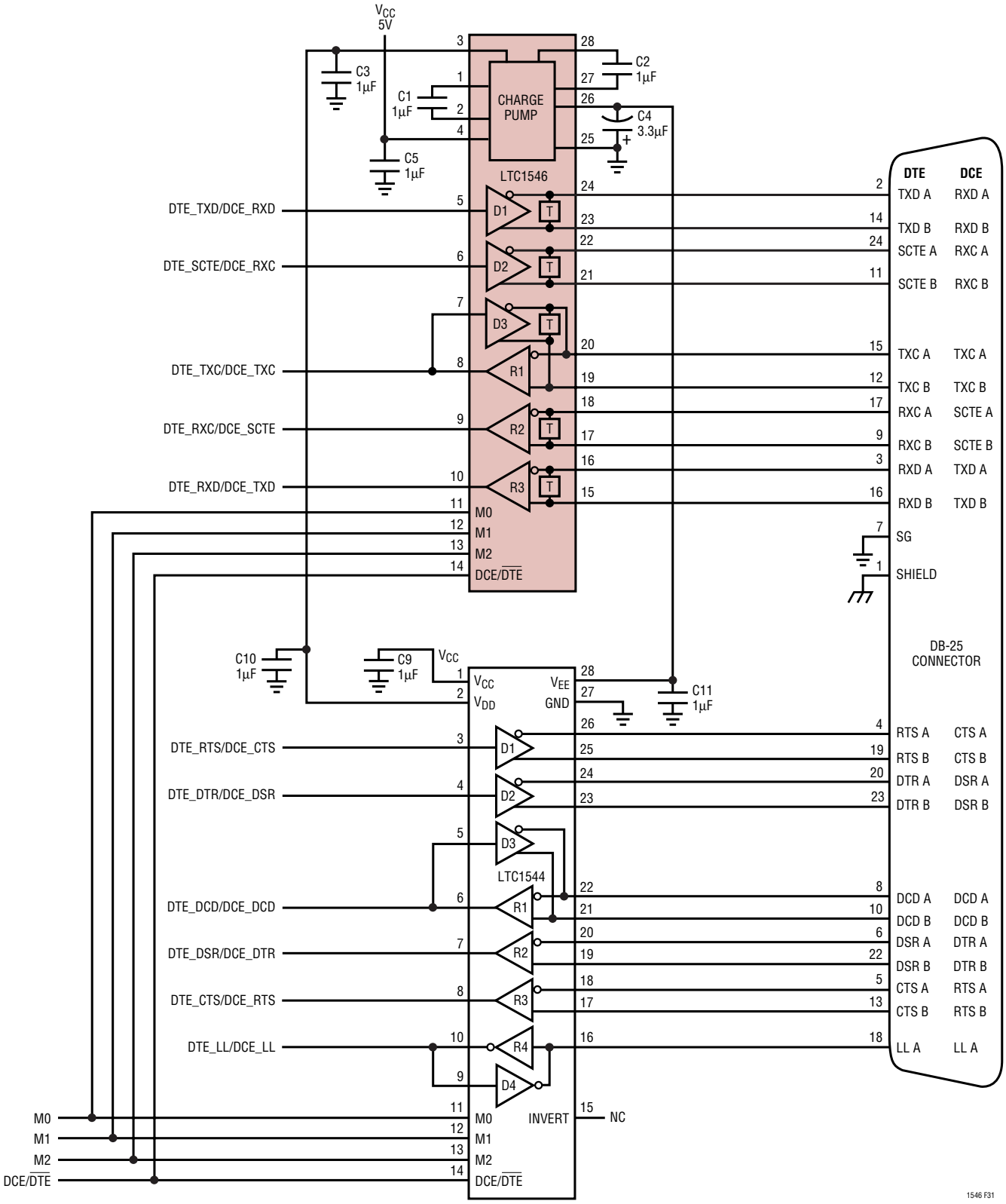


Figure 31. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

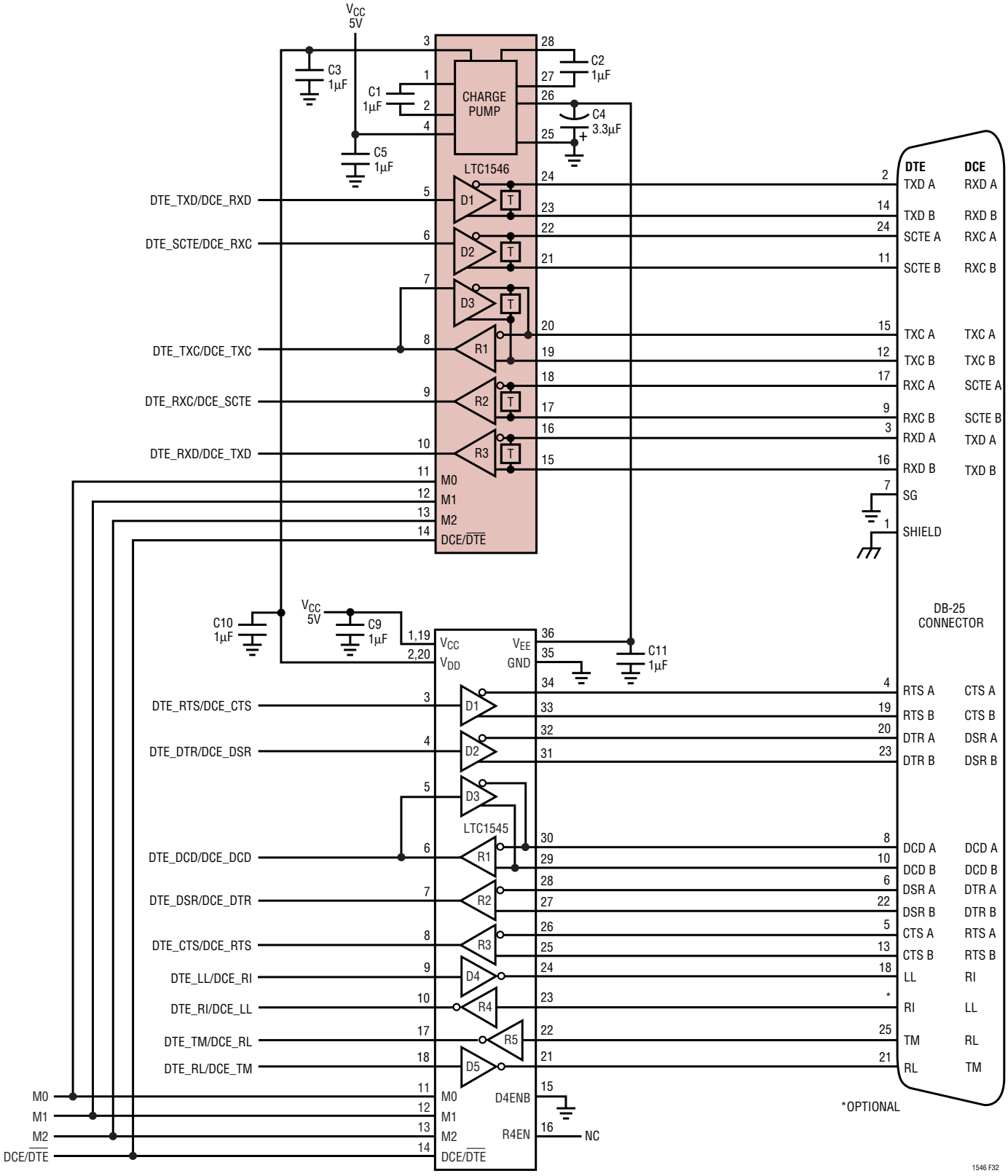
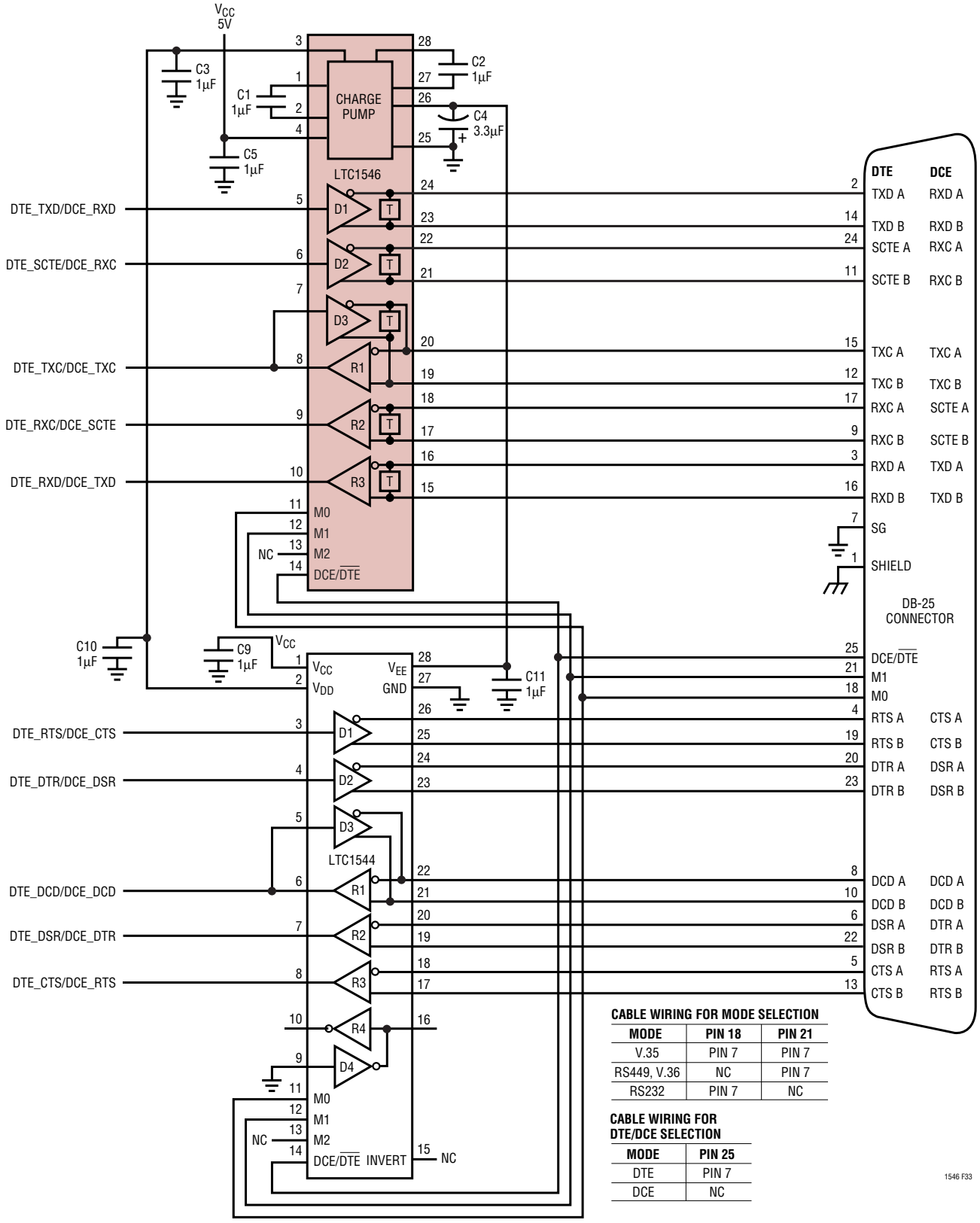


Figure 32. Controller-Selectable Multiprotocol DTE/DCE Port with RL, LL, TM and DB-25 Connector

TYPICAL APPLICATIONS



CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
RS449, V.36	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION

MODE	PIN 25
DTE	PIN 7
DCE	NC

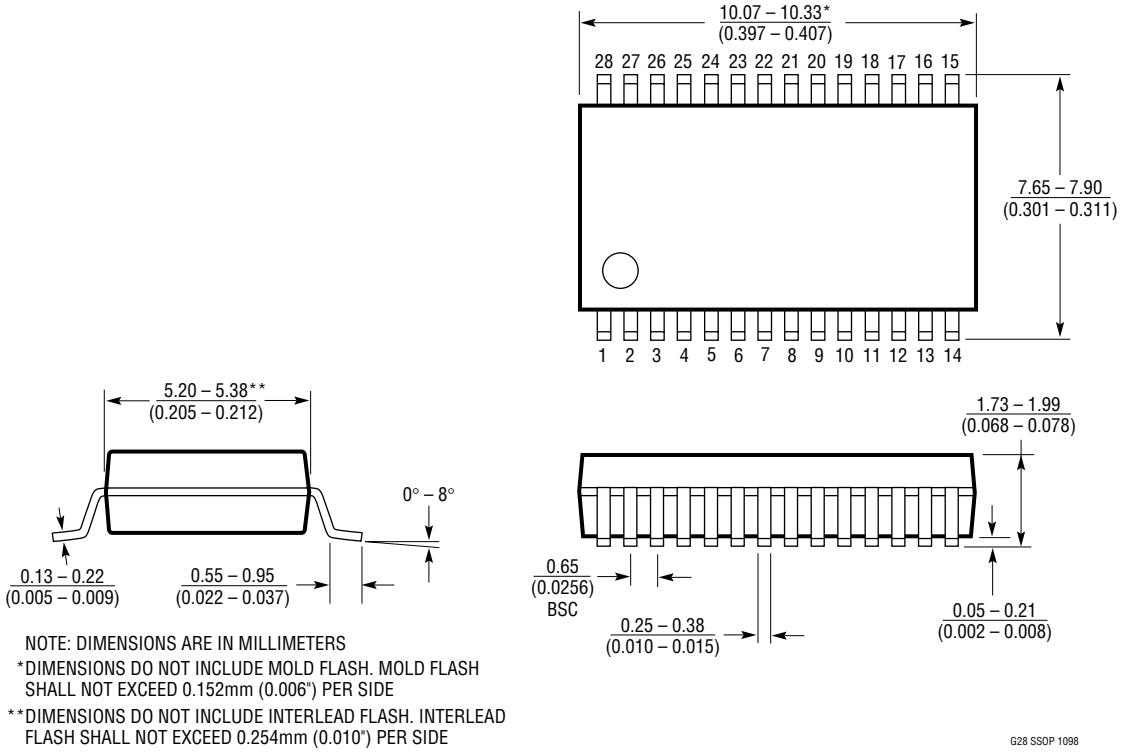
Figure 33. Cable-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

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PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G28 SSOP 1098

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1321	Dual RS232/RS485 Transceiver	Two RS232 Driver/Receiver Pairs or Two RS485 Driver/Receiver Pairs
LTC1334	Single 5V RS232/RS485 Multiprotocol Transceiver	Two RS232 Driver/Receiver or Four RS232 Driver/Receiver Pairs
LTC1343	Software-Selectable Multiprotocol Transceiver	4-Driver/4-Receiver for Data and Clock Signals
LTC1344A	Software-Selectable Cable Terminator	Perfect for Terminating the LTC1543 (Not Needed with LTC1546)
LTC1345	Single Supply V.35 Transceiver	3-Driver/3-Receiver for Data and Clock Signals
LTC1346A	Dual Supply V.35 Transceiver	3-Driver/3-Receiver for Data and Clock Signals
LTC1543	Software-Selectable Multiprotocol Transceiver	Terminated with LTC1344A for Data and Clock Signals, Companion to LTC1544 or LTC1545 for Control Signals
LTC1544	Software-Selectable Multiprotocol Transceiver	Companion to LTC1546 or LTC1543 for Control Signals Including LL
LTC1545	Software-Selectable Multiprotocol Transceiver	5-Driver/5-Receiver Companion to LTC1546 or LTC1543 for Control Signals Including LL, TM and RL

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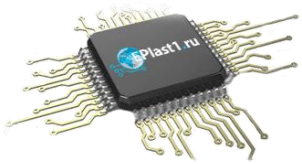
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