Precision Micropower, Low Dropout Voltage References

REF19x Series

FEATURES

Initial accuracy: ±2 mV maximum
Temperature coefficient: 5 ppm/°C maximum
Low supply current: 45 µA maximum
Sleep mode: 15 µA maximum
Low dropout voltage
Load regulation: 4 ppm/mA
Line regulation: 4 ppm/V
High output current: 30 mA
Short-circuit protection

APPLICATIONS

Portable instruments
ADCs and DACs
Smart sensors
Solar-powered applications
Loop current-powered instruments

GENERAL DESCRIPTION

The REF19x series precision band gap voltage references use a patented temperature drift curvature correction circuit and laser trimming of highly stable, thin-film resistors to achieve a very low temperature coefficient and high initial accuracy.

The REF19x series is made up of micropower, low dropout voltage (LDV) devices, providing stable output voltage from supplies as low as 100 mV above the output voltage and consuming less than 45 µA of supply current. In sleep mode, which is enabled by applying a low TTL or CMOS level to the $\overline{\text{SLEEP}}$ pin, the output is turned off, and supply current is further reduced to less than 15 µA.

The REF19x series references are specified over the extended industrial temperature range (−40°C to +85°C), with typical performance specifications over −40°C to +125°C for applications such as automotive.

All electrical grades are available in an 8-lead SOIC_N package; the PDIP and TSSOP packages are available only in the lowest electrical grade. Products are also available in die form.

TEST PINS

Test Pin 1 and Test Pin 5 are reserved for in-package Zener zap. To achieve the highest level of accuracy at the output, the Zener zapping technique is used to trim the output voltage. Since each unit may require a different amount of adjustment, the resistance value at the test pins varies widely from pin to pin and from part to part. The user should leave Pin 1 and Pin 5 unconnected.

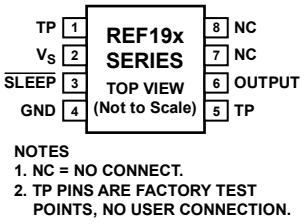


Figure 1. 8-Lead SOIC_N and TSSOP Pin Configuration (S Suffix and RU Suffix)

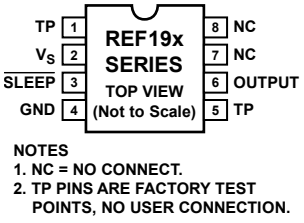


Figure 2. 8-Lead PDIP Pin Configuration (P Suffix)

Table 1. Nominal Output Voltage

Part Number	Nominal Output Voltage (V)
REF191	2.048
REF192	2.50
REF193	3.00
REF194	4.50
REF195	5.00
REF196	3.30
REF198	4.096

Rev. I
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1/96—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—REF191 @ T_A = 25°C

@ V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
E Grade	V_O	I_{OUT} = 0 mA	2.046	2.048	2.050	V
F Grade			2.043		2.053	V
G Grade			2.038		2.058	V
LINE REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
F and G Grades				4	8	ppm/V
LOAD REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 30 mA		4	10	ppm/mA
F and G Grades				6	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.15 V, I_{LOAD} = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 30 mA			1.55	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		20		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF191 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 3.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
F Grade				5	10	ppm/°C
G Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
F and G Grades				10	20	ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 25°C		5	15	ppm/mA
F and G Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.15 V, I_{LOAD} = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 25 mA			1.55	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.

[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$$

[3] Guaranteed by characterization.

[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF191 @ −40°C ≤ T_A ≤+125°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 4.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2		ppm/°C
F Grade				5		ppm/°C
G Grade[3]				10		ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		10		ppm/V
F and G Grades				20		ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA		10		ppm/mA
F and G Grades				20		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 20 mA			1.55	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF192 @ T_A = 25°C

@ V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
E Grade	V_O	I_{OUT} = 0 mA	2.498	2.500	2.502	V
F Grade			2.495		2.505	V
G Grade			2.490		2.510	V
LINE REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
F and G Grades				4	8	ppm/V
LOAD REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 30 mA		4	10	ppm/mA
F and G Grades				6	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.5 V, I_{LOAD} = 10 mA			1.00	V
		V_S = 3.9 V, I_{LOAD} = 30 mA			1.40	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		25		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF192 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 6.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
F Grade				5	10	ppm/°C
G Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
F and G Grades				10	20	ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 25 mA		5	15	ppm/mA
F and G Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.5 V, I_{LOAD} = 10 mA			1.00	V
		V_S = 4.0 V, I_{LOAD} = 25 mA			1.50	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF192 @ −40°C ≤ T_A ≤ +125°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 7.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2		ppm/°C
F Grade				5		ppm/°C
G Grade[3]				10		ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		10		ppm/V
F and G Grades				20		ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA		10		ppm/mA
F and G Grades				20		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.5 V, I_{LOAD} = 10 mA			1.00	V
		V_S = 4.0 V, I_{LOAD} = 20 mA			1.50	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF193 @ T_A = 25°C

@ V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
G Grade	V_O	I_{OUT} = 0 mA	2.990	3.0	3.010	V
LINE REGULATION[2]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.3 V, ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		4	8	ppm/V
LOAD REGULATION[2]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 30 mA		6	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.8 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.0 V, I_{LOAD} = 30 mA			1.00	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		30		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF193 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 9.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
G Grade[3]	TCV_O/°C	I_{OUT} = 0 mA		10	25	ppm/°C
LINE REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.3 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		10	20	ppm/V
LOAD REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 25 mA		10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.8 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.1 V, I_{LOAD} = 30 mA			1.10	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF193 @ T_A ≤ −40°C ≤ +125°C

@ V_S = 3.3 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 10.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
G Grade[3]	TCV_O/°C	I_{OUT} = 0 mA		10		ppm/°C
LINE REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.3 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		20		ppm/V
LOAD REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA		10		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.8 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.1 V, I_{LOAD} = 20 mA			1.10	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF194 @ T_A = 25°C

@ V_S = 5.0 V, T_A = 25°C, unless otherwise noted.

Table 11.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
E Grade	V_O	I_{OUT} = 0 mA	4.498	4.5	4.502	V
F Grade			4.495		4.505	V
G Grade			4.490		4.510	V
LINE REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.75 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
F and G Grades				4	8	ppm/V
LOAD REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.8 V, 0 mA ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
F and G Grades				4	8	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.00 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 5.8 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		45		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF194 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 5.0 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 12.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
F Grade				5	10	ppm/°C
G Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.75 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
F and G Grades				10	20	ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.80 V, 0 mA ≤ I_{OUT} ≤ 25 mA		5	15	ppm/mA
F and G Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.00 V, I_{LOAD} = 10 mA			0.5	V
		V_S = 5.80 V, I_{LOAD} = 25 mA			1.30	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF194 @ −40°C ≤ T_A ≤ +125°C

@ V_S = 5.0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 13.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2		ppm/°C
F Grade				5		ppm/°C
G Grade[3]				10		ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.75 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5		ppm/V
F and G Grades				10		ppm/V
LOAD REGULATION						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.80 V, 0 mA ≤ I_{OUT} ≤ 20 mA		5		ppm/mA
F and G Grades				10		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.10 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 5.95 V, I_{LOAD} = 20 mA			1.45	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF195 @ T_A = 25°C

@ V_S = 5.10 V, T_A = 25°C, unless otherwise noted.

Table 14.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
E Grade	V_O	I_{OUT} = 0 mA	4.998	5.0	5.002	V
F Grade			4.995		5.005	V
G Grade			4.990		5.010	V
LINE REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{IN}$	5.10 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
F and G Grades				4	8	ppm/V
LOAD REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 6.30 V, 0 mA ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
F and G Grades				4	8	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.50 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 6.30 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		50		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF195 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 5.15 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 15.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1,2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
F Grade				5	10	ppm/°C
G Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	5.15 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
F and G Grades				10	20	ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 6.30 V, 0 mA ≤ I_{OUT} ≤ 25 mA		5	10	ppm/mA
F and G Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.50 V, I_{LOAD} = 10 mA			0.50	V
		V_S = 6.30 V, I_{LOAD} = 25 mA			1.30	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$$

[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF195 @ −40°C ≤ T_A ≤ +125°C

@ V_S = 5.20 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 16.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2		ppm/°C
F Grade				5		ppm/°C
G Grade[3]				10		ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	5.20 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5		ppm/V
F and G Grades				10		ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 6.45 V, 0 mA ≤ I_{OUT} ≤ 20 mA		5		ppm/mA
F and G Grades				10		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 5.60 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 6.45 V, I_{LOAD} = 20 mA			1.45	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF196 @ T_A = 25°C

@ V_S = 3.5 V, T_A = 25°C, unless otherwise noted.

Table 17.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
G Grade	V_O	I_{OUT} = 0 mA	3.290	3.3	3.310	V
LINE REGULATION[2]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.50 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		4	8	ppm/V
LOAD REGULATION[2]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 30 mA		6	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.1 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.3 V, I_{LOAD} = 30 mA			1.00	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		33		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF196 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 3.5 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 18.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
G Grade[3]	TCV_O/°C	I_{OUT} = 0 mA		10	25	ppm/°C
LINE REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.5 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		10	20	ppm/V
LOAD REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 25 mA		10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.1 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.3 V, I_{LOAD} = 25 mA			1.00	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF196 @ −40°C ≤ T_A ≤ +125°C

@ V_S = 3.50 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 19.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
G Grade[3]	TCV_O/°C	I_{OUT} = 0 mA		10		ppm/°C
LINE REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{IN}$	3.50 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		20		ppm/V
LOAD REGULATION[4]						
G Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA		20		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.1 V, I_{LOAD} = 10 mA			0.80	V
		V_S = 4.4 V, I_{LOAD} = 20 mA			1.10	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF198 @ T_A = 25°C

@ V_S = 5.0 V, T_A = 25°C, unless otherwise noted.

Table 20.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
INITIAL ACCURACY[1]						
E Grade	V_O	I_{OUT} = 0 mA	4.094	4.096	4.098	V
F Grade			4.091		4.101	V
G Grade			4.086		4.106	V
LINE REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.5 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
F and G Grades				4	8	ppm/V
LOAD REGULATION[2]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.4 V, 0 mA ≤ I_{OUT} ≤ 30 mA		2	4	ppm/mA
F and G Grades				4	8	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.6 V, I_{LOAD} = 10 mA			0.502	V
		V_S = 5.4 V, I_{LOAD} = 30 mA			1.30	V
LONG-TERM STABILITY[3]	DV_O	1000 hours @ 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		40		µV p-p

[1] Initial accuracy includes temperature hysteresis effect.
[2] Line and load regulation specifications include the effect of self-heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

ELECTRICAL CHARACTERISTICS—REF198 @ −40°C ≤ T_A ≤ +85°C

@ V_S = 5.0 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 21.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
F Grade				5	10	ppm/°C
G Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.5 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
F and G Grades				10	20	ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.4 V, 0 mA ≤ I_{OUT} ≤ 25 mA		5	10	ppm/mA
F and G Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.6 V, I_{LOAD} = 10 mA			0.502	V
		V_S = 5.4 V, I_{LOAD} = 25 mA			1.30	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	µA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	µA
SUPPLY CURRENT		No load			45	µA
Sleep Mode		No load			15	µA

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

ELECTRICAL CHARACTERISTICS—REF198 @ −40°C ≤ T_A ≤ +125°C

@ V_S = 5.0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 22.

Parameter	Mnemonic	Condition	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]						
E Grade	TCV_O/°C	I_{OUT} = 0 mA		2		ppm/°C
F Grade				5		ppm/°C
G Grade[3]				10		ppm/°C
LINE REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{IN}$	4.5 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5		ppm/V
F and G Grades				10		ppm/V
LOAD REGULATION[4]						
E Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.6 V, 0 mA ≤ I_{OUT} ≤ 20 mA		5		ppm/mA
F and G Grades				10		ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 4.7 V, I_{LOAD} = 10 mA			0.60	V
		V_S = 5.6 V, I_{LOAD} = 20 mA			1.50	V

[1] For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.
$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$
[3] Guaranteed by characterization.
[4] Line and load regulation specifications include the effect of self-heating.

WAFER TEST LIMITS

For proper operation, a 1 µF capacitor is required between the output pins and the GND pin of the REF19x. Electrical tests and wafer probe to the limits are shown in **Table 23**. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

@ I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.

Table 23.

Parameter	Mnemonic	Condition	Limit	Unit
INITIAL ACCURACY				
REF191	V_O		2.043/2.053	V
REF192			2.495/2.505	V
REF193			2.990/3.010	V
REF194			4.495/4.505	V
REF195			4.995/5.005	V
REF196			3.290/3.310	V
REF198			4.091/4.101	V
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	(V_O + 0.5 V) < V_{IN} < 15 V, I_{OUT} = 0 mA	15	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_{LOAD}$	0 mA < I_{LOAD} < 30 mA, V_{IN} = (V_O + 1.3 V)	15	ppm/mA
DROPOUT VOLTAGE	$V_O - V+$	I_{LOAD} = 10 mA	1.25	V
		I_{LOAD} = 30 mA	1.55	V
$\overline{\text{SLEEP}}$ MODE INPUT				
Logic Input High	V_{IH}		2.4	V
Logic Input Low	V_{IL}		0.8	V
SUPPLY CURRENT	V_{IN} = 15 V	No load	45	µA
Sleep Mode		No load	15	µA

ABSOLUTE MAXIMUM RATINGS

Table 24.

Parameter[1]	Rating
Supply Voltage	−0.3 V, +18 V
Output to GND	−0.3 V, V_S + 0.3 V
Output to GND Short-Circuit Duration	Indefinite
Storage Temperature Range	
PDIP, SOIC_N Package	−65°C to +150°C
Operating Temperature Range	
REF19x	−40°C to +85°C
Junction Temperature Range	
PDIP, SOIC_N Package	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 25. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead PDIP	103	43	°C/W
8-Lead SOIC_N	158	43	°C/W

[1] θ_{JA} is specified for worst-case conditions; that is, θ_{JA} is specified for the device in socket for PDIP and is specified for the device soldered in the circuit board for the SOIC package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

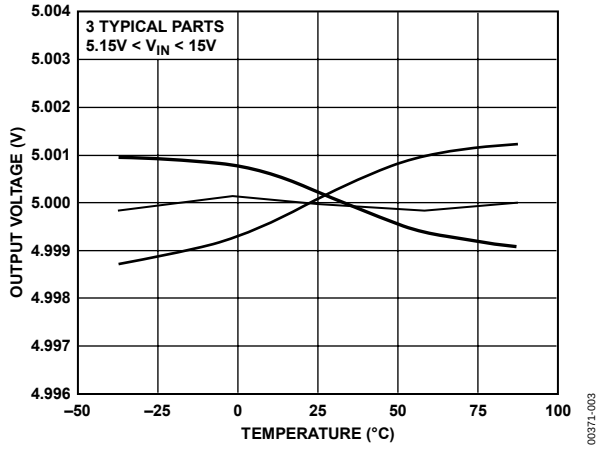


Figure 3. REF195 Output Voltage vs. Temperature

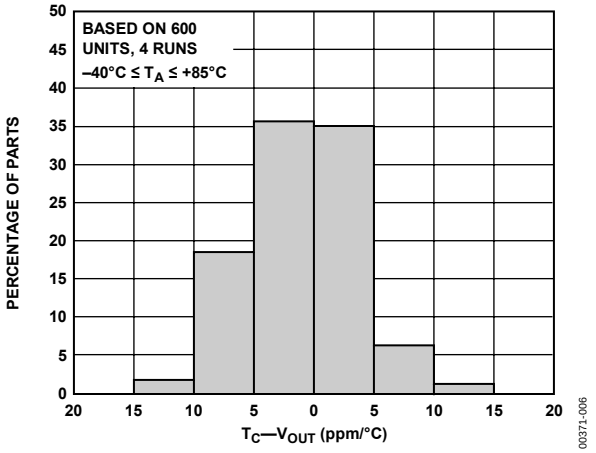


Figure 6. T_C—V_{OUT} Distribution

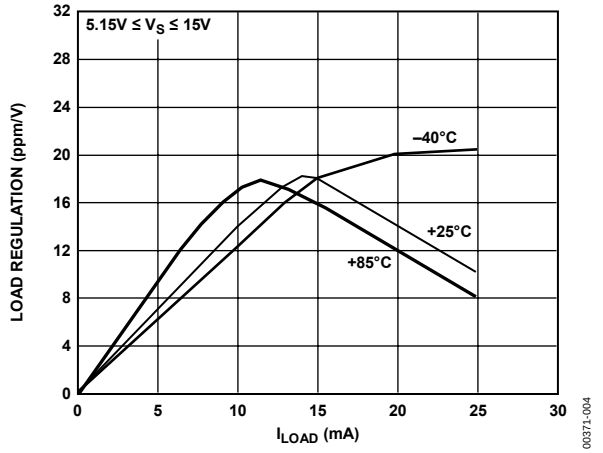


Figure 4. REF195 Load Regulator vs. I_{LOAD}

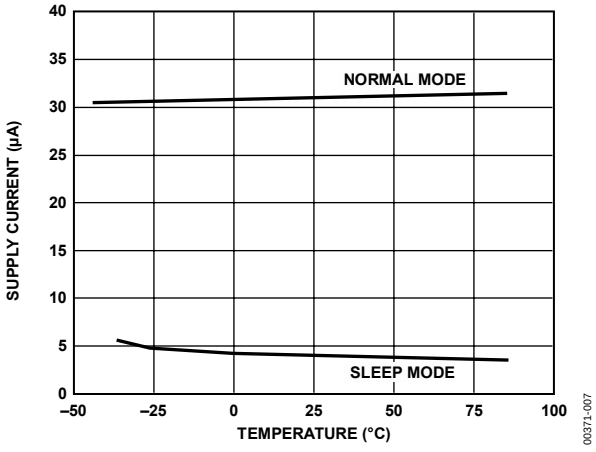


Figure 7. Supply Current vs. Temperature

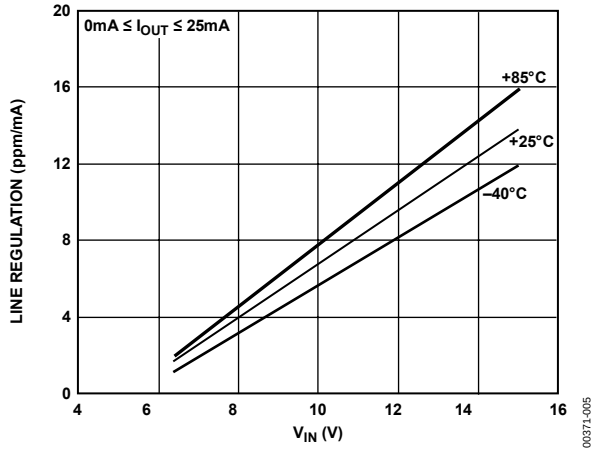


Figure 5. REF195 Line Regulator vs. V_{IN}

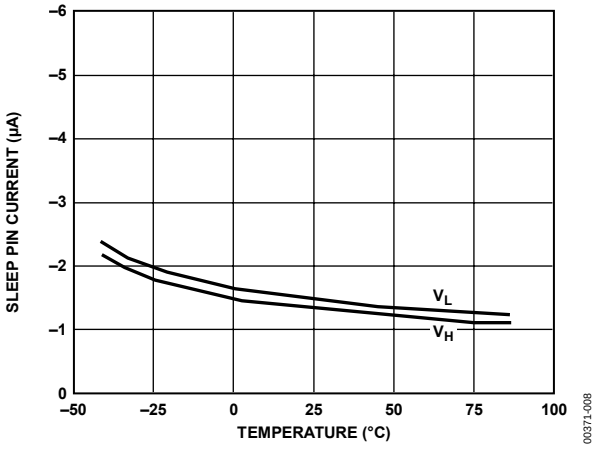


Figure 8. $\overline{SLEEP}$ Pin Current vs. Temperature

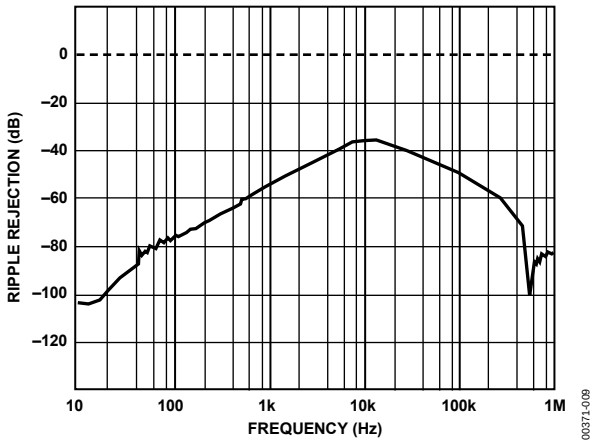


Figure 9. Ripple Rejection vs. Frequency

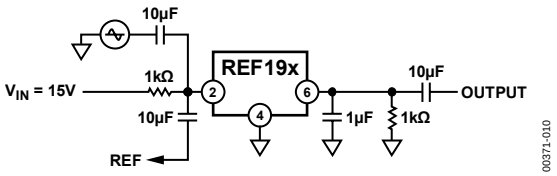


Figure 10. Ripple Rejection vs. Frequency Measurement Circuit

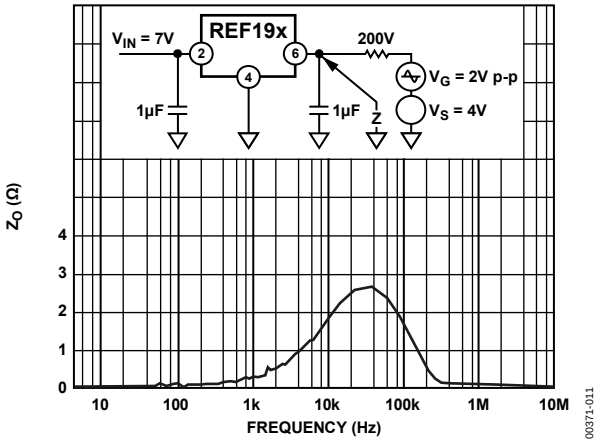


Figure 11. Output Impedance vs. Frequency

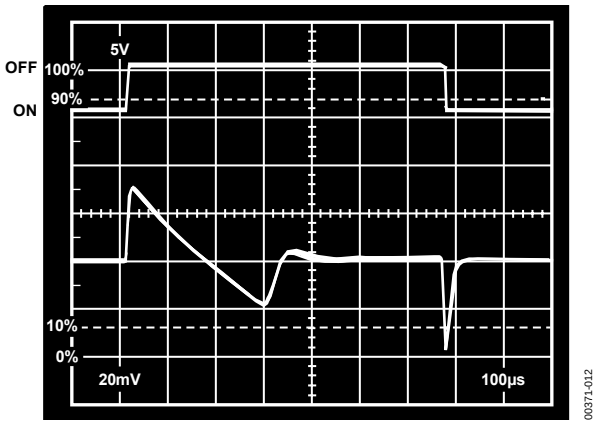


Figure 12. Load Transient Response

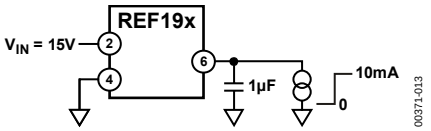


Figure 13. Load Transient Response Measurement Circuit

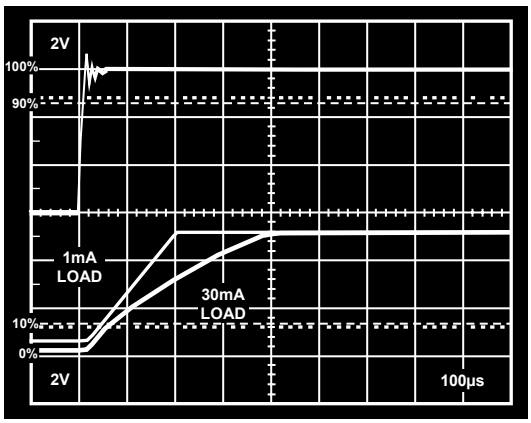


Figure 14. Power-On Response Time

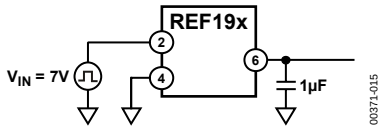


Figure 15. Power-On Response Time Measurement Circuit

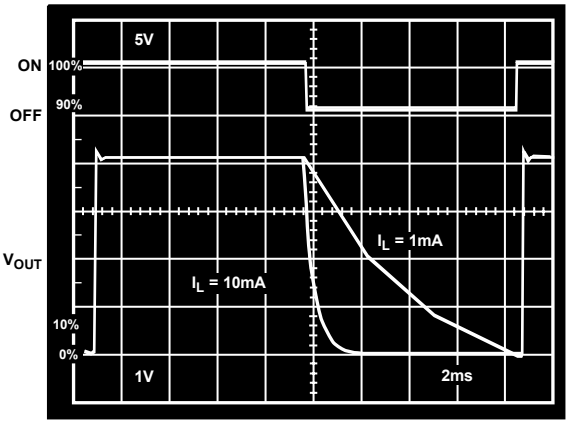


Figure 16. $\overline{SLEEP}$ Response Time

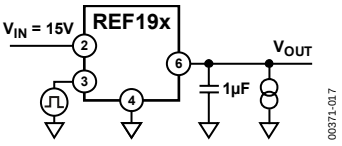


Figure 17. $\overline{SLEEP}$ Response Time Measurement Circuit

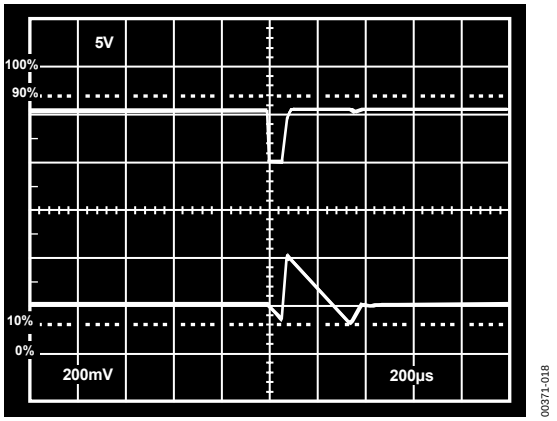


Figure 18. Line Transient Response

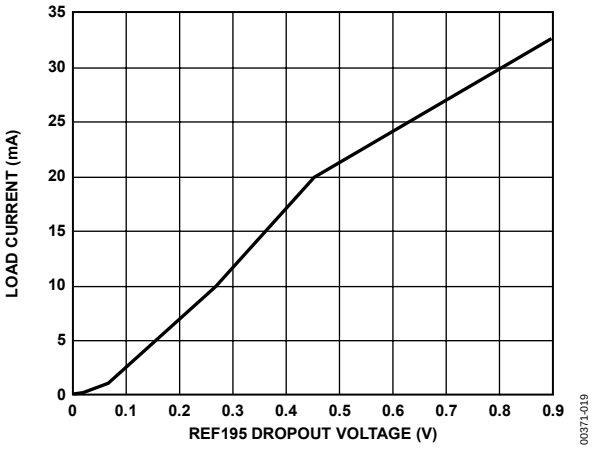


Figure 19. Load Current vs. Dropout Voltage

APPLICATIONS

OUTPUT SHORT-CIRCUIT BEHAVIOR

The REF19x family of devices is completely protected from damage due to accidental output shorts to GND or to V+. In the event of an accidental short-circuit condition, the reference device shuts down and limits its supply current to 40 mA.

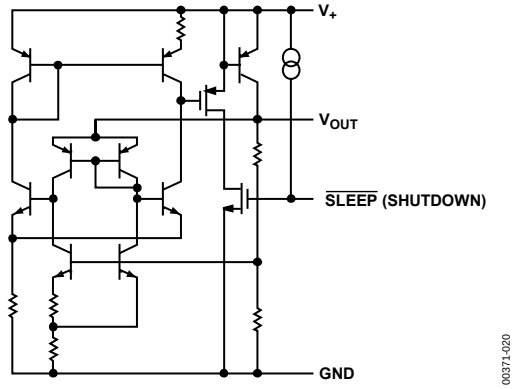


Figure 20. Simplified Schematic

DEVICE POWER DISSIPATION CONSIDERATIONS

The REF19x family of references is capable of delivering load currents to 30 mA with an input voltage that ranges from 3.3 V to 5 V. When these devices are used in applications with large input voltages, exercise care to avoid exceeding the maximum internal power dissipation of these devices. Exceeding the published specifications for maximum power dissipation or junction temperature can result in premature device failure. The following formula should be used to calculate a device's maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

In this equation, T_J and T_A are the junction and ambient temperatures, respectively; P_D is the device power dissipation; and θ_{JA} is the device package thermal resistance.

OUTPUT VOLTAGE BYPASSING

For stable operation, low dropout voltage regulators and references generally require a bypass capacitor connected from their V_{OUT} pins to their GND pins. Although the REF19x family of references is capable of stable operation with capacitive loads exceeding 100 µF, a 1 µF capacitor is sufficient to guarantee rated performance. The addition of a 0.1 µF ceramic capacitor in parallel with the bypass capacitor improves load current transient performance. For best line voltage transient performance, it is recommended that the voltage inputs of these devices be bypassed with a 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

SLEEP MODE OPERATION

All REF19x devices include a sleep capability that is TTL/CMOS-level compatible. Internally, a pull-up current source to V_{IN} is connected at the $\overline{SLEEP}$ pin. This permits the $\overline{SLEEP}$ pin to be driven from an open collector/drain driver. A logic low or a 0 V condition on the $\overline{SLEEP}$ pin is required to turn off the output stage. During sleep, the output of the references becomes a high impedance state where its potential would then be determined by external circuitry. If the sleep feature is not used, it is recommended that the $\overline{SLEEP}$ pin be connected to V_{IN} (Pin 2).

BASIC VOLTAGE REFERENCE CONNECTIONS

The circuit in Figure 21 illustrates the basic configuration for the REF19x family of references. Note the 10 µF/0.1 µF bypass network on the input and the 1 µF/0.1 µF bypass network on the output. It is recommended that no connections be made to Pin 1, Pin 5, Pin 7, and Pin 8. If the sleep feature is not required, Pin 3 should be connected to V_{IN}.

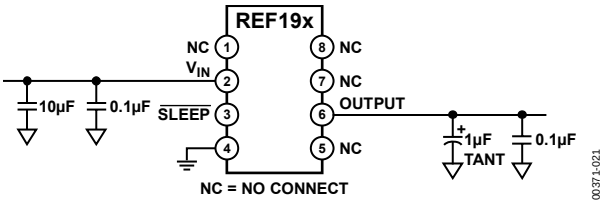


Figure 21. Basic Voltage Reference Configuration

MEMBRANE SWITCH-CONTROLLED POWER SUPPLY

With output load currents in the tens of mA, the REF19x family of references can operate as a low dropout power supply in hand-held instrument applications. In the circuit shown in Figure 22, a membrane on/off switch is used to control the operation of the reference. During an initial power-on condition, the $\overline{SLEEP}$ pin is held to GND by the 10 kΩ resistor. Recall that this condition (read: three-state) disables the REF19x output. When the membrane on switch is pressed, the $\overline{SLEEP}$ pin is momentarily pulled to V_{IN}, enabling the REF19x output. At this point, current through the 10 kΩ resistor is reduced, and the internal current source connected to the $\overline{SLEEP}$ pin takes control. Pin 3 assumes and remains at the same potential as V_{IN}. When the membrane off switch is pressed, the $\overline{SLEEP}$ pin is momentarily connected to GND, which once again disables the REF19x output.

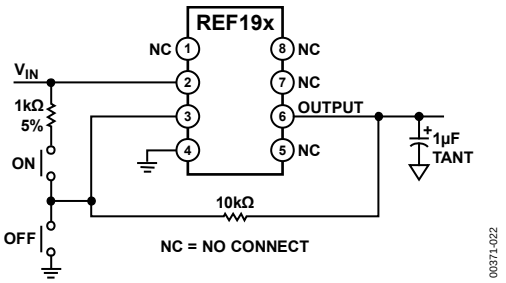
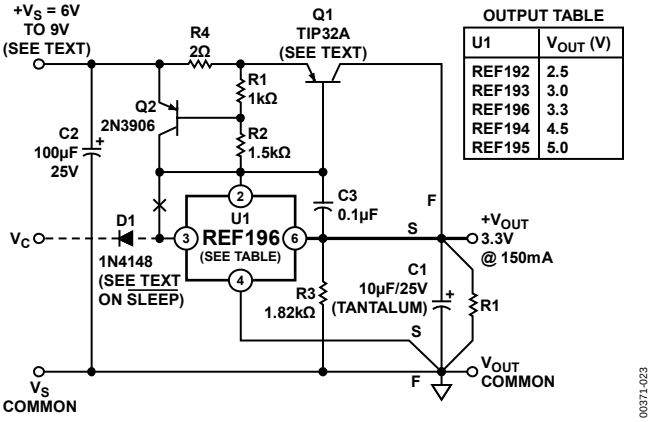


Figure 22. Membrane Switch-Controlled Power Supply

CURRENT-BOOSTED REFERENCES WITH CURRENT LIMITING

While the 30 mA rated output current of the REF19x series is higher than is typical of other reference ICs, it can be boosted to higher levels, if desired, with the addition of a simple external PNP transistor, as shown in Figure 23. Full-time current limiting is used to protect the pass transistor against shorts.



OUTPUT TABLE	
U1	V_{OUT} (V)
REF192	2.5
REF193	3.0
REF196	3.3
REF194	4.5
REF195	5.0

Figure 23. Boosted 3.3 V Referenced with Current Limiting

In this circuit, the power supply current of reference U1 flowing through R1 to R2 develops a base drive for Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100 mA to 200 mA loads, U1 is never required to furnish more than a few mA, so this factor minimizes temperature-related drift. Short-circuit protection is provided by Q2, which clamps the drive to Q1 at about 300 mA of load current, with values as shown in Figure 23. With this separation of control and power functions, dc stability is optimum, allowing most advantageous use of premium grade REF19x devices for U1. Of course, load management should still be exercised. A short, heavy, low dc resistance (DCR) conductor should be used from U1 to U6 to the V_{OUT} Sense Point S, where the collector of Q1 connects to the load, Point F.

Because of the current limiting configuration, the dropout voltage circuit is raised about 1.1 V over that of the REF19x devices, due to the V_{BE} of Q1 and the drop across Current Sense Resistor R4. However, overall dropout is typically still low enough to allow operation of a 5 V to 3.3 V regulator/reference using the REF196 for U1 as noted, with a V_S as low as 4.5 V and a load current of 150 mA.

The requirement for a heat sink on Q1 depends on the maximum input voltage and short-circuit current. With V_S = 5 V and a 300 mA current limit, the worst-case dissipation of Q1 is 1.5 W, less than the TO-220 package 2 W limit. However, if smaller TO-39 or TO-5 packaged devices, such as the 2N4033, are used, the current limit should be reduced to keep maximum dissipation below the package rating. This is accomplished by simply raising R4.

A tantalum output capacitor is used at C1 for its low equivalent series resistance (ESR), and the higher value is required for stability. Capacitor C2 provides input bypassing and can be an ordinary electrolytic.

Shutdown control of the booster stage is an option, and when used, some cautions are needed. Due to the additional active devices in the V_S line to U1, a direct drive to Pin 3 does not work as with an unbuffered REF19x device. To enable shutdown control, the connection from U1 to U2 is broken at the X, and Diode D1 then allows a CMOS control source, V_C, to drive U1 to U3 for on/off operation. Startup from shutdown is not as clean under heavy load as it is in basic REF19x series, and can require several milliseconds under load. Nevertheless, it is still effective and can fully control 150 mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

NEGATIVE PRECISION REFERENCE WITHOUT PRECISION RESISTORS

In many current-output CMOS DAC applications where the output signal voltage must be the same polarity as the reference voltage, it is often necessary to reconfigure a current-switching DAC into a voltage-switching DAC using a 1.25 V reference, an op amp, and a pair of resistors. Using a current-switching DAC directly requires an additional operational amplifier at the output to reinvert the signal. A negative voltage reference is then desirable, because an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference using an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

The circuit illustrated in Figure 24 avoids the need for tightly matched resistors by using an active integrator circuit. In this circuit, the output of the voltage reference provides the input drive for the integrator. To maintain circuit equilibrium, the integrator adjusts its output to establish the proper relationship between the reference's V_{OUT} and GND. Thus, any desired negative output voltage can be selected by substituting for the appropriate reference IC. The sleep feature is maintained in the circuit with the simple addition of a PNP transistor and a 10 kΩ resistor.

One caveat to this approach is that although rail-to-rail output amplifiers work best in the application, these operational amplifiers require a finite amount (mV) of headroom when required to provide any load current. The choice for the circuit's negative supply should take this issue into account.

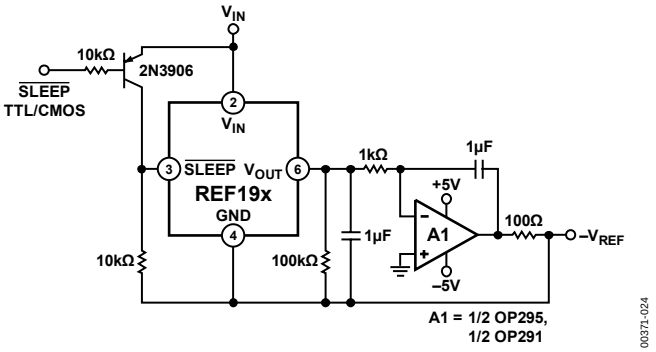


Figure 24. Negative Precision Voltage Reference Uses No Precision Resistors

STACKING REFERENCE ICS FOR ARBITRARY OUTPUTS

Some applications may require two reference voltage sources that are a combined sum of standard outputs. The circuit shown in Figure 25 shows how this stacked output reference can be implemented.

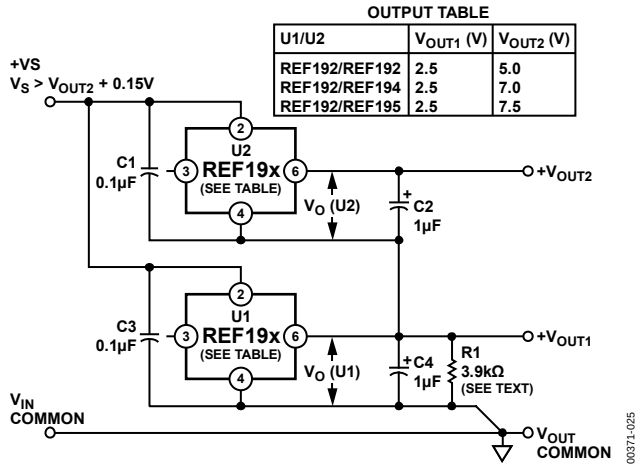


Figure 25. Stacking Voltage References with the REF19x

Two reference ICs are used, fed from a common unregulated input, V_S. The outputs of the individual ICs are connected in series, as shown in Figure 25, which provide two output voltages, V_{OUT1} and V_{OUT2}. V_{OUT1} is the terminal voltage of U1, while V_{OUT2} is the sum of this voltage and the terminal voltage of U2. U1 and U2 are chosen for the two voltages that supply the required outputs (see Output Table in Figure 25). If, for example, both U1 and U2 are REF192s, the two outputs are 2.5 V and 5.0 V.

While this concept is simple, some cautions are needed. Since the lower reference circuit must sink a small bias current from U2 (50 µA to 100 µA), plus the base current from the series PNP output transistor in U2, either the external load of U1 or R1 must provide a path for this current. If the U1 minimum load is not well defined, Resistor R1 should be used, set to a value that conservatively passes 600 µA of current with the applicable V_{OUT1} across it. Note that the two U1 and U2 reference circuits are locally treated as macrocells, each having its own bypasses at input and output for best stability. Both U1 and U2 in this circuit can source dc currents up to their full rating. The minimum input voltage, V_S, is determined by the sum of the outputs, V_{OUT2}, plus the dropout voltage of U2.

A related variation on stacking two 3-terminal references is shown in Figure 26, where U1, a REF192, is stacked with a 2-terminal reference diode, such as the AD589. Like the 3-terminal stacked reference above, this circuit provides two outputs, VOUT1 and VOUT2, which are the individual terminal voltages of D1 and U1, respectively. Here this is 1.235 V and 2.5 V, which provides a V_{OUT2} of 3.735 V. When using 2-terminal reference diodes, such as D1, the rated minimum and maximum device currents must be observed, and the maximum load current from V_{OUT1} can be no greater than the current setup by R1 and V_O (U1). When V_O (U1) is equal to 2.5 V, R1 provides a 500 µA bias to D1, so the maximum load current available at V_{OUT1} is 450 µA or less.

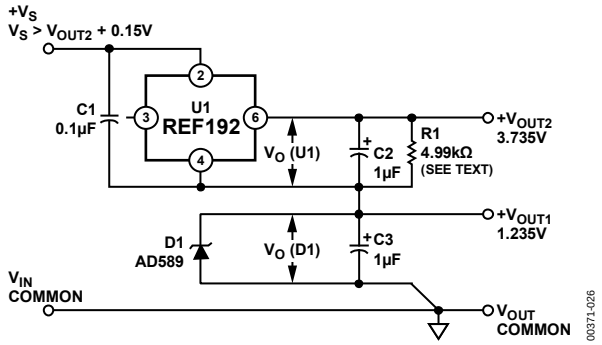


Figure 26. Stacking Voltage References with the REF192

PRECISION CURRENT SOURCE

In low power applications, the need often arises for a precision current source that can operate on low supply voltages. As shown in Figure 27, any one of the devices in the REF19x family of references can be configured as a precision current source. The circuit configuration illustrated is a floating current source with a grounded load. The output voltage of the reference is bootstrapped across R_{SET}, which sets the output current into the load. With this configuration, circuit precision is maintained for load currents in the range from the reference's supply current (typically 30 µA) to approximately 30 mA. The low dropout voltage of these devices maximizes the current source's output voltage compliance without excess headroom.

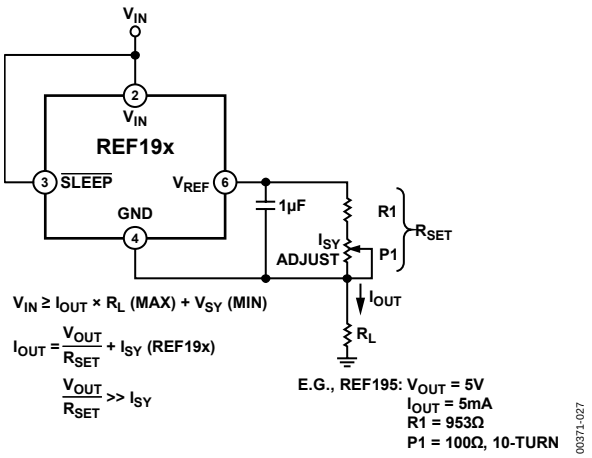


Figure 27. A Low Dropout, Precision Current Source

The governing equations for the circuit are

$$V_{IN} = I_{OUT} \times R_L\ (Max) + V_{SY}\ (Min,\ REF19x)$$

$$I_{OUT} = \frac{V_{OUT}}{R_{SET}} + I_{SY}\ (REF19x)$$

$$\frac{V_{OUT}}{R_{SET}} \rangle\rangle\ I_{SY}\ (REF19x)$$

SWITCHED OUTPUT 5 V/3.3 V REFERENCE

Applications often require digital control of reference voltages, selecting between one stable voltage and a second. With the sleep feature inherent to the REF19x series, switched output reference configurations are easily implemented with little additional hardware.

The circuit in Figure 28 illustrates the general technique, which takes advantage of the output wire-OR capability of the REF19x device family. When off, a REF19x device is effectively an open circuit at the output node with respect to the power supply. When on, a REF19x device can source current up to its current rating, but sink only a few µA (essentially, just the relatively low current of the internal output scaling divider). Consequently, when two devices are wired together at their common outputs, the output voltage is the same as the output voltage for the on device. The off state device draws a small standby current of 15 µA (max), but otherwise does not interfere with operation of the on device, which can operate to its full current rating. Note that the two devices in the circuit conveniently share both input and output capacitors, and with CMOS logic drive, it is power efficient.

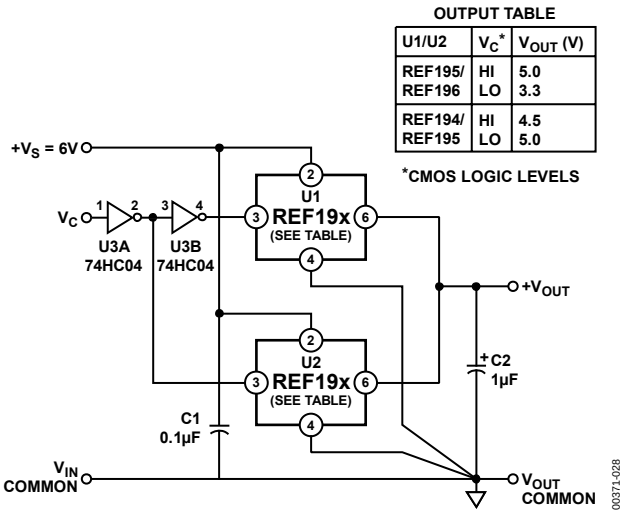


Figure 28. Switched Output Reference

Using dissimilar REF19x series devices with this configuration allows logic selection between the U1/U2-specified terminal voltages. For example, with U1 (a REF195) and U2 (a REF196), as noted in the table in Figure 28, changing the CMOS-compatible V_C logic control voltage from HI to LO selects between a nominal output of 5 V and 3.3 V, and vice versa. Other REF19x family units can also be used for U1/U2, with similar operation in a logic sense, but with outputs as per the individual paired devices (see the table in Figure 28). Of course, the exact output voltage tolerance, drift, and overall quality of the reference voltage is consistent with the grade of individual U1 and U2 devices.

Due to the nature of the wire-OR, one application caveat should be understood about this circuit. Since U1 and U2 can only source current effectively, negative going output voltage changes, which require the sinking of current, necessarily takes longer than positive going changes. In practice, this means that the circuit is quite fast when undergoing a transition from 3.3 V to 5 V, but the transition from 5 V to 3.3 V takes longer. Exactly how much longer is a function of the load resistance, R_L, seen at the output and the typical 1 µF value of C2. In general, a conservative transition time is approximately several milliseconds for load resistances in the range of 100 Ω to 1 kΩ. Note that for highest accuracy at the new output voltage, several time constants should be allowed (>7.6 time constants for <1/2 LSB error @ 10 bits, for example).

KELVIN CONNECTIONS

In many portable applications where the PC board cost and area go hand-in-hand, circuit interconnects are very often narrow. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. The interconnections of a circuit can exhibit a typical line resistance of 0.45 mΩ/square (1 oz. Cu, for example).

In applications where these devices are configured as low dropout voltage regulators, these wiring voltage drops can become a large source of error. To circumvent this problem, force and sense connections can be made to the reference through the use of an operational amplifier, as shown in Figure 29. This method provides a means by which the effects of wiring resistance voltage drops can be eliminated. Load currents flowing through wiring resistance produce an I-R error ($I_{LOAD} \times R_{WIRE}$) at the load. However, the Kelvin connection overcomes the problem by including the wiring resistance within the forcing loop of the op amp. Because the op amp senses the load voltage, op amp loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load. Depending on the reference device chosen, operational amplifiers that can be used in this application are the OP295, OP292, and OP183.

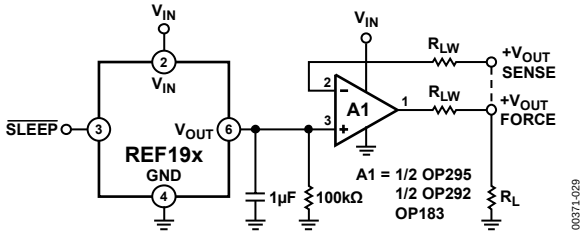


Figure 29. A Low Dropout, Kelvin-Connected Voltage Reference

FAIL-SAFE 5 V REFERENCE

Some critical applications require a reference voltage to be maintained at a constant voltage, even with a loss of primary power. The low standby power of the REF19x series and the switched output capability allow a fail-safe reference configuration to be implemented rather easily. This reference maintains a tight output voltage tolerance for either a primary power source (ac line derived) or a standby (battery derived) power source, automatically switching between the two as the power conditions change.

The circuit in Figure 30 illustrates this concept, which borrows from the switched output idea of Figure 28, again using the REF19x device family output wire-OR capability. In this case, since a constant 5 V reference voltage is desired for all conditions, two REF195 devices are used for U1 and U2, with their on/off switching controlled by the presence or absence of the primary dc supply source, V_S. V_{BAT} is a 6 V battery backup source that supplies power to the load only when V_S fails. For normal (V_S present) power conditions, V_{BAT} sees only the 15 µA (maximum) standby current drain of U1 in its off state.

In operation, it is assumed that for all conditions, either U1 or U2 is on, and a 5 V reference output is available. With this voltage constant, a scaled down version is applied to the Comparator IC U3, providing a fixed 0.5 V input to the negative input for all power conditions. The R1 to R2 divider provides a signal to the U3 positive input proportionally to V_S, which switches U3 and U1/U2, dependent upon the absolute level of V_S. In Figure 30, Op Amp U3 is configured as a comparator with hysteresis, which provides clean, noise-free output switching. This hysteresis is important to eliminate rapid switching at the threshold due to V_S ripple. Furthermore, the device chosen is the AD820, a rail-to-rail output device. This device provides HI and LO output states within a few mV of V_S, ground for accurate thresholds, and compatible drive for U2 for all V_S conditions. R3 provides positive feedback for circuit hysteresis, changing the threshold at the positive input as a function of the output of U3.

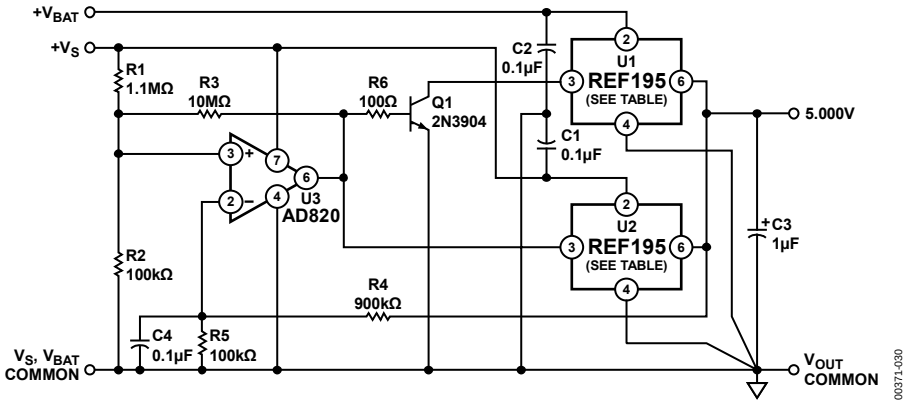


Figure 30. A Fail-Safe 5 V Reference

For V_S levels lower than the lower threshold, U3 output is low; thus, U2 and Q1 are off while U1 is on. For V_S levels higher than the upper threshold, the situation reverses, with U1 off and both U2 and Q1 on. In the interest of battery power conservation, all of the comparison switching circuitry is powered from V_S and is arranged so that when V_S fails, the default output comes from U1.

For the R1 to R3 values, as shown in Figure 30, lower/upper V_S switching thresholds are approximately 5.5 V and 6 V, respectively. These can be changed to suit other V_S supplies, as can the REF19x devices used for U1 and U2, over a range of 2.5 V to5 V of output. U3 can operate down to a V_S of 3.3 V, which is generally compatible with all REF19x family devices.

LOW POWER, STRAIN GAGE CIRCUIT

As shown in Figure 31, the REF19x family of references can be used in conjunction with low supply voltage operational amplifiers, such as the OP492 or the OP283, in a self-contained strain gage circuit in which the REF195 is used as the core. Other references can be easily accommodated by changing circuit element values. The references play a dual role, first as the voltage regulator to provide the supply voltage requirements of the strain gage and the operational amplifiers, and second as a precision voltage reference for the current source used to stimulate the bridge. A distinct feature of the circuit is that it can be remotely controlled on or off by digital means via the $\overline{\text{SLEEP}}$ pin.

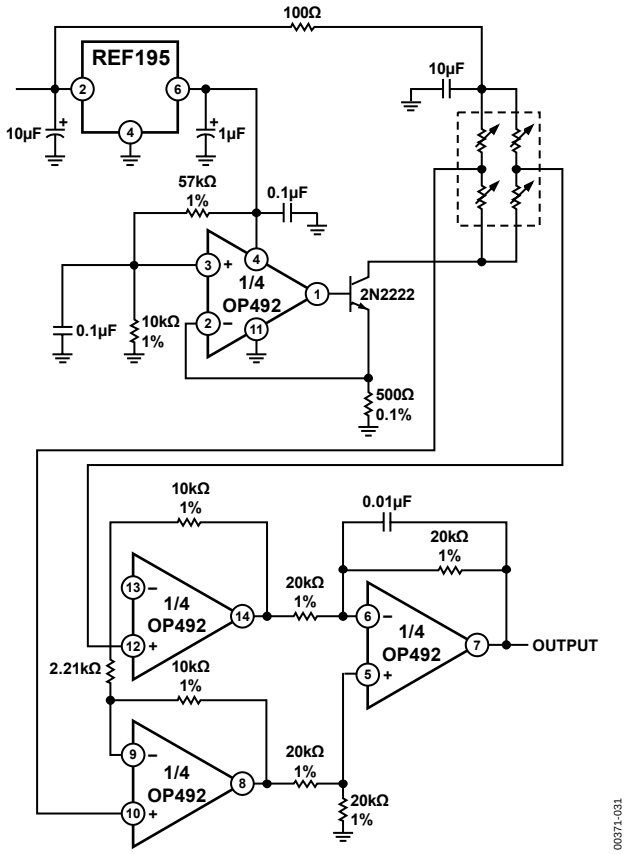
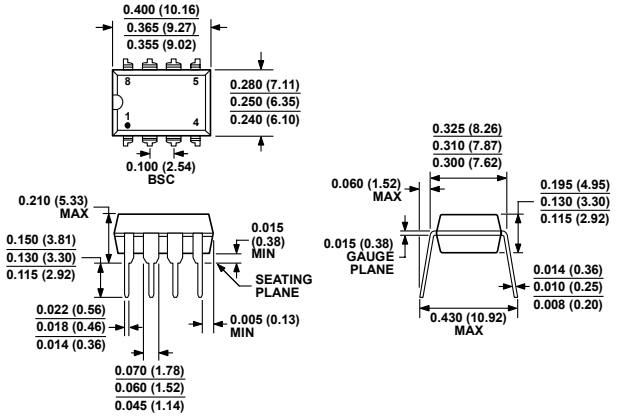


Figure 31. A Low Power, Strain Gage Circuit

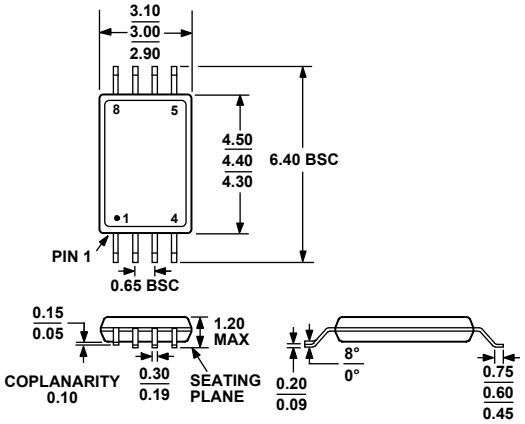
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

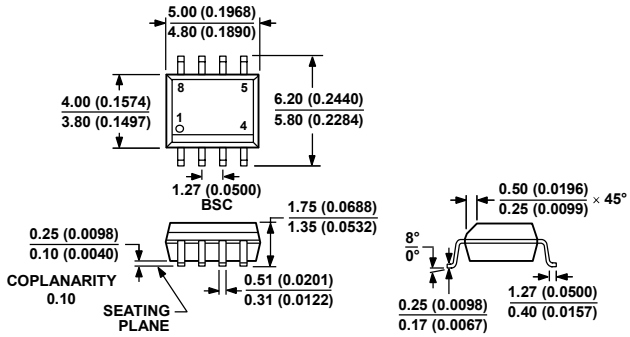
070606-A

Figure 32. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
P-Suffix
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-153-AA

Figure 33. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060506-A

Figure 34. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
S-Suffix
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Minimum Quantities/Reel
REF191ES	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF191ES-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF191ESZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF191ESZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF191GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF191GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF191GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF191GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF191GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF191GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192ES	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192ES-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192ES-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF192ESZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192ESZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192ESZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF192FS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192FS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192FS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF192FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192FSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF192GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF192GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF192GRU	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF192GRU-REEL7	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF192GRUZ[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF192GRUZ-REEL7[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF192GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF192GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF192GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF192GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF193GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF193GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF193GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF193GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF194ES	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194ES-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF194ESZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194ESZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF194FS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF194GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF194GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF194GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF194GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF194GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500

Model	Temperature Range	Package Description	Package Option	Minimum Quantities/Reel
REF194GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF195ES	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195ES-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195ESZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195ESZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195FS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195FS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF195GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF195GRU	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF195GRU-REEL7	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF195GRUZ[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF195GRUZ-REEL7[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF195GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF195GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF195GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF195GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF196GRU-REEL7	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF196GRUZ-REEL7[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF196GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF196GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF196GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF196GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF196GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF198ES	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198ES-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF198ESZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198ESZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF198ESZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	1000
REF198FS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198FS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF198FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF198GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF198GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)	
REF198GRU	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF198GRU-REEL7	−40°C to +85°C	8-Lead TSSOP	RU-8	1000
REF198GRUZ[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	
REF198GRUZ-REEL7[1]	−40°C to +85°C	8-Lead TSSOP	RU-8	2500
REF198GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500
REF198GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
REF198GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	2500

[1] Z = Pb-free part.

NOTES

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