SY54020R

Low Voltage 1.2V/1.8V/2.5V CML 1:4 Fanout Buffer with /EN and Fail-Safe Input 3.2Gbps, 2.5GHz

General Description

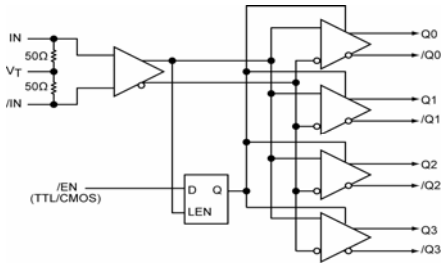
The SY54020R is a fully differential, low voltage 1.2V/1.8V/2.5V CML 1:4 Fanout Buffer with active-low Enable (/EN) and Fail-Safe Input (FSI). The Enable is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. When this device is used as a clock fanout, disabling the downstream clock may reduce system power. FSI is a special circuit designed to sense the amplitude of the input signal and to latch the output when an invalid or no signal is present at the input. The SY54020R can process clock signals up to 2.5 GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals as small as 100mV ($200mV_{pp}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V_T pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 100ps.

The SY54020R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (–40°C to +85°C).

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge®

Features

- 1.2V/1.8V/2.5V CML 1:4 Fanout Buffer with FSI
- Active-low Enable (/EN) input to disable the outputs
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 3.2Gbps Data throughput
  - DC-to > 2.5GHz Clock throughput
  - <400 ps propagation delay (IN-to-Q)
  - <20ps within-device skew
  - <100 ps rise/fall times
- Ultra-low jitter design
  - $<1ps_{RMS}$ cycle-to-cycle jitter
- High-speed CML outputs
- 2.5V ±5% V_{CC} , 1.2/1.8V/2.5V ±5% V_{CCO} power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) MLF® package

Applications

- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology.

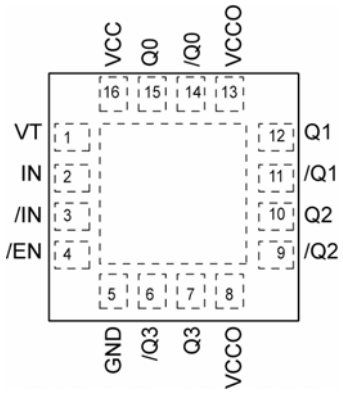
Ordering Information [1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY54020RMG	MLF-16	Industrial	020R with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY54020RMGTR[2]	MLF-16	Industrial	020R with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin MLF® (MLF-16)

Pin Description

Pin Number	Pin Name	Pin Function
2,3	IN, /IN	Differential Input: This input pair is the differential signal input to the device. It accepts differential signals as small as 100mV (200mV$_{PP}$). Each input pin internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail-Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. Please refer to the "Interface Applications" section for more details.
1	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC coupling. For AC coupling, bypass VT with 0.1µF low ESR capacitor to VCC. See "Interface Applications" subsection and Figure 2a.
4	/EN	Single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. The input -switching threshold is Vcc/2. Note that this input is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state (Enabled) if left open. Outputs are disabled when /EN is high. See Figure 1b for more details.
16	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CC} pin as possible. Supplies input and core circuitry.
8,13	VCCO	Output Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CCO} pin as possible. Supplies the output buffers.
5	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
15,14 12,11 10,9 7,6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	CML Differential Output Pairs: Differential buffered copy of the input signal. The output swing is typically 380mV. See "Interface Applications" subsection for termination information.

Truth Table

IN	/IN	/EN	Q	/Q
0	1	0	0	1
1	0	0	1	0
X	X	1	0(1)	1(1)

Note:

1. See timing diagram, Figure 1b.

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +3.0V
Supply Voltage (V_{CCO}) ..... –0.5V to +2.7V
V_{CC} - V_{CCO} ..... <1.8V
V_{CCO} - V_{CC} ..... <0.5V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.5V
CML Output Voltage (V_{OUT}) ..... 0.6V to V_{CCO}+0.5V
Current (V_T)
Source or sink current on VT pin ..... ±100mA
Input Current
Source or sink current on (IN, /IN) ..... ±50mA
Maximum operating Junction Temperature ..... 125°C
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 2.375V to 2.625V
(V_{CCO}) ..... 1.14V to 2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF®
Still-air (θ_{JA}) ..... 75°C/W
Junction-to-board (ψ_{JB}) ..... 33°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range	V_{CC}	2.375	2.5	2.625	V
		V_{CCO}	1.14	1.2	1.26	V
		V_{CCO}	1.7	1.8	1.9	V
		V_{CCO}	2.375	2.5	2.625	V
I_{CC}	Power Supply Current	Max. V_{CC}		42	58	mA
I_{CCO}	Power Supply Current	No Load. V_{CCO}		64	84	mA
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	Min. V_{IL} with V_{IH} = 1.2V	0.2		V_{IH}–0.1	V
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.14		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	V_{IL} with V_{IH} = 1.14V, (1.2V-5%)	0.66		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	see Figure 3a	0.1		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	see Figure 3b	0.2		2.0	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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CML Outputs DC Electrical Characteristics [5]

V_{CCO} = 1.14V to 1.26V, R_L = 50Ω to $V_{CCO,}$
V_{CCO} = 1.7V to 1.9V; 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CCO}	V_{CCO}-0.020	V_{CCO}-0.010	V_{CCO}	V
V_{OUT}	Output Voltage Swing	See Figure 3a	300	390	475	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	600	780	950	mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

LVTTL/CMOS DC Electrical Characteristics [5]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{CC}			200	µA
I_{IL}	Input LOW Current	V_{IL} = 0V	-5		75	µA

Note:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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AC Electrical Characteristics

V_{CCO} = 1.14V to 1.26V, R_L = 50Ω to V_{CCO}
V_{CCO} = 1.7V to 1.9V, 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs.
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Data Rate/ Frequency	NRZ Data	3.2			Gbps
		V_{OUT} > 200mV clock	2.5			GHz
t_{PD}	Propagation Delay IN-to-Q	V_{IN} > 200mV Note 6, Fig. 1a	200	300	400	ps
		V_{IN}: 100mV -200mV, Note 6, Fig. 1a	240	360	490	
t_S	Setup Time /EN			150		ps
t_H	Hold Time /EN			250		ps
t_{SKEW}	Output-to-Output skew	Note 7		5	20	ps
	Part-to-Part Skew	Note 8			75	ps
t_{Jitter}	Data Random Jitter	Note 9			1	ps_{RMS}
	Deterministic Jitter	Note 10			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	Note 11			1	ps_{RMS}
	Total Jitter	Note 12			10	ps_{PP}
t_R, t_F	Output Rise/Fall Times (20% to 80%)	Input <300mV	35	60	100	ps
	Duty Cycle	Differential I/O ≤2.5GHz	47		53	%

Notes:

6. Propagation delay is measured with input tr/tf ≤ 300ps (20 to 80%)
7. Output-to-Output skew is the difference in time between both outputs, receiving data from the same input, for the same temperature, voltage and transition.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges of the respective inputs.
9. Random jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.
10. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
11. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
12. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input of this device has a built-in FSI circuit that senses the input amplitude and latches the output when the input signal is not present or when its amplitude drops below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of the SY54020R is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low input signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal close to the FSI threshold. Due to the FSI function, the propagation delay will depend upon rise and fall time of the input signal and on its amplitude. Refer to “Typical Characteristics” for detailed information.

Interface Applications

For Input Interface Applications, see Figures 4a through 4f. For CML Output Termination, see Figures 5a through 5d.

CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ω to1.2V, DC-coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω to 1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC-couple with internally terminated receiver, such as 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation. Any unused output pair needs to be terminated when VCCO is 1.2V, do not leave floating.

CML Output Termination with VCCO 1.8V, 2.5V

For VCCO of 1.8V and 2.5V, Figure 5a and Figure 5b, terminate with either 50Ω to VCCO or 100Ω differentially across the outputs. See Figure 5c for AC-coupling.

Input AC-Coupling

The SY54020R input can accept AC-coupling from any driver. Bypass VT with a 0.1µF low ESR capacitor to VCC, as shown in Figures 4c and 4d. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

Timing Diagrams

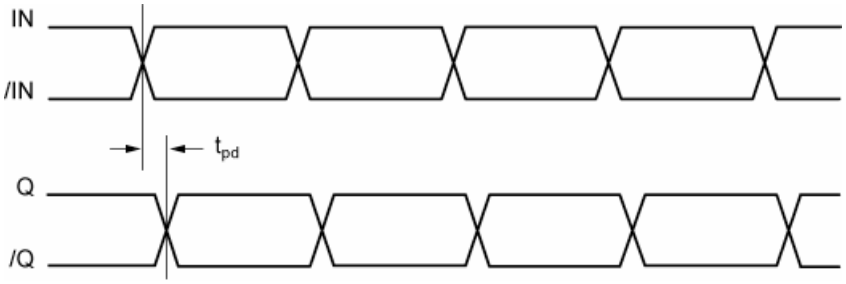


Figure 1a. Propagation Delay

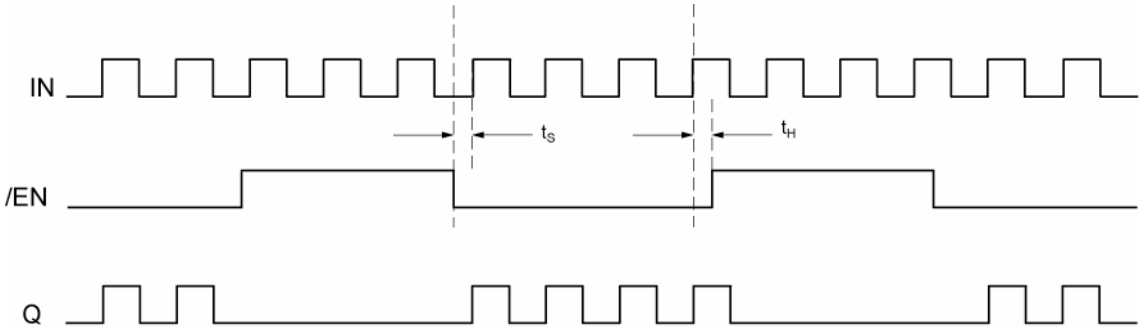


Figure 1b. Output Enable/Disable Timing

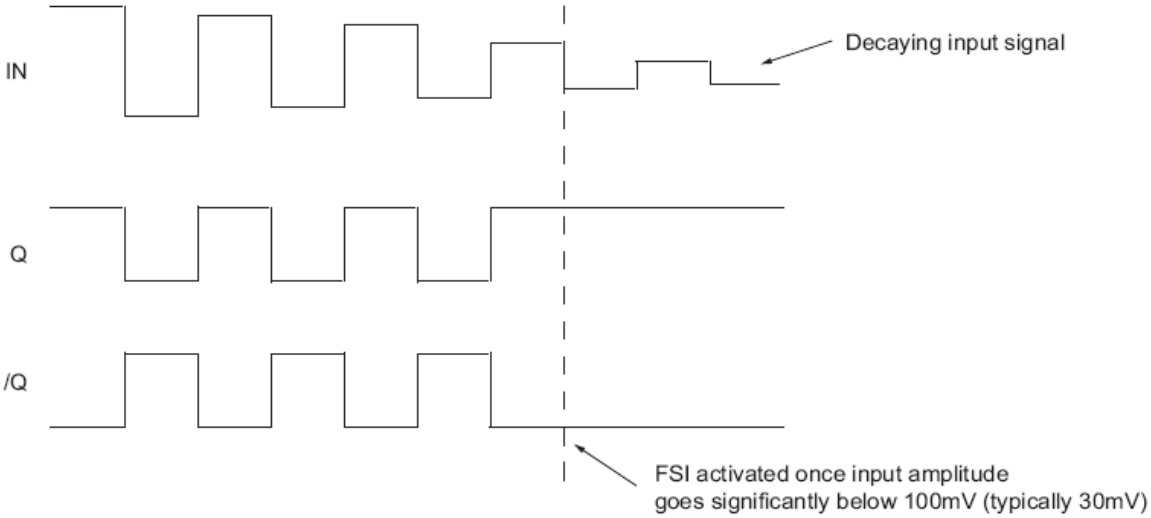


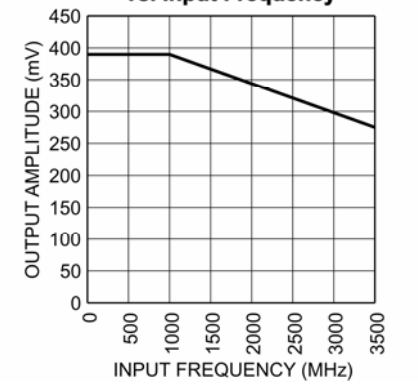
Figure 1c. Fail-Safe Feature

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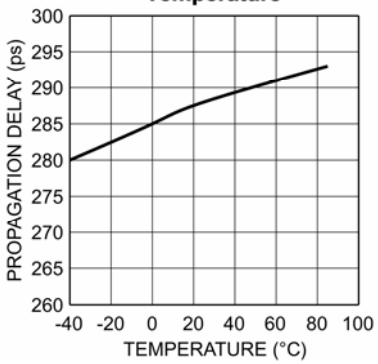
Typical Characteristics

V_{CC} = 2.5V, V_{CCO} = 1.2V GND = 0V, V_{IN} = 400mV, R_L = 50Ω to 1.2V, T_A = 25°C, unless otherwise stated.

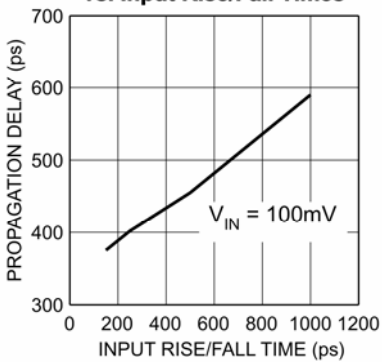
Output Amplitude vs. Input Frequency



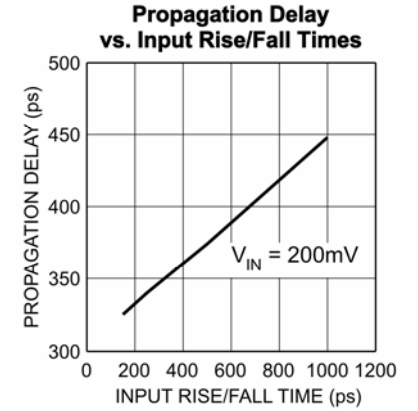
Propagation Delay vs. Temperature



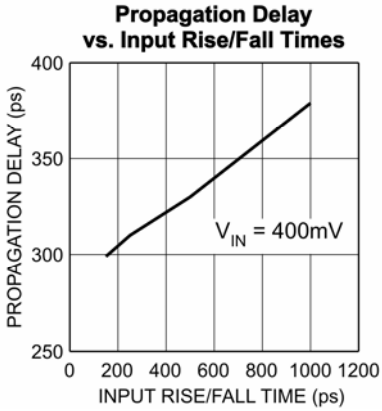
Propagation Delay vs. Input Rise/Fall Times



Propagation Delay vs. Input Rise/Fall Times



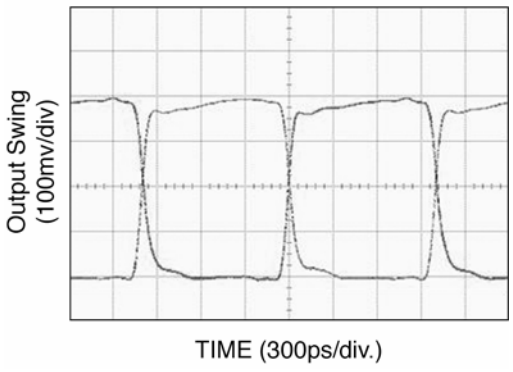
Propagation Delay vs. Input Rise/Fall Times



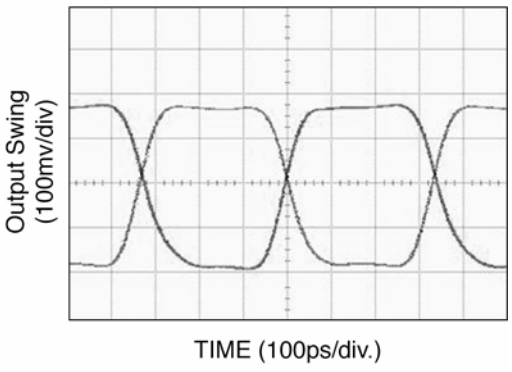
Functional Characteristics

V_{CC} = 2.5V, V_{CCO} =1.2V GND = 0V, V_{IN} = 400mV, R_L = 50Ω to 1.2V, T_A = 25°C, unless otherwise stated.

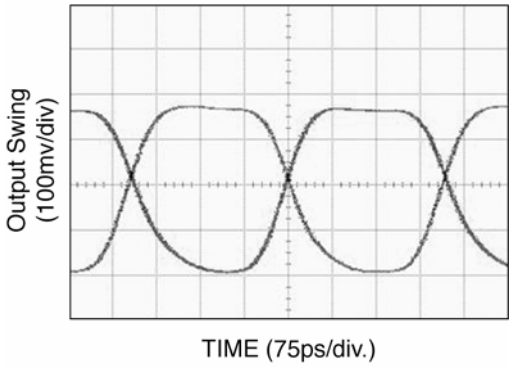
500MHz Output



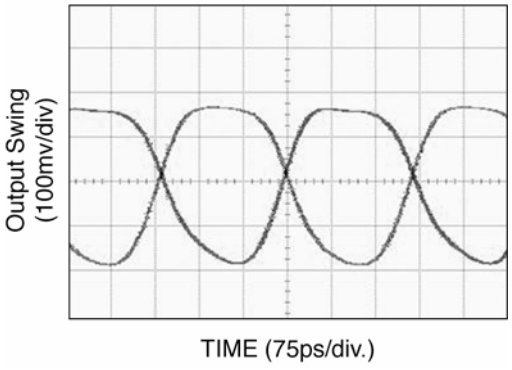
1.5GHz Output



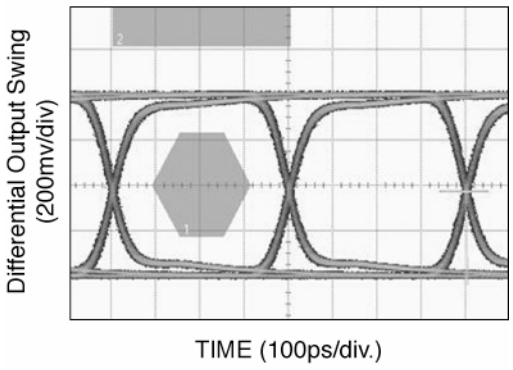
2GHz Output



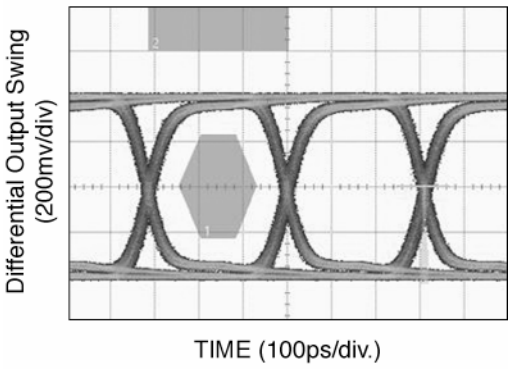
2.5GHz Output



2.5Gbps Output



3.2Gbps Output



Input and Output Stage

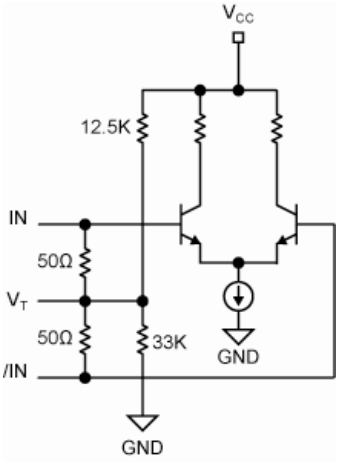


Figure 2a. Simplified Differential Input Buffer

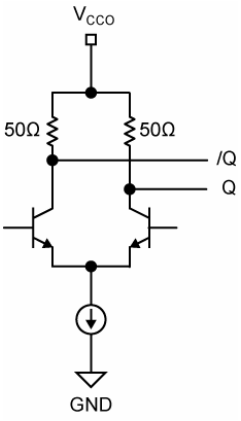


Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings



Figure 3a. Single-Ended Swing

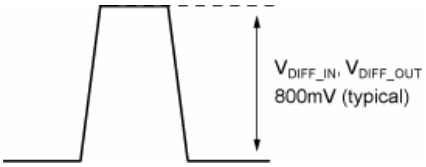


Figure 3b. Differential Swing

Input Interface Applications

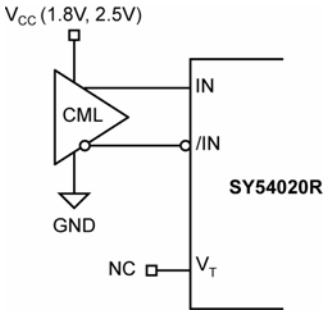


Figure 4a. CML Interface (DC-Coupled, 1.8V, 2.5V)

Option: may connect V_T to V_{CC}

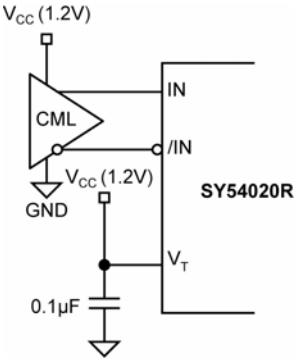


Figure 4b. CML Interface (DC-Coupled, 1.2V)

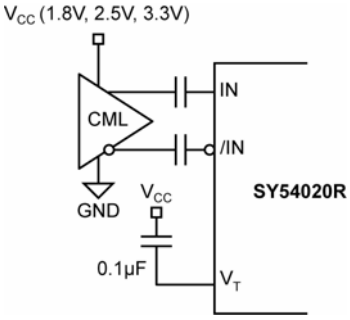


Figure 4c. CML Interface (AC-Coupled)

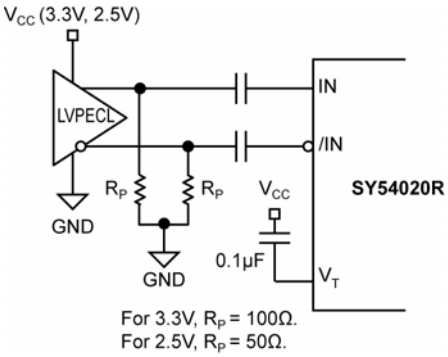


Figure 4d. LVPECL Interface (AC-Coupled)

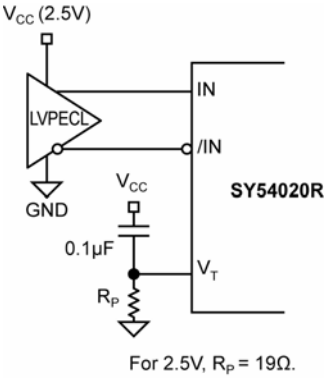


Figure 4e. LVPECL Interface (DC-Coupled)

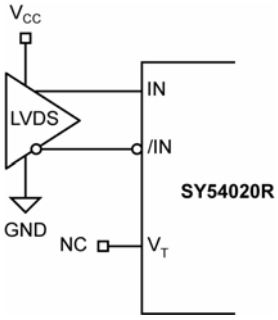


Figure 4f. LVDS Interface

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CML Output Termination

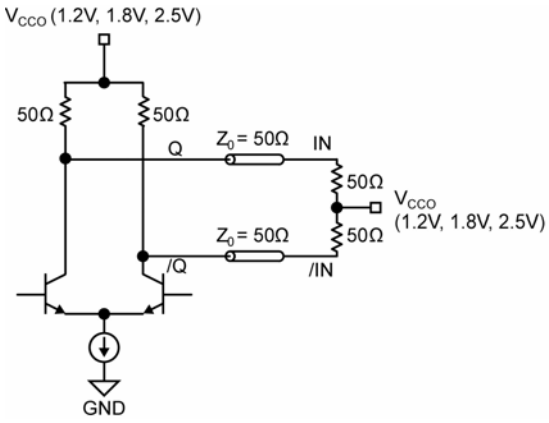


Figure 5a. 1.2V, 1.8V or 2.5V CML DC-Coupled Termination

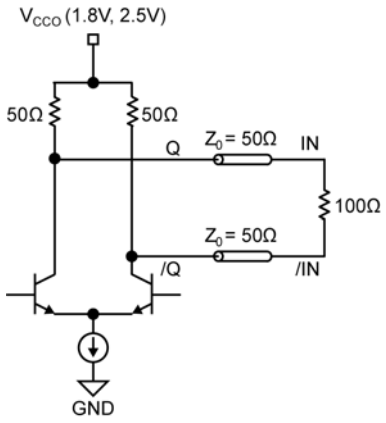


Figure 5b. 1.8V or 2.5V CML DC-Coupled Termination

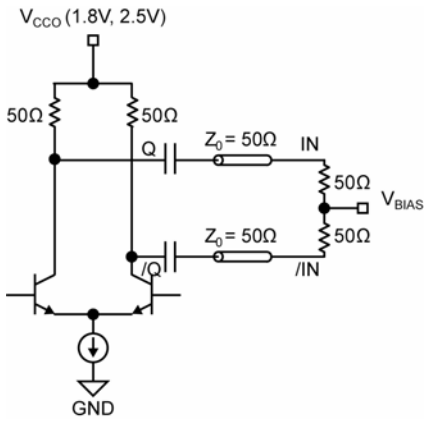


Figure 5c. CML AC-Coupled Termination (V_{CCO} 1.8V or 2.5V)

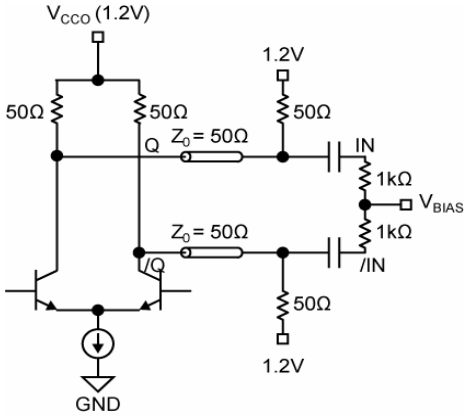
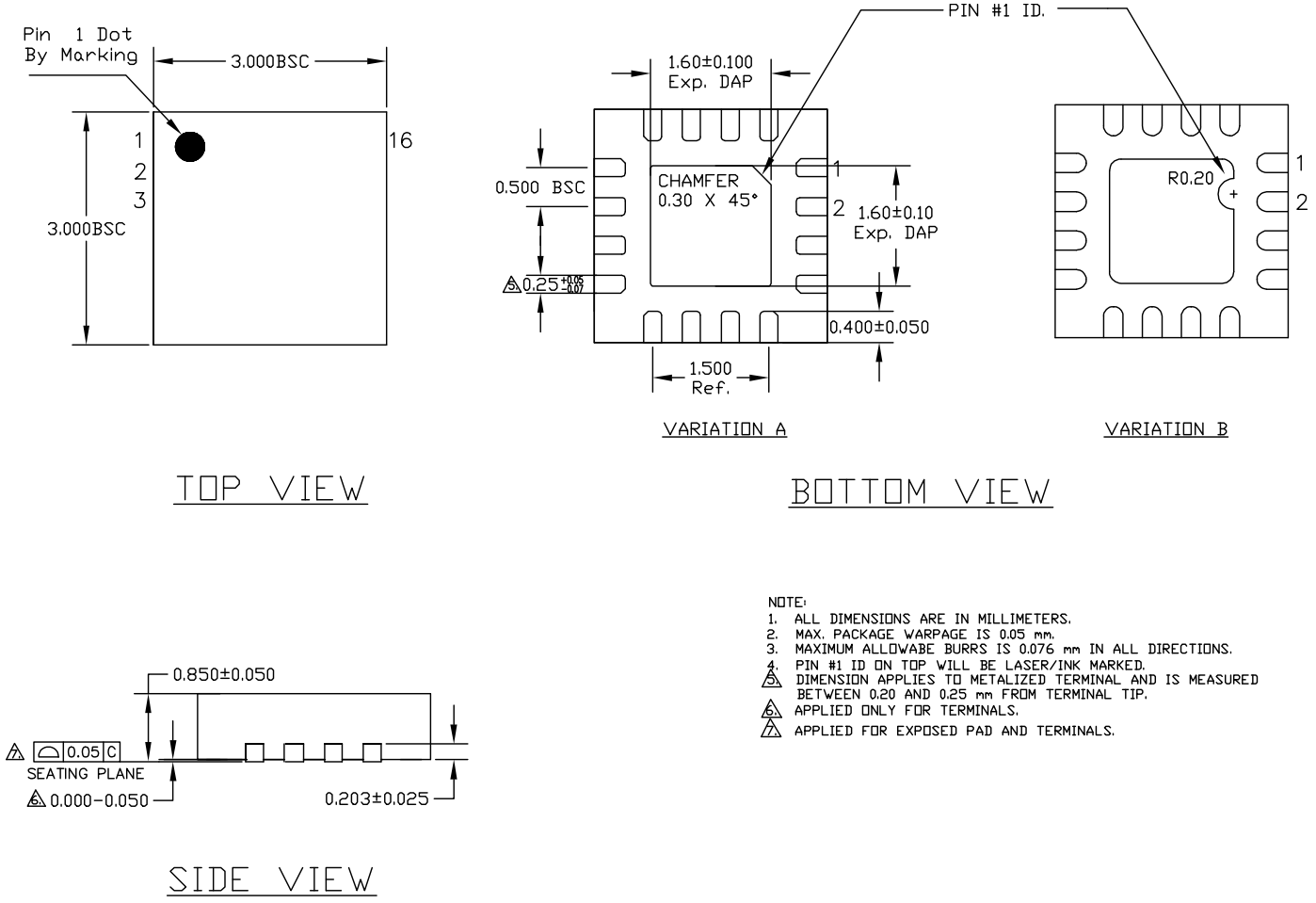


Figure 5d. CML AC-Coupled Termination (V_{CCO} 1.2V only)

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Package Information



16-Pin MLF® (3mm x3mm) (MLF-16)

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