High Performance Narrow-Band Transceiver IC

ADF7021

FEATURES

- Low power, narrow-band transceiver
- Frequency bands using dual VCO
  - 80 MHz to 650 MHz
  - 862 MHz to 950 MHz
- Modulation schemes
  - 2FSK, 3FSK, 4FSK, MSK
- Spectral shaping
  - Gaussian and raised cosine filtering
- Data rates supported
  - 0.05 kbps to 32.8 kbps
- 2.3 V to 3.6 V power supply
- Programmable output power
  - −16 dBm to +13 dBm in 63 steps
- Automatic PA ramp control
- Receiver sensitivity
  - −130 dBm at 100 bps, 2FSK
  - −122 dBm at 1 kbps, 2FSK
  - −113 dBm at 25 kbps, raised cosine 2FSK
- Patent pending, on-chip image rejection calibration
- On-chip VCO and fractional-N PLL
- On-chip, 7-bit ADC and temperature sensor
- Fully automatic frequency control loop (AFC)
- Digital received signal strength indication (RSSI)
- Integrated Tx/Rx switch
- 0.1 µA leakage current in power-down mode

APPLICATIONS

- Narrow-band standards
  - ETSI EN 300 220, FCC Part 15, FCC Part 90, FCC Part 95, ARIB STD-T67
- Low cost, wireless data transfer
- Remote control/security systems
- Wireless metering
- Private mobile radio
- Wireless medical telemetry service (WMTS)
- Keyless entry
- Home automation
- Process and building control
- Pagers

FUNCTIONAL BLOCK DIAGRAM

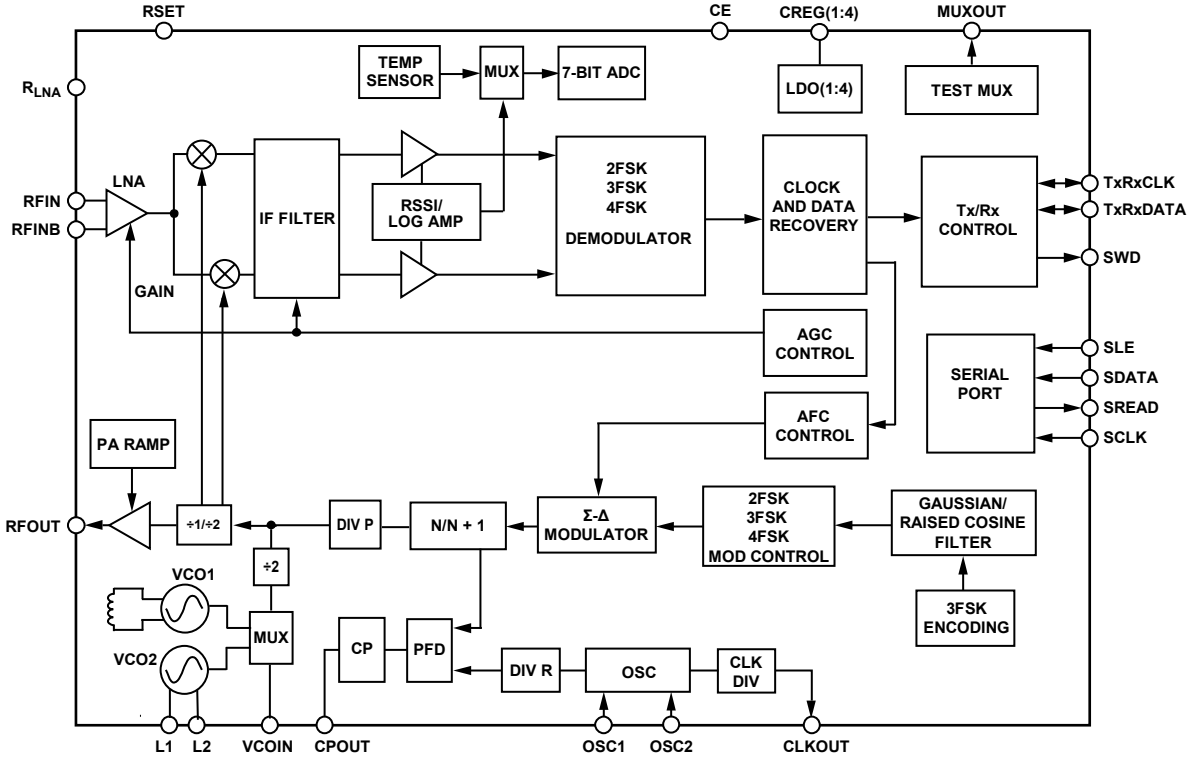


Figure 1.

Rev. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

9/07—Rev. 0 to Rev. A

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3/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7021 is a high performance, low power, highly integrated 2FSK/3FSK/4FSK transceiver. It is designed to operate in the narrow-band, license-free ISM bands, and in the licensed bands with frequency ranges of 80 MHz to 650 MHz and 862 MHz to 950 MHz. The part has both Gaussian and raised cosine transmit data filtering options to improve spectral efficiency for narrow-band applications. It is suitable for circuit applications targeted at European ETSI EN 300 220, the Japanese ARIB STD-T67, the Chinese short range device regulations, and the North American FCC Part 15, Part 90, and Part 95 regulatory standards. A complete transceiver can be built using a small number of external discrete components, making the ADF7021 very suitable for price sensitive and area sensitive applications.

The range of on-chip FSK modulation and data filtering options allows users greater flexibility in their choice of modulation schemes while meeting tight spectral efficiency requirements. The ADF7021 also supports protocols that dynamically switch between 2FSK/3FSK/4FSK to maximize communication range and data throughput.

The transmit section contains dual voltage controlled oscillators (VCOs) and a low noise fractional-N PLL with an output resolution of <1 ppm. The ADF7021 has a VCO using an internal LC tank (431 MHz to 475 MHz, 862 MHz to 950 MHz) and a VCO using an external inductor as part of its tank circuit (80 MHz to 650 MHz). The dual VCO design allows dual-band operation where the user can transmit and/or receive at any frequency supported by the internal inductor VCO and can also transmit and/or receive at a particular frequency band supported by the external inductor VCO.

The frequency agile PLL allows the ADF7021 to be used in frequency hopping spread spectrum (FHSS) systems.

Both VCOs operate at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 63 steps from −16 dBm to +13 dBm, and has an automatic power ramp control to prevent spectral splatter and help meet regulatory standards. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (100 kHz), which minimizes power consumption and the external component count, yet avoids dc offset and flicker noise at low frequencies. The IF filter has programmable bandwidths of 12.5 kHz, 18.75 kHz, and 25 kHz. The ADF7021 supports a wide variety of programmable features including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patent-pending automatic frequency control (AFC) loop with programmable pull-in range that allows the PLL to track out the frequency error in the incoming signal.

The receiver achieves an image rejection performance of 56 dB using a patent-pending IR calibration scheme that does not require the use of an external RF source.

An on-chip ADC provides readback of the integrated temperature sensor, external analog input, battery voltage, and RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±10°C over the full operating temperature range of −40°C to +85°C. This accuracy can be improved by performing a 1-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C. All measurements are performed with the EVAL-ADF7021DBx using the PN9 data sequence, unless otherwise noted.

RF AND PLL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					See Table 9 for required VCO_BIAS and VCO_ADJUST settings
Frequency Ranges (Direct Output)	160		650	MHz	External inductor VCO
	862		950	MHz	Internal inductor VCO
Frequency Ranges (RF Divide-by-2 Mode)	80		325	MHz	External inductor VCO, RF divide-by-2 enabled
	431		475	MHz	Internal inductor VCO, RF divide-by-2 enabled
Phase Frequency Detector (PFD) Frequency[1]	RF/256		26/30	MHz	Crystal reference/external reference
PHASE-LOCKED LOOP (PLL)					
VCO Gain[2]					
868 MHz, Internal Inductor VCO		58		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 8
434 MHz, Internal Inductor VCO		29		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 8
426 MHz, External Inductor VCO		27		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 3
160 MHz, External Inductor VCO		6		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 2
Phase Noise (In-Band)					
868 MHz, Internal Inductor VCO		−97		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
433 MHz, Internal Inductor VCO		−103		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
426 MHz, External Inductor VCO		−95		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 9.84 MHz, VCO_BIAS = 3
Phase Noise (Out-of-Band)		−124		dBc/Hz	1 MHz offset, f_{RF} = 433 MHz, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
Normalized In-Band Phase Noise Floor[3]		−203		dBc/Hz	
PLL Settling		40		µs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 19.68 MHz, loop bandwidth (LBW) = 100 kHz
REFERENCE INPUT					
Crystal Reference[4]	3.625		26	MHz	
External Oscillator[4, 5]	3.625		30	MHz	
Crystal Start-Up Time[6]					
XTAL Bias = 20 µA		0.930		ms	10 MHz XTAL, 33 pF load capacitors, V_{DD} = 3.0 V
XTAL Bias = 35 µA		0.438		ms	10 MHz XTAL, 33 pF load capacitors, V_{DD} = 3.0 V
Input Level for External Oscillator[7]					
OSC1		0.8		V p-p	Clipped sine wave
OSC2		CMOS levels		V	
ADC PARAMETERS					
INL		±0.4		LSB	V_{DD} = 2.3 V to 3.6 V, T_A = 25°C
DNL		±0.4		LSB	V_{DD} = 2.3 V to 3.6 V, T_A = 25°C

[1] The maximum usable PFD at a particular RF frequency is limited by the minimum N divide value.
[2] VCO gain measured at a VCO tuning voltage of 1 V. The VCO gain varies across the tuning range of the VCO. The software package ADIsimPLL™ can be used to model this variation.
[3] This value can be used to calculate the in-band phase noise for any operating frequency. Use the following equation to calculate the in-band phase noise performance as seen at the PA output: $-203 + 10\log(f_{PFD}) + 20\log N$.
[4] Guaranteed by design. Sample tested to ensure compliance.
[5] A TCXO, VCXO, or OCXO can be used as an external oscillator.
[6] Crystal start-up time is the time from chip enable (CE) being asserted to correct clock frequency on the CLKOUT pin.
[7] Refer to the Reference Input section for details on using an external oscillator.

TRANSMISSION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					
2FSK, 3FSK	0.05		25[1]	kbps	IF_BW = 25 kHz
4FSK	0.05		32.8[2]	kbps	IF_BW = 25 kHz
MODULATION					
Frequency Deviation (f_{DEV})[3]	0.056		28.26	kHz	PFD = 3.625 MHz
	0.306		156	kHz	PFD = 20 MHz
Deviation Frequency Resolution	56			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Raised Cosine Filter Alpha		0.5/0.7			Programmable
TRANSMIT POWER					
Maximum Transmit Power[4]		+13		dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temperature		±1		dB	−40°C to +85°C
Transmit Power Variation vs. V_{DD}		±1		dB	2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	902 MHz to 928 MHz, 3 V, T_A = 25°C
Programmable Step Size		0.3125		dB	−20 dBm to +13 dBm
ADJACENT CHANNEL POWER (ACP)					
426 MHz, External Inductor VCO					PFD = 9.84 MHz
12.5 kHz Channel Spacing		−50		dBc	Gaussian 2FSK modulation, measured in a ±4.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ARIB STD-T67
25 kHz Channel Spacing		−50		dBc	Gaussian 2FSK modulation, measured in a ±8 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ARIB STD-T67
868 MHz, Internal Inductor VCO					PFD = 19.68 MHz
12.5 kHz Channel Spacing		−46		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±6.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ETSI EN 300-220
25 kHz Channel Spacing		−43		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±12.5 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ETSI EN 300-220
433 MHz, Internal Inductor VCO					PFD = 19.68 MHz
12.5 kHz Channel Spacing		−50		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±6.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ETSI EN 300-220
25 kHz Channel Spacing		−47		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±12.5 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ETSI EN 300-220
OCCUPIED BANDWIDTH					99.0% of total mean power; 12.5 kHz channel spacing (2.4 kbps PN9 data, 1.2 kHz frequency deviation); 25 kHz channel spacing (9.6 kbps PN9 data, 2.4 kHz frequency deviation)
2FSK Gaussian Data Filtering					
12.5 kHz Channel Spacing		3.9		kHz	
25 kHz Channel Spacing		9.9		kHz	
2FSK Raised Cosine Data Filtering					
12.5 kHz Channel Spacing		4.4		kHz	
25 kHz Channel Spacing		10.2		kHz	
3FSK Raised Cosine Filtering					
12.5 kHz Channel Spacing		3.9		kHz	
25 kHz Channel Spacing		9.5		kHz	
4FSK Raised Cosine Filtering					19.2 kbps PN9 data, 1.2 kHz frequency deviation
25 kHz Channel Spacing		13.2		kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS EMISSIONS					
Reference Spurs		−65		dBc	100 kHz loop bandwidth
HARMONICS[5]					13 dBm output power, unfiltered conductive/filtered conductive
Second Harmonic		−35/−52		dBc	
Third Harmonic		−43/−60		dBc	
All Other Harmonics		−36/−65		dBc	
OPTIMUM PA LOAD IMPEDANCE[6]					
f_{RF} = 915 MHz		39 + j61		Ω	
f_{RF} = 868 MHz		48 + j54		Ω	
f_{RF} = 450 MHz		98 + j65		Ω	
f_{RF} = 426 MHz		100 + j65		Ω	
f_{RF} = 315 MHz		129 + j63		Ω	
f_{RF} = 175 MHz		173 + j49		Ω	

[1] Using Gaussian or raised cosine filtering. The frequency deviation should be chosen to ensure that the transmit occupied signal bandwidth is within the receiver IF filter bandwidth.
[2] Using raised cosine filtering with an alpha = 0.7. The inner frequency deviation = 1.78 kHz, and the POST_DEMOD_BW = 24.6 kHz.
[3] For the definition of frequency deviation, refer to the Register 2—Transmit Modulation Register section.
[4] Measured as maximum unmodulated power.
[5] Conductive filtered harmonic emissions measured on the EVAL-ADF7021DBx, which includes a T-stage harmonic filter (two inductors and one capacitor).
[6] For matching details, refer to the LNA/PA Matching section.

RECEIVER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY					Bit error rate (BER) = 10^{-3}, low noise amplifier (LNA) and power amplifier (PA) matched separately
2FSK					
Sensitivity at 0.1 kbps		−130		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−122		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−115		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−110		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
Gaussian 2FSK					
Sensitivity at 0.1 kbps		−129		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−121		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−111		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
GMSK					
Sensitivity at 9.6 kbps		−113		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Raised Cosine 2FSK					
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−121		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−113		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
3FSK					
Sensitivity at 9.6 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 18.75 kHz, Viterbi detection on
Raised Cosine 3FSK					
Sensitivity at 9.6 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 12.5 kHz, alpha = 0.5, Viterbi detection on
Sensitivity at 19.6 kbps		−106		dBm	f_{DEV} = 4.8 kHz, high sensitivity mode, IF_BW = 18.75 kHz, alpha = 0.5, Viterbi detection on
4FSK					
Sensitivity at 9.6 kbps		−112		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 19.6 kbps		−107		dBm	f_{DEV} (inner) = 2.4 kHz, high sensitivity mode, IF_BW = 25 kHz
Raised Cosine 4FSK					
Sensitivity at 9.6 kbps		−109		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 12.5 kHz, alpha = 0.5
Sensitivity at 19.2 kbps		−103		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 18.75 kHz, alpha = 0.5
Sensitivity at 32.8 kbps		−100		dBm	f_{DEV} (inner) = 1.8 kHz, high sensitivity mode, IF_BW = 25 kHz, alpha = 0.7
INPUT IP3					Two-tone test, f_{LO} = 860 MHz, F1 = f_{LO} + 100 kHz, F2 = f_{LO} − 800 kHz
Low Gain Enhanced Linearity Mode		−3		dBm	LNA_GAIN = 3, MIXER_LINEARITY = 1
Medium Gain Mode		−13.5		dBm	LNA_GAIN = 10, MIXER_LINEARITY = 0
High Sensitivity Mode		−24		dBm	LNA_GAIN = 30, MIXER_LINEARITY = 0

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADJACENT CHANNEL REJECTION					
868 MHz					Wanted signal is 3 dB above the sensitivity point (BER = 10^{-3}); unmodulated interferer is at the center of the adjacent channel; rejection measured as the difference between interferer level and wanted signal level in dB
12.5 kHz Channel Spacing		25		dB	12.5 kHz IF_BW
25 kHz Channel Spacing		27		dB	25 kHz IF_BW
25 kHz Channel Spacing		39		dB	18 kHz IF_BW
426 MHz, External Inductor VCO					Wanted signal 3 dB above reference sensitivity point (BER = 10^{-2}); modulated interferer (1 kHz sine, ±2 kHz deviation) at the center of the adjacent channel; rejection measured as the difference between interferer level and reference sensitivity level in dB
12.5 kHz Channel Spacing		25		dB	12.5 kHz IF_BW
25 kHz Channel Spacing		30		dB	25 kHz IF_BW
25 kHz Channel Spacing		41		dB	18 kHz IF_BW, compliant with ARIB STD-T67
CO-CHANNEL REJECTION					Wanted signal (2FSK, 9.6 kbps, ±4 kHz deviation) is 10 dB above the sensitivity point (BER = 10^{-3}), modulated interferer
868 MHz		−3		dB	
IMAGE CHANNEL REJECTION					Wanted signal (2FSK, 9.6 kbps, ±4 kHz deviation) is 10 dB above the sensitivity point (BER = 10^{-3}); modulated interferer (2FSK, 9.6 kbps, ±4 kHz deviation) is placed at the image frequency of f_{RF} − 200 kHz; interferer level is increased until BER = 10^{-3}
900 MHz		23/39		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
450 MHz		29/50		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
450 MHz, External Inductor VCO		38/53		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
BLOCKING					Wanted signal is 10 dB above the input sensitivity level; CW interferer level is increased until BER = 10^{-3}
±1 MHz		69		dB	
±2 MHz		75		dB	
±5 MHz		78		dB	
±10 MHz		78.5		dB	
SATURATION (MAXIMUM INPUT LEVEL)		12		dBm	2FSK mode, BER = 10^{-3}
RSSI					
Range at Input[2]		−120 to −47		dBm	
Linearity		±2		dB	Input power range = −100 dBm to −47 dBm
Absolute Accuracy		±3		dB	Input power range = −100 dBm to −47 dBm
Response Time		300		µs	See the RSSI/AGC section
AFC					
Pull-In Range	0.5		1.5 × IF_BW	kHz	The range is programmable, R10_DB[24:31]
Response Time		48		Bits	
Accuracy		0.5		kHz	Input power range = −100 dBm to +12 dBm
Rx SPURIOUS EMISSIONS[3]					
Internal Inductor VCO		−91/−91		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
		−52/−70		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive
External Inductor VCO		−62/−72		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
		−64/−85		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LNA INPUT IMPEDANCE					RFIN to RFGND
f_{RF} = 915 MHz		24 – j60		Ω	
f_{RF} = 868 MHz		26 – j63		Ω	
f_{RF} = 450 MHz		63 – j129		Ω	
f_{RF} = 426 MHz		68 – j134		Ω	
f_{RF} = 315 MHz		96 – j160		Ω	
f_{RF} = 175 MHz		178 – j190		Ω	

[1] Calibration of the image rejection used an external RF source.
[2] For received signal levels < −100 dBm, it is recommended to average the RSSI readback value over a number of samples to improve the RSSI accuracy at low input powers.
[3] Filtered conductive receive spurious emissions measured on the EVAL-ADF7021DBx, which includes a T-stage harmonic filter (two inductors and one capacitor).

DIGITAL SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIMING INFORMATION					
Chip Enabled to Regulator Ready		10		µs	C_{REG} = 100 nF
Chip Enabled to Tx Mode					32-bit register write time = 50 µs
TCXO Reference		1		ms	
XTAL		2		ms	
Chip Enabled to Rx Mode					32-bit register write time = 50 µs, IF filter coarse calibration only
TCXO Reference		1.2		ms	
XTAL		2.2		ms	
Tx to Rx Turnaround Time		300 µs + (5 × t_{BIT})			Time to synchronized data out, includes AGC settling and CDR synchronization; see AGC Information and Timing section for more details; t_{BIT} = data bit period
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DD}			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} – 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLKOUT Rise/Fall			5	ns	
CLKOUT Load			10	pF	

GENERAL SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE (T_A)	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply, V_{DD}	2.3		3.6	V	All VDD pins must be tied together
TRANSMIT CURRENT CONSUMPTION[1]					V_{DD} = 3.0 V, PA is matched into 50 Ω
868 MHz					VCO_BIAS = 8
0 dBm		20.2		mA	
5 dBm		24.7		mA	
10 dBm		32.3		mA	
450 MHz, Internal Inductor VCO					VCO_BIAS = 8
0 dBm		19.9		mA	
5 dBm		23.2		mA	
10 dBm		29.2		mA	
426 MHz, External Inductor VCO					VCO_BIAS = 2
0 dBm		13.5		mA	
5 dBm		17		mA	
10 dBm		23.3		mA	
RECEIVE CURRENT CONSUMPTION					V_{DD} = 3.0 V
868 MHz					VCO_BIAS = 8
Low Current Mode		22.7		mA	
High Sensitivity Mode		24.6		mA	
433MHz, Internal Inductor VCO					VCO_BIAS = 8
Low Current Mode		24.5		mA	
High Sensitivity Mode		26.4		mA	
426 MHz, External Inductor VCO					VCO_BIAS = 2
Low Current Mode		17.5		mA	
High Sensitivity Mode		19.5		mA	
POWER-DOWN CURRENT CONSUMPTION					
Low Power Sleep Mode		0.1	1	µA	CE low

[1] The transmit current consumption tests used the same combined PA and LNA matching network as that used on the EVAL-ADF7021DBx evaluation boards. Improved PA efficiency is achieved by using a separate PA matching network.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%, DGND = AGND = 0 V, T_A = 25°C, unless otherwise noted. Guaranteed by design but not production tested.

Table 6.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	>10	ns	SDATA to SCLK setup time
t_2	>10	ns	SDATA to SCLK hold time
t_3	>25	ns	SCLK high duration
t_4	>25	ns	SCLK low duration
t_5	>10	ns	SCLK to SLE setup time
t_6	>20	ns	SLE pulse width
t_8	<25	ns	SCLK to SREAD data valid, readback
t_9	<25	ns	SREAD hold time after SCLK, readback
t_{10}	>10	ns	SCLK to SLE disable time, readback
t_{11}	$5 < t_{11} < (¼ \times t_{BIT})$	ns	TxRxCLK negative edge to SLE
t_{12}	>5	ns	TxRxDATA to TxRxCLK setup time (Tx mode)
t_{13}	>5	ns	TxRxCLK to TxRxDATA hold time (Tx mode)
t_{14}	$>¼ \times t_{BIT}$	µs	TxRxCLK negative edge to SLE
t_{15}	$>¼ \times t_{BIT}$	µs	SLE positive edge to positive edge of TxRxCLK

Timing Diagrams

Serial Interface

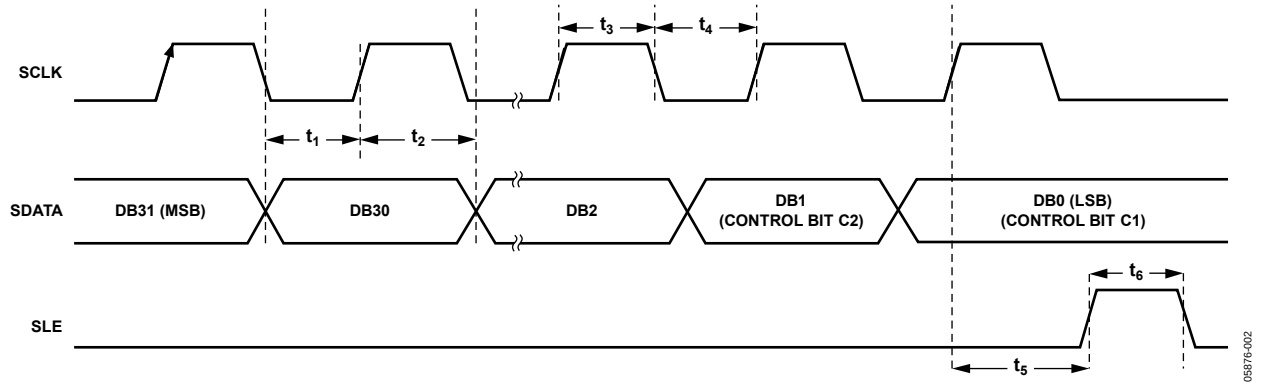


Figure 2. Serial Interface Timing Diagram

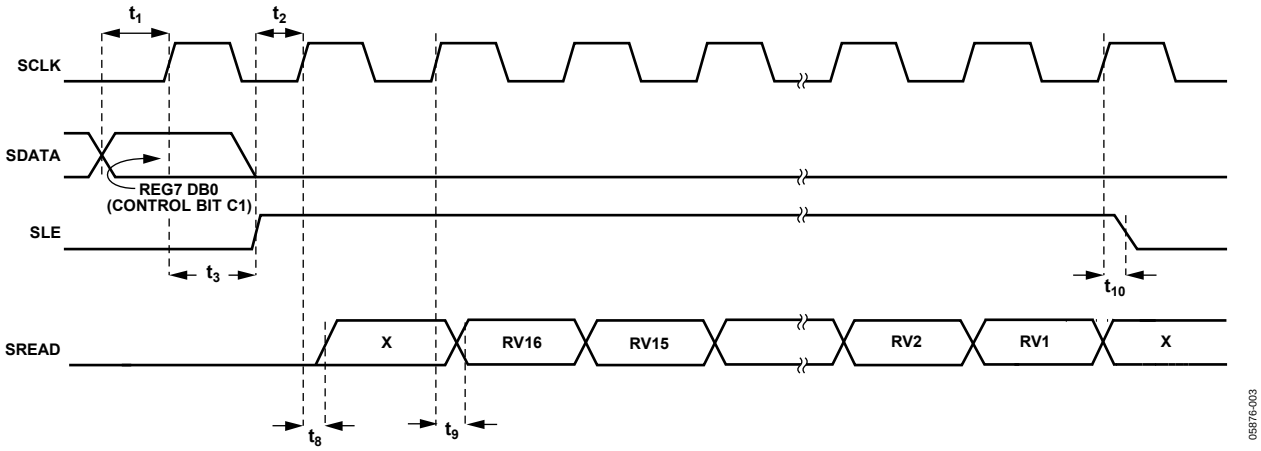


Figure 3. Serial Interface Readback Timing Diagram

2FSK/3FSK Timing

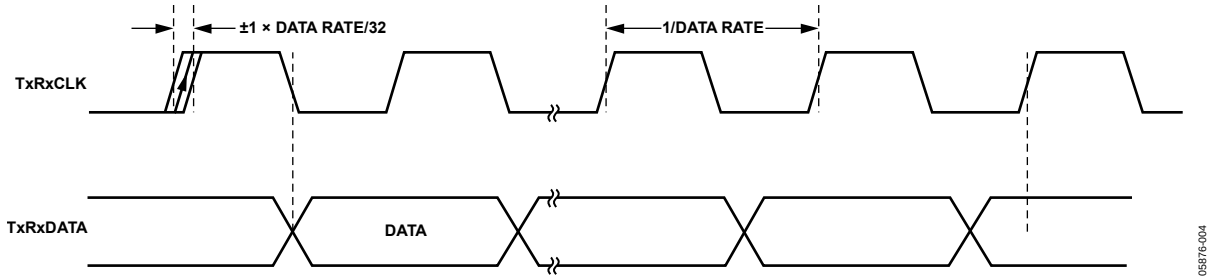


Figure 4. TxRxDATA/TxRxCLK Timing Diagram in Receive Mode

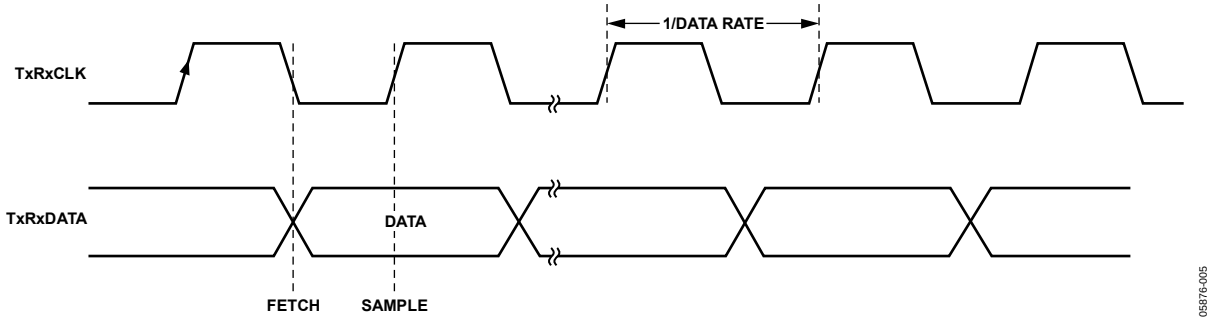


Figure 5. TxRxDATA/TxRxCLK Timing Diagram in Transmit Mode

4FSK Timing

In 4FSK receive mode, MSB/LSB synchronization should be guaranteed by SWD in the receive bit stream.

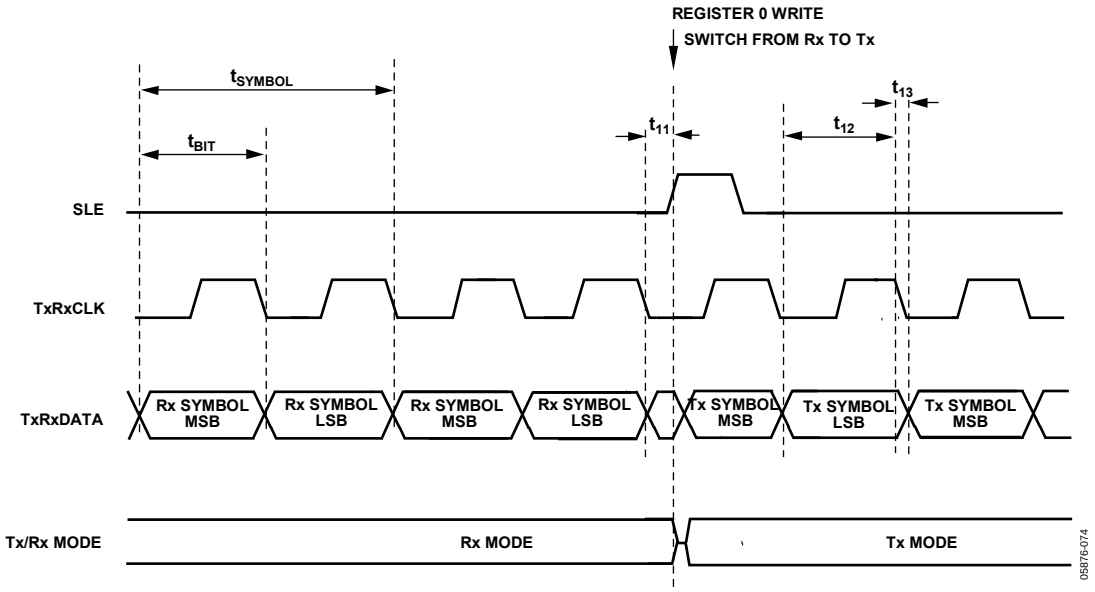


Figure 6. Receive-to-Transmit Timing Diagram in 4FSK Mode

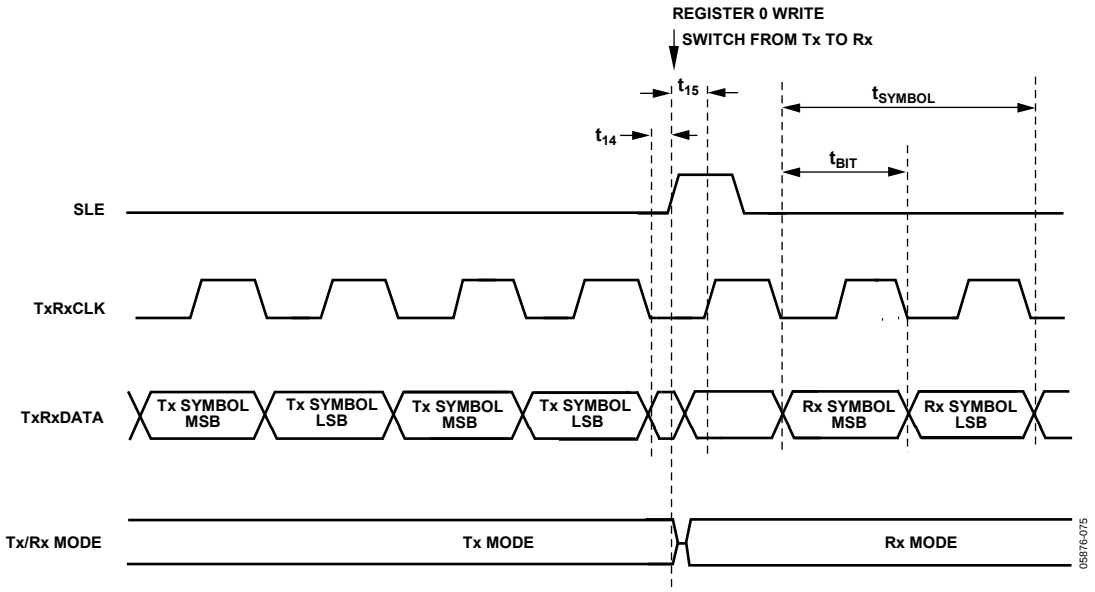


Figure 7. Transmit-to-Receive Timing Diagram in 4FSK Mode

UART/SPI Mode

UART mode is enabled by setting R0_DB28 to 1. SPI mode is enabled by setting R0_DB28 to 1 and setting R15_DB[17:19] to 0x7. The transmit/receive data clock is available on the CLKOUT pin.

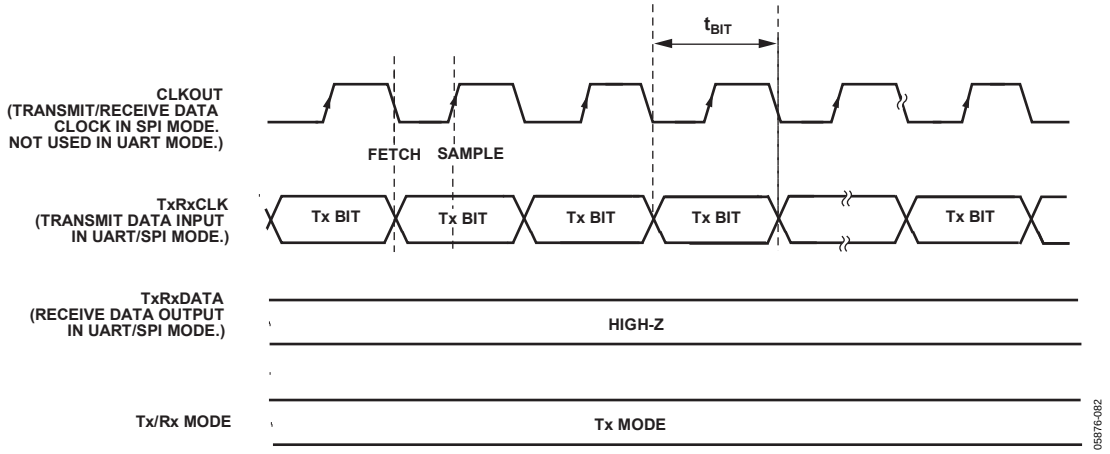


Figure 8. Transmit Timing Diagram in UART/SPI Mode

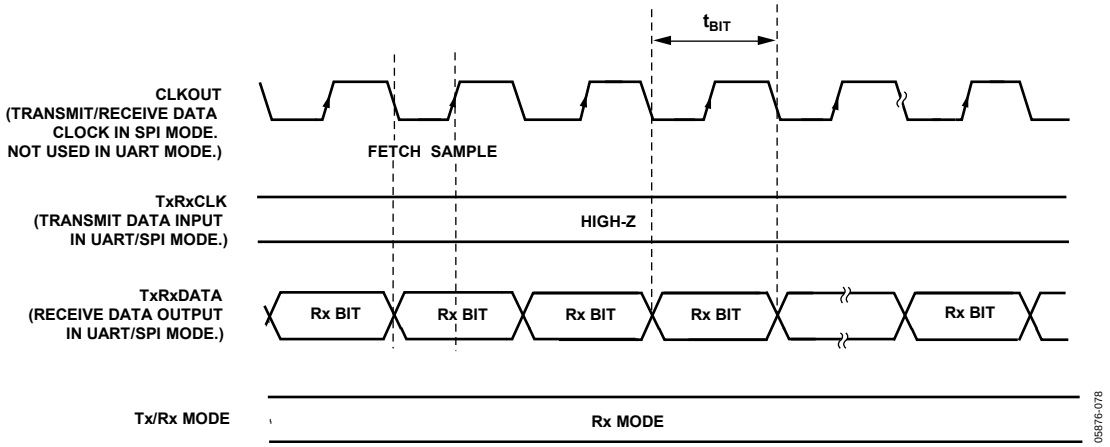


Figure 9. Receive Timing Diagram in UART/SPI Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = CPGND = RFGND = DGND = AGND = 0.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

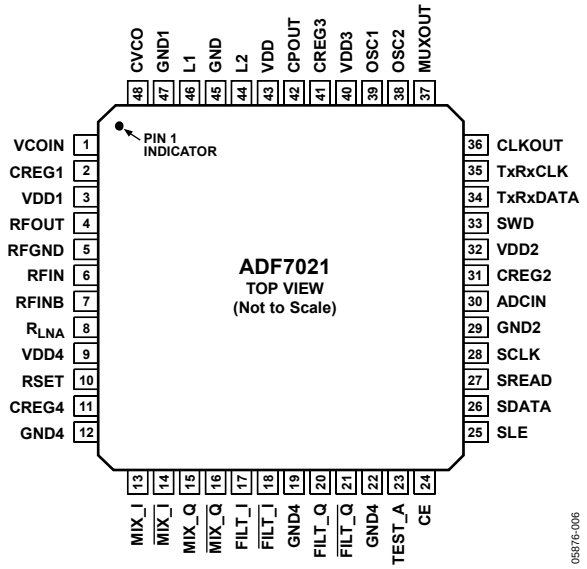


Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	CREG1	Regulator Voltage for PA Block. Place a series 3.9 Ω resistor and a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Place decoupling capacitors of 0.1 µF and 100 pF as close as possible to this pin. Tie all VDD pins together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −16 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components (see the Transmitter section).
5	RFGND	Ground for Output Stage of Transmitter. All GND pins should be tied together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer (see the LNA/PA Matching section).
7	RFINB	Complementary LNA Input (see the LNA/PA Matching section).
8	R_{LNA}	External Bias Resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/MIXER Block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor. Sets charge pump current and some internal bias currents. Use a 3.6 kΩ resistor with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/MIXER Block. Place a 100 nF capacitor between this pin and GND for regulator stability and noise rejection.
12, 19, 22	GND4	Ground for LNA/MIXER Block.
13 to 18	MIX_I, $\overline{\text{MIX_I}}$, MIX_Q, $\overline{\text{MIX_Q}}$, FILT_I, $\overline{\text{FILT_I}}$	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
20, 21, 23	FILT_Q, $\overline{\text{FILT_Q}}$, TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7021 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When SLE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the 4 LSBs as the control bits. This pin is a high impedance CMOS input.
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7021 to the microcontroller. The SCLK input is used to clock each readback bit (for example, AFC or ADC) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This pin is a digital CMOS input.

Pin No.	Mnemonic	Description
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 V to 1.9 V. Readback is made using the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. Place a decoupling capacitor of 10 nF as close as possible to this pin.
33	SWD	Sync Word Detect. The ADF7021 asserts this pin when it has found a match for the sync word sequence (see the Register 11—Sync Word Detect Register section). This provides an interrupt for an external microcontroller indicating valid data is being received.
34	TxRxDATA	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply. In UART/SPI mode, this pin provides an output for the received data in receive mode. In transmit UART/SPI mode, this pin is high impedance (see the Interfacing to Microcontroller/DSP section).
35	TxRxCLK	Outputs the data clock in both receive and transmit modes. This is a digital pin and normal CMOS levels apply. The positive clock edge is matched to the center of the received data. In transmit mode, this pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. In UART/SPI mode, this pin is used to input the transmit data in transmit mode. In receive UART/SPI mode, this pin is high impedance (see the Interfacing to Microcontroller/DSP section).
36	CLKOUT	A divided-down version of the crystal reference with output driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio and is inverted with respect to the reference. Place a series 1 kΩ resistor as close as possible to the pin in applications where the CLKOUT feature is being used.
37	MUXOUT	Provides the DIGITAL_LOCK_DETECT Signal. This signal is used to determine if the PLL is locked to the correct frequency. It also provides other signals such as REGULATOR_READY, which is an indicator of the status of the serial interface regulator (see the MUXOUT section for more information).
38	OSC2	Connect the reference crystal between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the internal crystal oscillator.
39	OSC1	Connect the reference crystal between this pin and OSC2. A TCXO reference can be used by driving this pin with ac-coupled 0.8 V p-p levels and by enabling the internal crystal oscillator.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. Decouple this pin to ground with a 10 nF capacitor.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. Decouple this pin to ground with a 10 nF capacitor.
44, 46	L2, L1	External VCO Inductor Pins. If using an external VCO inductor, connect a chip inductor across these pins to set the VCO operating frequency. If using the internal VCO inductor, these pins can be left floating. See the Voltage Controlled Oscillator (VCO) section for more information.
45, 47	GND, GND1	Grounds for VCO Block.
48	CVCO	Place a 22 nF capacitor between this pin and CREG1 to reduce VCO noise.

TYPICAL PERFORMANCE CHARACTERISTICS

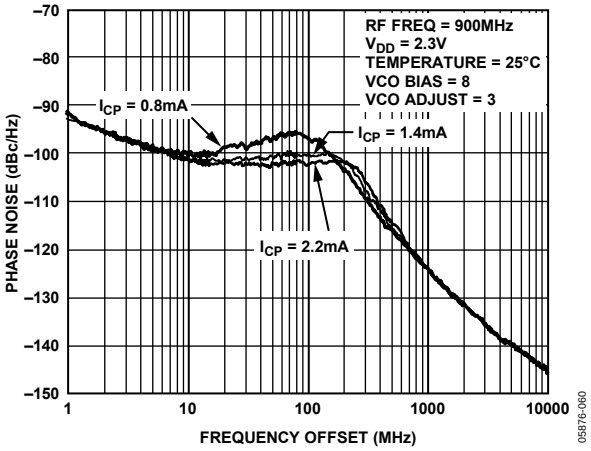


Figure 11. Phase Noise Response at 900 MHz, V_{DD} = 2.3 V

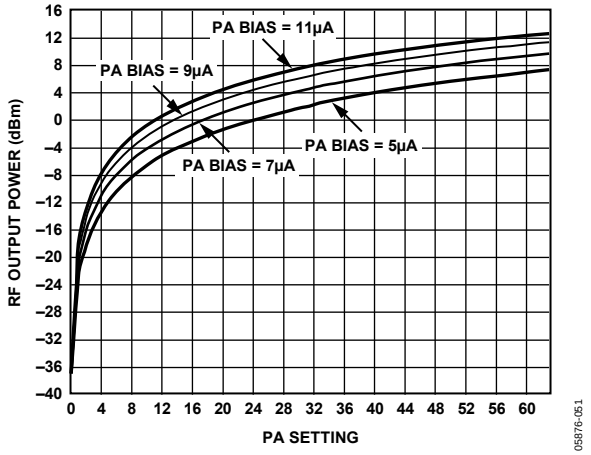


Figure 12. RF Output Power vs. PA Setting

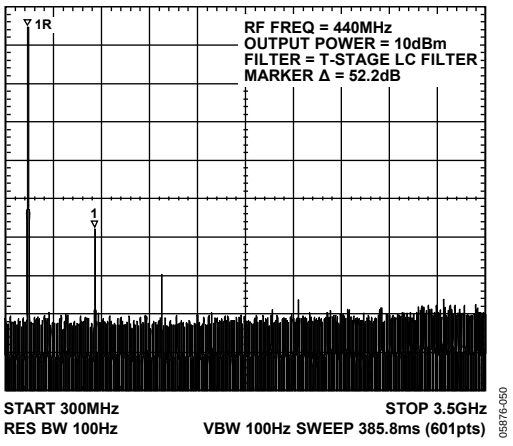


Figure 13. PA Output Harmonic Response with T-Stage LC Filter

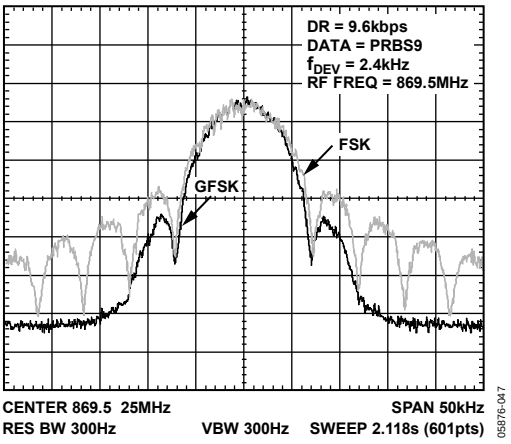


Figure 14. Output Spectrum in 2FSK and GFSK Modes

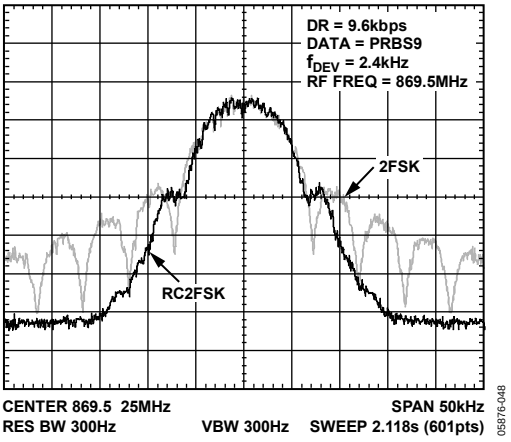


Figure 15. Output Spectrum in 2FSK and Raised Cosine 2FSK Modes

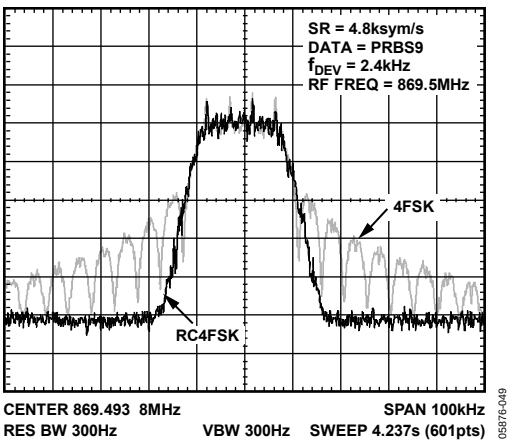


Figure 16. Output Spectrum in 4FSK and Raised Cosine 4FSK Modes

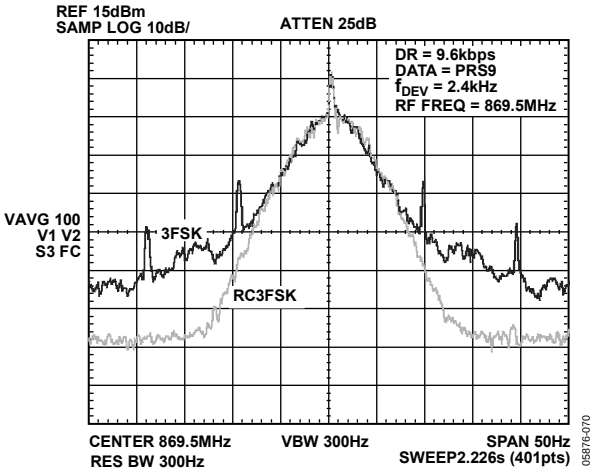


Figure 17. Output Spectrum in 3FSK and Raised Cosine 3FSK Modes

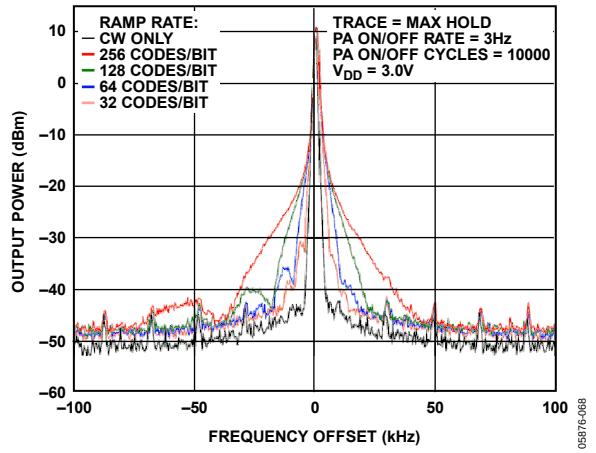


Figure 18. Output Spectrum in Maximum Hold for Various PA Ramp Rate Options

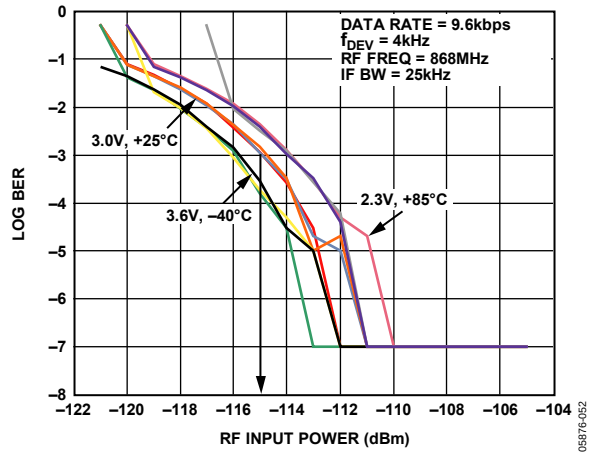


Figure 19. 2FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 868 MHz

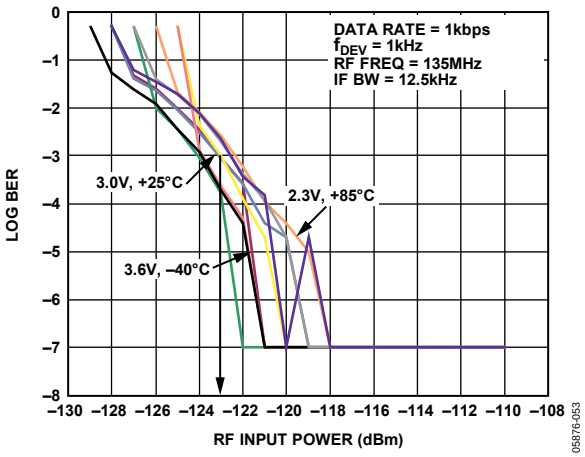


Figure 20. 2FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 135 MHz

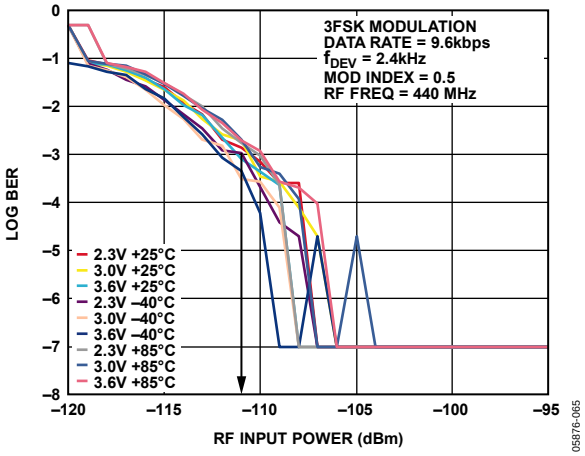


Figure 21. 3FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 440 MHz

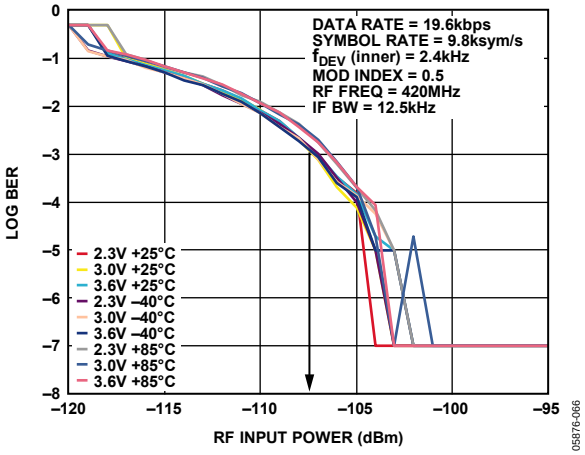


Figure 22. 4FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 420 MHz

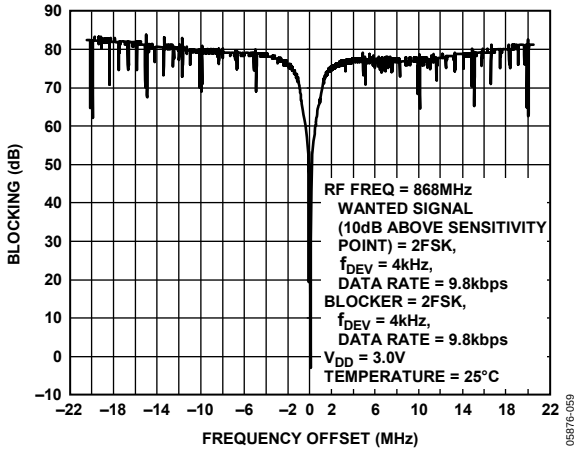


Figure 23. Wideband Interference Rejection

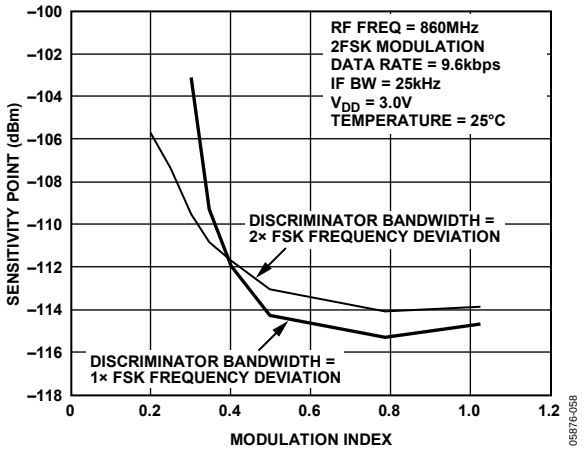


Figure 26. 2FSK Sensitivity vs. Modulation Index vs. Correlator Discriminator Bandwidth

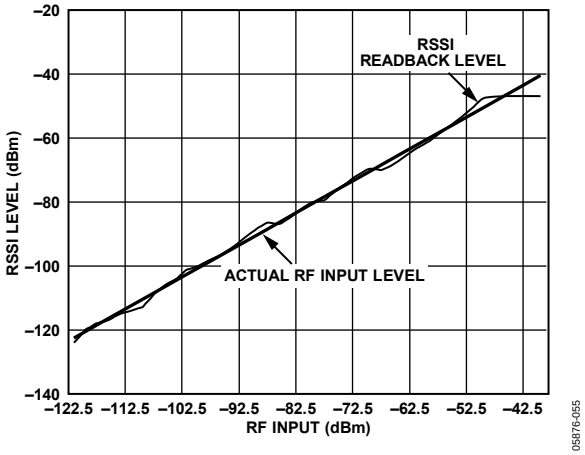


Figure 24. Digital RSSI Readback Linearity

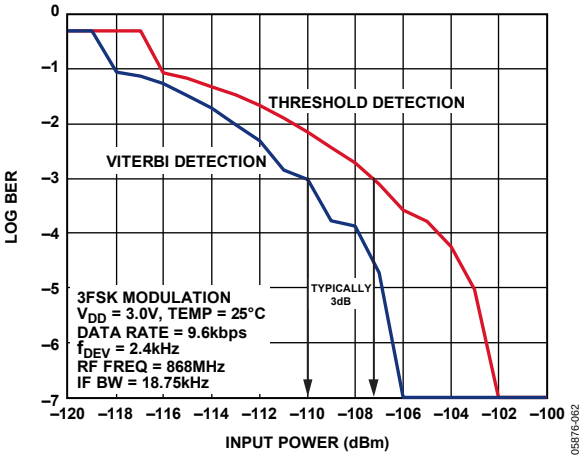


Figure 27. 3FSK Receiver Sensitivity Using Viterbi Detection and Threshold Detection

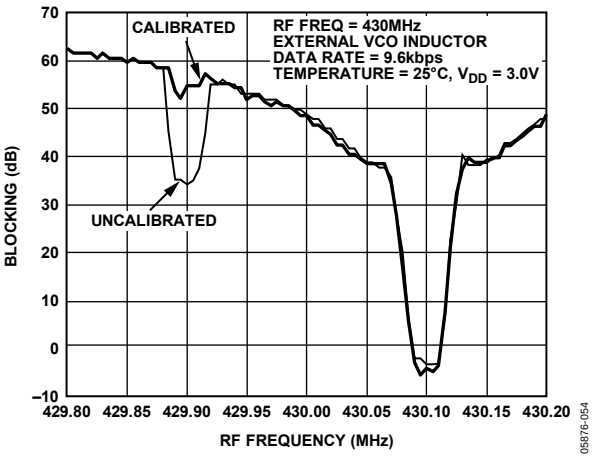


Figure 25. Image Rejection, Uncalibrated vs. Calibrated

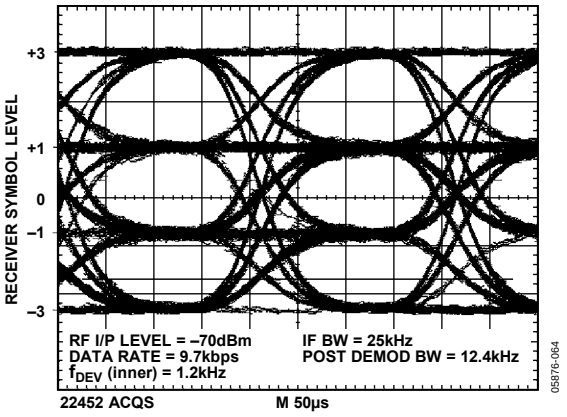


Figure 28. 4FSK Receiver Eye Diagram Measure Using the Test DAC Output

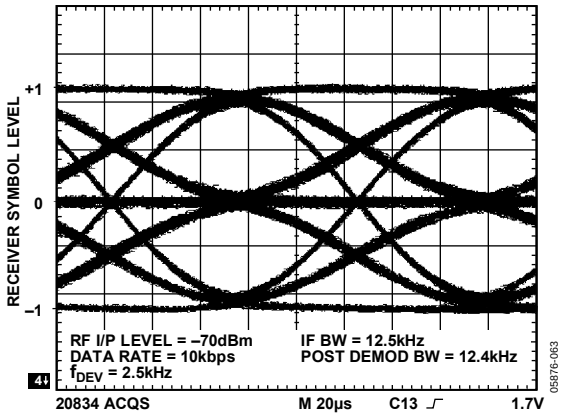


Figure 29. 3FSK Receiver Eye Diagram Measured Using the Test DAC Output

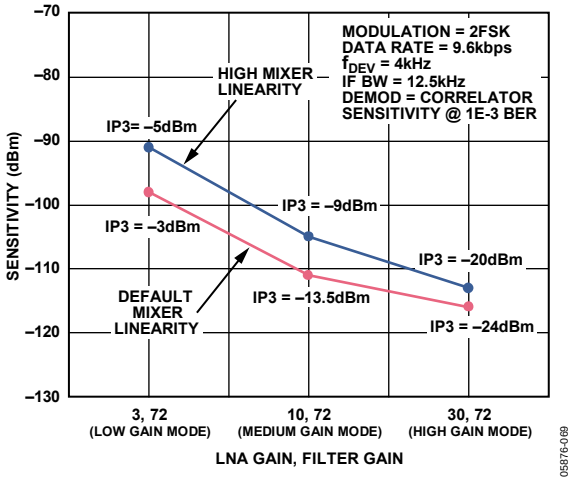


Figure 30. Receive Sensitivity vs. LNA/IF Filter Gain and Mixer Linearity Settings (The Input IP3 at Each Setting is Also Shown)

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 31) can use a quartz crystal as the PLL reference. Using a quartz crystal with a frequency tolerance of ≤10 ppm for narrow-band applications is recommended. It is possible to use a quartz crystal with >10 ppm tolerance, but to comply with the absolute frequency error specifications of narrow-band regulations (for example, ARIB STD-T67 and ETSI EN 300-220), compensation for the frequency error of the crystal is necessary.

The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected by using the automatic frequency control feature or by adjusting the fractional-N value (see the N Counter section).

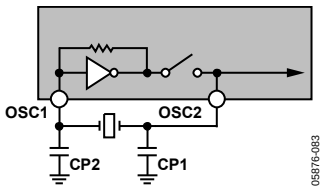


Figure 31. Oscillator Circuit on the ADF7021

Two parallel resonant capacitors are required for oscillation at the correct frequency. Their values are dependent upon the crystal specification. They should be chosen to make sure that the series value of capacitance added to the PCB track capacitance adds up to the specified load capacitance of the crystal, usually 12 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

Using a TCXO Reference

A single-ended reference (TCXO, VCXO, or OCXO) can also be used with the ADF7021. This is recommended for applications having absolute frequency accuracy requirements of <10 ppm, such as ARIB STD-T67 or ETSI EN 300-220. There are two options for interfacing the ADF7021 to an external reference oscillator.

- An oscillator with CMOS output levels can be applied to OSC2. The internal oscillator circuit should be disabled by setting R1_DB12 low.
- An oscillator with 0.8 V p-p levels can be ac-coupled through a 22 pF capacitor into OSC1. The internal oscillator circuit should be enabled by setting R1_DB12 high.

Programmable Crystal Bias Current

Bias current in the oscillator circuit can be configured between 20 μA and 35 μA by writing to the XTAL_BIAS bits (R1_DB[13:14]). Increasing the bias current allows the crystal oscillator to power up faster.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 31, and supplies a divided-down, 50:50 mark-space signal to the CLKOUT pin. The CLKOUT signal is inverted with respect to the reference clock. An even divide from 2 to 30 is available. This divide number is set in R1_DB[7:10]. On power-up, the CLKOUT defaults to divide-by-8.

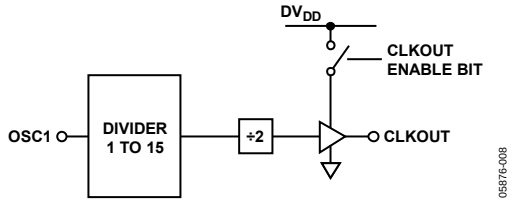


Figure 32. CLKOUT Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A series resistor (1 kΩ) can be used to slow the clock edges to reduce these spurs at the CLKOUT frequency.

R Counter

The 3-bit R counter divides the reference input frequency by an integer of 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in R1_DB[4:6]. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output and reduces occurrences of spurious components.

Register 1 defaults to R = 1 on power-up.

$$PFD\ [\text{Hz}] = XTAL/R$$

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 33.

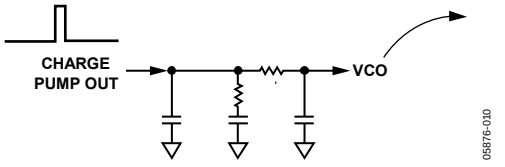


Figure 33. Typical Loop Filter Configuration

The loop should be designed so that the loop bandwidth (LBW) is approximately 100 kHz. This provides a good compromise between in-band phase noise and out-of-band spurious rejection. Widening the LBW excessively reduces the time spent jumping between frequencies, but it can cause insufficient spurious attenuation. Narrow-loop bandwidths can result in the loop taking long periods to attain lock and can also result in a higher level of power falling into the adjacent channel. The loop filter design on the EVAL-ADF7021DBX should be used for optimum performance.

The free design tool ADIsimPLL can also be used to design loop filters for the ADF7021 (go to www.analog.com/ADIsimPLL for details).

N Counter

The feedback divider in the ADF7021 PLL consists of an 8-bit integer counter (R0_DB[19:26]) and a 15-bit Σ-Δ fractional_N divider (R0_DB[4:18]). The integer counter is the standard pulse-swallow type that is common in PLLs. This sets the minimum integer divide value to 23. The fractional divide value provides very fine resolution at the output, where the output frequency of the PLL is calculated as

$$f_{OUT} = \frac{XTAL}{R} \times \left(Integer_N + \frac{Fractional_N}{2^{15}} \right)$$

When RF_DIVIDE_BY_2 (see the Voltage Controlled Oscillator (VCO) section) is selected, this formula becomes

$$f_{OUT} = \frac{XTAL}{R} \times 0.5 \times \left(Integer_N + \frac{Fractional_N}{2^{15}} \right)$$

The combination of the integer_N (maximum = 255) and the fractional_N (maximum = 32,768/32,768) give a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

$$PFD_{MIN}[\text{Hz}] = \frac{Maximum\ Required\ Output\ Frequency}{(255+1)}$$

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz.

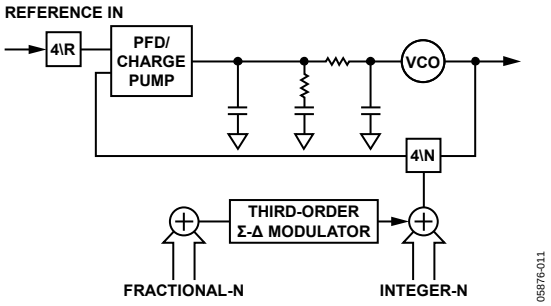


Figure 34. Fractional-N PLL

Voltage Regulators

The ADF7021 contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Regulator 1 requires a 3.9 Ω resistor and a 100 nF capacitor in series between CREG1 and GND, whereas the other regulators require a 100 nF capacitor connected between CREGx and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the CE pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates from a regulator supply. Therefore, to write to the part, the user must have CE high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the REGULATOR_READY signal from MUXOUT.

MUXOUT

The MUXOUT pin allows access to various digital points in the ADF7021. The state of MUXOUT is controlled by R0_DB[29:31].

REGULATOR_READY

REGULATOR_READY is the default setting on MUXOUT after the transceiver is powered up. The power-up time of the regulator is typically 50 μs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7021 can be programmed. The status of the regulator can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7021 can begin.

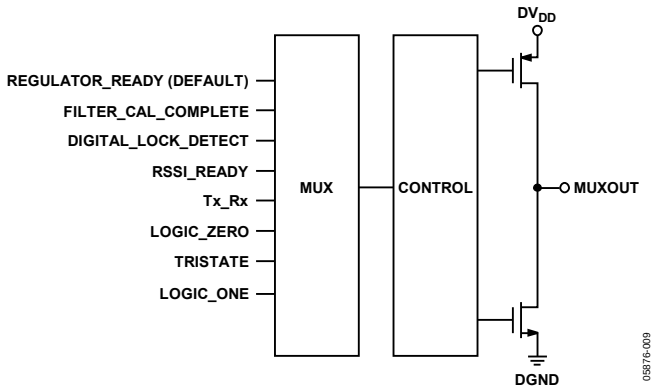


Figure 35. MUXOUT Circuit

FILTER_CAL_COMPLETE

MUXOUT can be set to FILTER_CAL_COMPLETE. This signal goes low for the duration of both a coarse IF filter calibration and a fine IF filter calibration. It can be used as an interrupt to a microcontroller to signal the end of the IF filter calibration.

DIGITAL_LOCK_DETECT

DIGITAL_LOCK_DETECT indicates when the PLL has locked. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until a 25 ns phase error is detected at the PFD.

RSSI_READY

MUXOUT can be set to RSSI_READY. This indicates that the internal analog RSSI has settled and a digital RSSI readback can be performed.

Tx_Rx

Tx_Rx signifies whether the ADF7021 is in transmit or receive mode. When in transmit mode, this signal is low. When in receive mode, this signal is high. It can be used to control an external Tx/Rx switch.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The ADF7021 contains two VCO cores. The first VCO, the internal inductor VCO, uses an internal LC tank and supports 862 MHz to 950 MHz and 431 MHz to 475 MHz operating bands. The second VCO, the external inductor VCO, uses an external inductor as part of its LC tank and supports the RF operating band of 80 MHz to 650 MHz.

To minimize spurious emissions, both VCOs operate at twice the RF frequency. The VCO signal is then divided by 2 inside the synthesizer loop, giving the required frequency for the transmitter and the required local oscillator (LO) frequency for the receiver. A further divide-by-2 (RF_DIVIDE_BY_2) is performed outside the synthesizer loop to allow operation in the 431 MHz to 475 MHz band (internal inductor VCO) and 80 MHz to 325 MHz band (external inductor VCO).

The VCO needs an external 22 nF capacitor between the CVCO pin and the regulator (CREG1) to reduce internal noise.

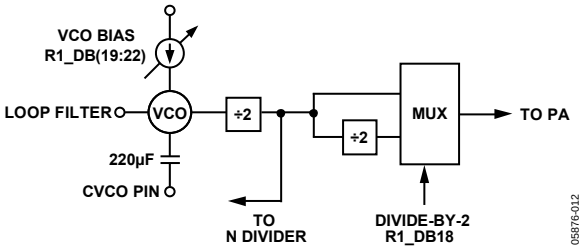


Figure 36. Voltage Controlled Oscillator (VCO)

Internal Inductor VCO

To select the internal inductor VCO, set R1_DB25 to Logic 0, which is the default setting.

VCO bias current can be adjusted using R1_DB[19:22]. To ensure VCO oscillation, the minimum bias current setting under all conditions when using the internal inductor VCO is 0x8.

The VCO should be re-centered, depending on the required frequency of operation, by programming the VCO_ADJUST bits (R1_DB[23:24]). This is detailed in Table 9.

External Inductor VCO

When using the external inductor VCO, the center frequency of the VCO is set by the internal varactor capacitance and the combined inductance of the external chip inductor, bond wire, and PCB track. The external inductor is connected between the L2 and L1 pins.

A plot of the VCO operating frequency vs. total external inductance (chip inductor + PCB track) is shown in Figure 37.

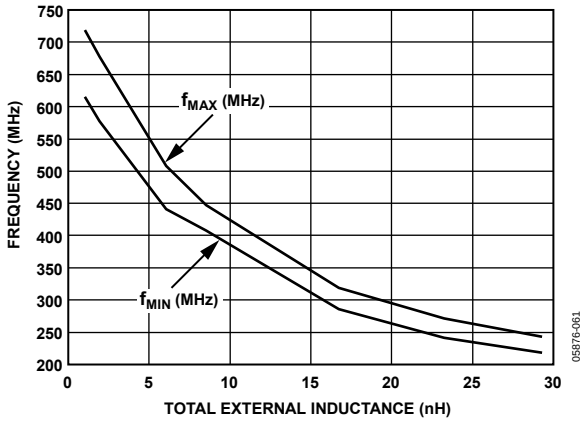


Figure 37. Direct RF Output vs. Total External Inductance

The inductance for a PCB track using FR4 material is approximately 0.57 nH/mm. This should be subtracted from the total value to determine the correct chip inductor value.

Typically, a particular inductor value allows the ADF7021 to function over a range of ±6% of the RF operating frequency. When the RF_DIVIDE_BY_2 bit (R1_DB18) is selected, this range becomes ±3%. At 400 MHz, for example, an operating range of ±24 MHz (that is, 376 MHz to 424 MHz) with a single inductor (VCO range centered at 400 MHz) can be expected.

The VCO tuning voltage can be checked for a particular RF output frequency by measuring the voltage on the VCOIN pin when the part is fully powered up in transmit or receive mode.

The VCO tuning range is 0.2 V to 2 V. The external inductor value should be chosen to ensure that the VCO is operating as close as possible to the center of this tuning range. This is particularly important for RF frequencies <200 MHz, where the VCO gain is reduced and a tuning range of <±6 MHz exists.

The VCO operating frequency range can be adjusted by programming the VCO_ADJUST bits (R1_DB[23:24]). This typically allows the VCO operating range to be shifted up or down by a maximum of 1% of the RF frequency.

To select the external inductor VCO, set R1_DB25 to Logic 1. The VCO_BIAS_CURRENT should be set depending on the frequency of operation (as indicated in Table 9).

Table 9. RF Output Frequency Ranges for Internal and External Inductor VCOs and Required Register Settings

			Register Settings			
RF Frequency Output (MHz)	**VCO to Be Used**	**RF Divide by 2**	**(VCO_INDUCTOR) R1_DB25**	**(RF_DIVIDE_BY_2) R1_DB18**	**(VCO_ADJUST) R1_DB[23:24]**	**(VCO_BIAS) R1_DB[19:22]**
900 to 950	Internal L	No	0	0	11	8
862 to 900	Internal L	No	0	0	00	8
450 to 470	Internal L	Yes	0	1	11	8
431 to 450	Internal L	Yes	0	1	00	8
450 to 650	External L	No	1	0	XX	4
200 to 450	External L	No	1	0	XX	3
80 to 200	External L	Yes	1	1	XX	2

CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

An interaction between the RF VCO frequency and the reference frequency can lead to fractional spur creation. When the synthesizer is in fractional mode (that is, the RF VCO and reference frequencies are not integer related), spurs can appear on the VCO output spectrum at an offset frequency that corresponds to the difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter. They are more noticeable on channels close to integer multiples of the reference where the difference frequency may be inside the loop bandwidth; thus, the name integer boundary spurs. The occurrence of these spurs is rare because the integer frequencies are around multiples of the reference, which is typically >10 MHz. To avoid having very small or very large values in the fractional register, choose a suitable reference frequency.

TRANSMITTER

RF OUTPUT STAGE

The power amplifier (PA) of the ADF7021 is based on a single-ended, controlled current, open-drain amplifier that has been designed to deliver up to 13 dBm into a 50 Ω load at a maximum frequency of 950 MHz.

The PA output current and consequently, the output power, are programmable over a wide range. The PA configuration is shown in Figure 38. The output power is set using R2_DB[13:18].

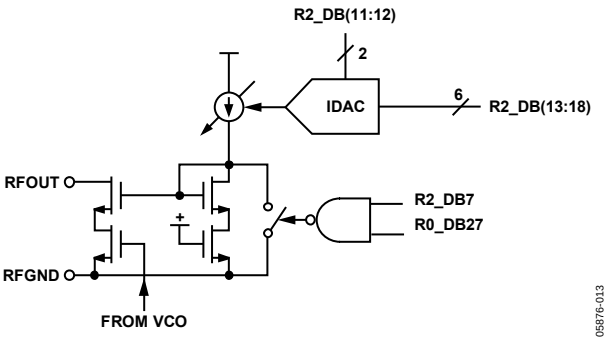


Figure 38. PA Configuration

The PA is equipped with overvoltage protection, which makes it robust in severe mismatch conditions. Depending on the application, users can design a matching network for the PA to exhibit optimum efficiency at the desired radiated output power level for a wide range of antennas, such as loop or monopole antennas. See the LNA/PA Matching section for more information.

PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. Some radio emissions regulations place limits on these PA transient-induced spurs (for example, ETSI EN 300 220). By gradually ramping the PA on and off, PA transient spurs are minimized.

The ADF7021 has built-in PA ramping configurability. As Figure 39 illustrates, there are eight ramp rate settings, defined as a certain number of PA setting codes per one data bit period. The PA steps through each of its 64 code levels but at different speeds for each setting. The ramp rate is set by configuring R2_DB[8:10].

If the PA is enabled/disabled by PA_ENABLE (R2_DB7), it ramps up at the programmed rate but turns off hard. If the PA is enabled/disabled by Tx/Rx (R0_DB27), it ramps up and down at the programmed rate.

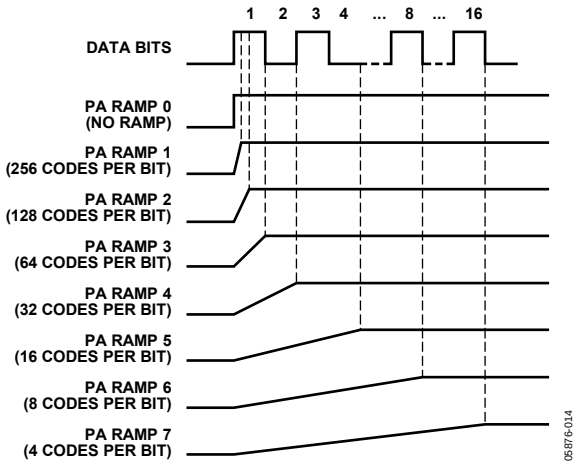


Figure 39. PA Ramping Settings

PA Bias Currents

The PA_BIAS bits (R2_DB[11:12]) facilitate an adjustment of the PA bias current to further extend the output power control range, if necessary. If this feature is not required, the default value of 9 μA is recommended. If output power of greater than 10 dBm is required, a PA bias setting of 11 μA is recommended. The output stage is powered down by resetting R2_DB7.

MODULATION SCHEMES

The ADF7021 supports 2FSK, 3FSK, and 4FSK modulation. The implementation of these modulation schemes is shown in Figure 40.

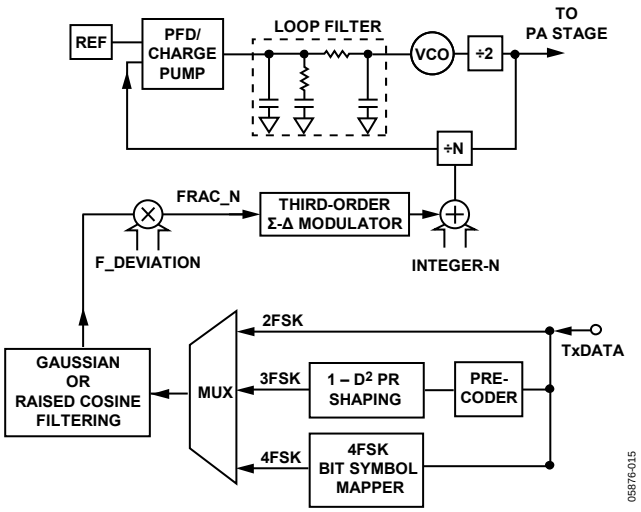


Figure 40. Transmit Modulation Implementation

Setting the Transmit Data Rate

In all modulation modes except oversampled 2FSK mode, an accurate clock is provided on the TxRxCLK pin to latch the data from the microcontroller into the transmit section at the required data rate. The exact frequency of this clock is defined by

$$DATA\ CLK = \frac{XTAL}{DEMOD_CLK_DIVIDE \times CDR_CLK_DIVIDE \times 32}$$

where:
XTAL is the crystal or TCXO frequency.
DEMOD_CLK_DIVIDE is the divider that sets the demodulator clock rate (R3_DB[6:9]).
CDR_CLK_DIVIDE is the divider that sets the CDR clock rate (R3_DB[10:17]).

Refer to the Register 3—Transmit/Receive Clock Register section for more programming information.

Setting the FSK Transmit Deviation Frequency

In all modulation modes, the deviation from the center frequency is set using the Tx_FREQUENCY_DEVIATION bits (R2_DB[19:27]).

The deviation from the center frequency in Hz is as follows:

For direct RF output,

$$f_{DEV}\ [\text{Hz}] = \frac{PFD \times Tx_FREQUENCY_DEVIATION}{2^{16}}$$

For RF_DIVIDE_BY_2 enabled,

$$f_{DEV}\ [\text{Hz}] = 0.5 \times \frac{PFD \times Tx_FREQUENCY_DEVIATION}{2^{16}}$$

where *Tx_FREQUENCY_DEVIATION* is a number from 1 to 511 (R2_DB[19:27]).

In 4FSK modulation, the four symbols (00, 01, 11, 10) are transmitted as $\pm 3 \times f_{DEV}$ and $\pm 1 \times f_{DEV}$.

Binary Frequency Shift Keying (2FSK)

Two-level frequency shift keying is implemented by setting the N value for the center frequency and then toggling it with the TxDATA line. The deviation from the center frequency is set using the Tx_FREQUENCY_DEVIATION bits, R2_DB[19:27].

2FSK is selected by setting the MODULATION_SCHEME bits (R2_DB[4:6]) to 000.

Minimum shift keying (MSK) or Gaussian minimum shift keying (GMSK) is supported by selecting 2FSK modulation and using a modulation index of 0.5. A modulation index of 0.5 is set up by configuring R2_DB[19:27] for a $FREQ_{DEVIATION}$ = 0.25 × transmit data rate.

3-Level Frequency Shift Keying (3FSK)

In 3-level FSK modulation (also known as modified Duobinary FSK), the binary data (Logic 0 and Logic 1) is mapped onto three distinct frequencies, the carrier frequency (f_C), the carrier frequency minus a deviation frequency ($f_C - f_{DEV}$), and the carrier frequency plus the deviation frequency ($f_C + f_{DEV}$).

A Logic 0 is mapped to the carrier frequency while a Logic 1 is either mapped onto frequency $f_C - f_{DEV}$ or $f_C + f_{DEV}$.

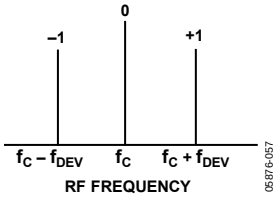


Figure 41. 3FSK Symbol-to-Frequency Mapping

Compared to 2FSK, this bits-to-frequency mapping results in a reduced transmission bandwidth because some energy is removed from the RF sidebands and transferred to the carrier frequency. At low modulation index, 3FSK improves the transmit spectral efficiency by up to 25% when compared to 2FSK.

Bit-to-symbol mapping for 3FSK is implemented using a linear convolutional encoder that also permits Viterbi detection to be used in the receiver. A block diagram of the transmit hardware used to realize this system is shown in Figure 42. The convolutional encoder polynomial used to implement the transmit spectral shaping is

$$P(D) = 1 - D^2$$

where:
P is the convolutional encoder polynomial.
D is the unit delay operator.

A digital precoder with transfer function 1/P(D) implements an inverse modulo-2 operation of the $1 - D^2$ shaping filter in the transmitter.

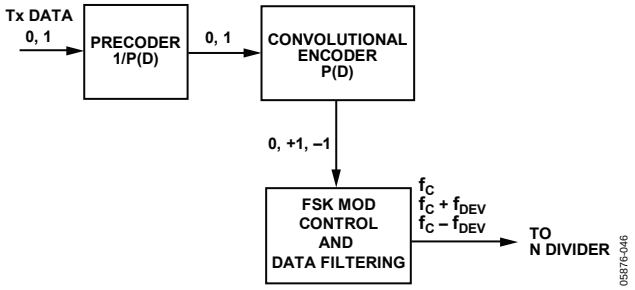


Figure 42. 3FSK Encoding

The signal mapping of the input binary transmit data to the 3-level convolutional output is shown in Table 10. The convolutional encoder restricts the maximum number of sequential +1s or −1s to two and delivers an equal number of +1s and −1s to the FSK modulator, thus ensuring equal spectral energy in both RF sidebands.

Table 10. 3-Level Signal Mapping of the Convolutional Encoder

TxDATA	1	0	1	1	0	0	1	0	0	1
Precoder Output	1	0	0	1	0	1	1	1	1	0
Encoder Output	+1	0	−1	+1	0	0	+1	0	0	−1

Another property of this encoding scheme is that the transmitted symbol sequence is dc-free, which facilitates symbol detection and frequency measurement in the receiver. In addition, there is no code rate loss associated with this 3-level convolutional encoder; that is, the transmitted symbol rate is equal to the data rate presented at the transmit data input.

3FSK is selected by setting the MODULATION_SCHEME bits (R2_DB[4:6]) to 010. It can also be used with raised cosine filtering to further increase the spectral efficiency of the transmit signal.

4-Level Frequency Shift Keying (4FSK)

In 4FSK modulation, two bits per symbol spectral efficiency is realized by mapping consecutive input bit-pairs in the Tx data bit stream to one of four possible symbols (−3, −1, +1, +3). Thus, the transmitted symbol rate is half of the input bit rate.

By minimizing the separation between symbol frequencies, 4FSK can have high spectral efficiency. The bit-to-symbol mapping for 4FSK is gray coded and is shown in Figure 43.

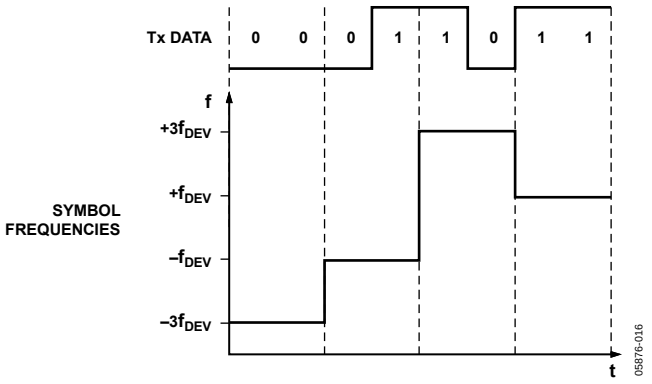


Figure 43. 4FSK Bit-to-Symbol Mapping

The inner deviation frequencies ($+f_{DEV}$ and $-f_{DEV}$) are set using the Tx_FREQUENCY_DEVIATION bits, R2_DB[19:27]. The outer deviation frequencies are automatically set to three times the inner deviation frequency.

The transmit clock from Pin TxRxCLK is available after writing to Register 3 in the power-up sequence for receive mode. The MSB of the first symbol should be clocked into the ADF7021 on the first transmit clock pulse from the ADF7021 after writing to Register 3. Refer to Figure 6 for more timing information.

Oversampled 2FSK

In oversampled 2FSK, there is no data clock from the TxRxCLK pin. Instead, the transmit data at the TxRxDATA pin is sampled at 32 times the programmed rate.

This is the only modulation mode that can be used with the UART mode interface for data transmission (refer to the

Interfacing to Microcontroller/DSP section for more information).

SPECTRAL SHAPING

Gaussian or raised cosine filtering can be used to improve transmit spectral efficiency. The ADF7021 supports Gaussian filtering (bandwidth time [BT] = 0.5) on 2FSK modulation. Raised cosine filtering can be used with 2FSK, 3FSK, or 4FSK modulation. The roll off factor (alpha) of the raised cosine filter has programmable options of 0.5 and 0.7. Both the Gaussian and raised cosine filters are implemented using linear phase digital filter architectures that deliver precise control over the BT and alpha filter parameters, and guarantee a transmit spectrum that is very stable over temperature and supply variation.

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the transmit data. The BT product of the Gaussian filter used is 0.5.

Gaussian filtering can only be used with 2FSK modulation. This is selected by setting R2_DB[4:6] to 001.

Raised Cosine Filtering

Raised cosine filtering provides digital prefiltering of the transmit data by using a raised cosine filter with a roll-off factor (alpha) of either 0.5 or 0.7. The alpha is set to 0.5 by default, but the raised cosine filter bandwidth can be increased to provide less aggressive data filtering by using an alpha of 0.7 (set R2_DB30 to Logic 1). Raised cosine filtering can be used with 2FSK, 3FSK, and 4FSK.

Raised cosine filtering is enabled by setting R2_DB[4:6] as outlined in Table 11.

MODULATION AND FILTERING OPTIONS

The various modulation and data filtering options are described in Table 11.

Table 11. Modulation and Filtering Options

Modulation	Data Filtering	R2_DB[4:6]
BINARY FSK		
2FSK	None	000
MSK[1]	None	000
OQPSK with half sine baseband shaping[2]	None	000
GFSK	Gaussian	001
GMSK[3]	Gaussian	001
RC2FSK	Raised cosine	101
Oversampled 2FSK	None	100
3-LEVEL FSK		
3FSK	None	010
RC3FSK	Raised cosine	110
4-LEVEL FSK		
4FSK	None	011
RC4FSK	Raised cosine	111

[1] MSK is 2FSK modulation with a modulation index = 0.5.
[2] Offset quadrature phase shift keying (OQPSK) with half sine baseband shaping is spectrally equivalent to MSK.
[3] GMSK is GFSK with a modulation index = 0.5.

TRANSMIT LATENCY

Transmit latency is the delay time from the sampling of a bit/symbol by the TxRxCLK signal to when that bit/symbol appears at the RF output. The latency without any data filtering is 1 bit. The addition of data filtering adds a further latency as outlined in Table 12.

It is important that the ADF7021 be left in transmit mode after the last data bit is sampled by the data clock to account for this latency. The ADF7021 should stay in transmit mode for a time equal to the number of latency bit periods for the applied modulation scheme. This ensures that all of the data sampled by the TxRxCLK signal appears at RF.

The figures for latency in Table 12 assume that the positive TxRxCLK edge is used to sample data (default). If the TxRxCLK is inverted by setting R2_DB[28:29], an additional 0.5 bit latency can be added to all values in Table 12.

Table 12. Bit/Symbol Latency in Transmit Mode for Various Modulation Schemes

Modulation	Latency
2FSK	1 bit
GFSK	4 bits
RC2FSK, Alpha = 0.5	5 bits
RC2FSK, Alpha = 0.7	4 bits
3FSK	1 bit
RC3FSK, Alpha = 0.5	5 bits
RC3FSK, Alpha = 0.7	4 bits
4FSK	1 symbol
RC4FSK, Alpha = 0.5	5 symbols
RC4FSK, Alpha = 0.7	4 symbols

TEST PATTERN GENERATOR

The ADF7021 has a number of built-in test pattern generators that can be used to facilitate radio link setup or RF measurement.

A full list of the supported patterns is shown in Table 13. The data rate for these test patterns is the programmed data rate set in Register 3.

The PN9 sequence is suitable for test modulation when carrying out adjacent channel power (ACP) or occupied bandwidth measurements.

Table 13. Transmit Test Pattern Generator Options

Test Pattern	R15_DB[8:10]
Normal	000
Transmit Carrier	001
Transmit + f_{DEV} tone	010
Transmit – f_{DEV} tone	011
Transmit 1010 pattern	100
Transmit PN9 sequence	101
Transmit SWD pattern repeatedly	110

RECEIVER SECTION

RF FRONT END

The ADF7021 is based on a fully integrated, low IF receiver architecture. The low IF architecture facilitates a very low external component count and does not suffer from powerline-induced interference problems.

Figure 44 shows the structure of the receiver front end. The many programming options allow users to trade off sensitivity, linearity, and current consumption to best suit their application. To achieve a high level of resilience against spurious reception, the low noise amplifier (LNA) features a differential input. Switch SW2 shorts the LNA input when transmit mode is selected (R0_DB27 = 0). This feature facilitates the design of a combined LNA/PA matching network, avoiding the need for an external Rx/Tx switch. See the LNA/PA Matching section for details on the design of the matching network.

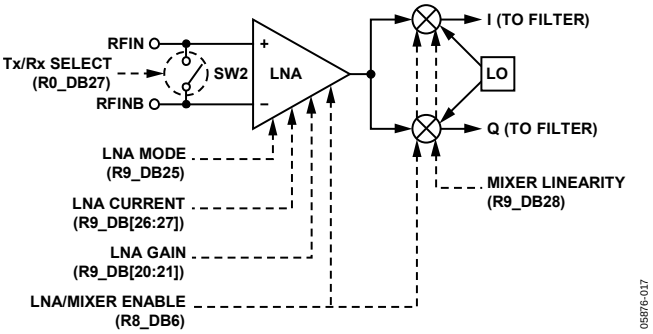


Figure 44. RF Front End

The LNA is followed by a quadrature downconversion mixer, which converts the RF signal to the IF frequency of 100 kHz. An important consideration is that the output frequency of the synthesizer must be programmed to a value 100 kHz below the center frequency of the received channel. The LNA has two basic operating modes: high gain/low noise mode and low gain/low power mode. To switch between these two modes, use the LNA_MODE bit (R9_DB25). The mixer is also configurable between a low current and an enhanced linearity mode using the MIXER_LINEARITY bit (R9_DB28).

Based on the specific sensitivity and linearity requirements of the application, it is recommended to adjust the LNA_MODE bit and MIXER_LINEARITY bit as outlined in Table 14.

The gain of the LNA is configured by the LNA_GAIN bits (R9_DB[20:21]) and can be set by either the user or the automatic gain control (AGC) logic.

IF FILTER

IF Filter Settings

Out-of-band interference is rejected by means of a fifth-order Butterworth polyphase IF filter centered on a frequency of 100 kHz. The bandwidth of the IF filter can be programmed to 12.5 kHz, 18.75 kHz, or 25 kHz by R4_DB[30:31] and should be chosen as a compromise between interference rejection and attenuation of the desired signal.

If the AGC loop is disabled, the gain of the IF filter can be set to one of three levels by using the FILTER_GAIN bits (R9_DB[22:23]). The filter gain is adjusted automatically if the AGC loop is enabled.

IF Filter Bandwidth and Center Frequency Calibration

To compensate for manufacturing tolerances, the IF filter should be calibrated after power-up to ensure that the bandwidth and center frequency are correct. Coarse and fine calibration schemes are provided to offer a choice between fast calibration (coarse calibration) and high filter centering accuracy (fine calibration). Coarse calibration is enabled by setting R5_DB4 high. Fine calibration is enabled by setting R6_DB4 high.

For details on when it is necessary to perform a filter calibration, and in what applications to use either a coarse calibration or fine calibration, refer to the IF Filter Bandwidth Calibration section.

It is necessary to do a coarse calibration before doing a fine calibration. If the IF_FINE_CAL bit (R6_DB4) has already been configured high, it is possible to do a fine calibration by writing only to Register 5. Once initiated by writing to the part, the calibration is performed automatically without any user intervention. Calibration time is 200 µs for coarse calibration and a few milliseconds for fine calibration, during which time the ADF7021 should not be accessed. The IF filter calibration logic requires that the IF_FILTER_DIVIDER bits (R5_DB[5:13]) be set such that

$$\frac{XTAL\,[\mathrm{Hz}]}{IF_FILTER_DIVIDER} = 50\,\mathrm{kHz}$$

IF Filter Fine Calibration Overview

The fine calibration uses two internally generated tones at certain offsets around the IF filter. The two tones are attenuated by the IF filter, and the level of this attenuation is measured using the RSSI. The filter center frequency is adjusted to allow equal attenuation of both tones. The attenuation of the two test tones is then remeasured. This continues for a maximum of 10 RSSI measurements, at which stage the calibration algorithm sets the IF filter center frequency to within 0.5 kHz of 100 kHz.

The frequency of these tones is set by the following bits:

- IF_CAL_LOWER_TONE_DIVIDER (R6_DB[5:12])
- IF_CAL_UPPER_TONE_DIVIDER (R6_DB[13:20])

It is recommended to place the lower and upper tones as close as possible to 65.8 kHz and 131.5 kHz, respectively, as outlined in the following equations:

$$\frac{XTAL}{IF_CAL_LOWER_TONE_DIVIDE \times 2} = 65.8\,\mathrm{kHz}$$

$$\frac{XTAL}{IF_CAL_UPPER_TONE_DIVIDE \times 2} = 131.5\,\mathrm{kHz}$$

The calibration algorithm adjusts the filter center frequency and measures the RSSI 10 times during the calibration. The time for an adjustment plus RSSI measurement is given by

$$IF\ Tone\ Calibration\ Time = \frac{IF_CAL_DWELL_TIME}{SEQ\ CLK}$$

It is recommended that the IF tone calibration time be at least 500 µs. The total time for the IF filter fine calibration is given by

$$IF\ Filter\ Fine\ Calibration\ Time = IF\ Tone\ Calibration\ Time \times 10$$

RSSI/AGC

The RSSI is implemented as a successive compression log amp following the baseband (BB) channel filtering. The log amp achieves ±3 dB log linearity. It also doubles as a limiter to convert the signal-to-digital levels for the FSK demodulator. The offset correction circuit uses the BBOS_CLK_DIVIDE bits (R3_DB[4:5]), which should be set between 1 MHz and 2 MHz. The RSSI level is converted for user readback and for digitally controlled AGC by an 80-level (7-bit) flash ADC. This level can be converted to input power in dBm. By default, the AGC is on when powered up in receive mode.

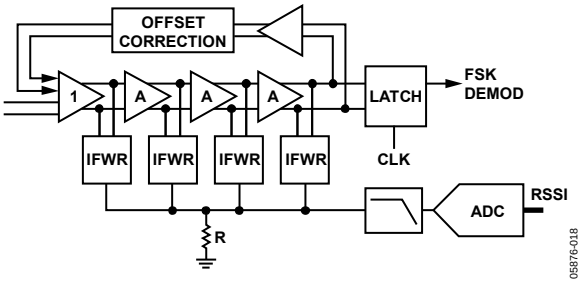


Figure 45. RSSI Block Diagram

RSSI Thresholds

When the RSSI is above AGC_HIGH_THRESHOLD (R9_DB[11:17]), the gain is reduced. When the RSSI is below AGC_LOW_THRESHOLD (R9_DB[4:10]), the gain is increased. The thresholds default to 30 and 70 on power-up in receive mode. A delay (set by AGC_CLOCK_DIVIDE, R3_DB[26:31]) is programmed to allow for settling of the loop. A value of 10 is recommended.

The user has the option of changing the two threshold values from the defaults of 30 and 70 (Register 9). The default AGC setup values should be adequate for most applications. The threshold values must be chosen to be more than 30 apart for the AGC to operate correctly.

Offset Correction Clock

In Register 3, the user should set the BBOS_CLK_DIVIDE bits (R3_DB[4:5]) to give a baseband offset clock (BBOS CLK) frequency between 1 MHz and 2 MHz.

$$BBOS\ CLK\ [\text{Hz}] = XTAL/(BBOS_CLK_DIVIDE)$$

where *BBOS_CLK_DIVIDE* can be set to 4, 8, 16, or 32.

AGC Information and Timing

AGC is selected by default and operates by setting the appropriate LNA and filter gain settings for the measured RSSI level. It is possible to disable AGC by writing to Register 9 if the user wants to enter one of the modes listed in Table 14. The time for the AGC circuit to settle and, therefore, the time it takes to measure the RSSI accurately, is typically 300 µs. However, this depends on how many gain settings the AGC circuit has to cycle through. After each gain change, the AGC loop waits for a programmed time to allow transients to settle. This AGC update rate is set according to

$$AGC\ Update\ Rate\ [\text{Hz}] = \frac{SEQ_CLK_DIVIDE\ [\text{Hz}]}{AGC_CLK_DIVIDE}$$

where:
AGC_CLK_DIVIDE is set by R3_DB[26:31]. A value of 10 is recommended.
SEQ_CLK_DIVIDE = 100 kHz (R3_DB[18:25]).

By using the recommended setting for *AGC_CLK_DIVIDE,* the total AGC settling time is

$$AGC\ Settling\ Time\ [\text{sec}] = \frac{Number\ of\ AGC\ Gain\ Changes}{AGC\ Update\ Rate\ [\text{Hz}]}$$

The worst case for AGC settling is when the AGC control loop has to cycle through all five gain settings, which gives a maximum AGC settling time of 500 µs.

Table 14. LNA/Mixer Modes

Receiver Mode	LNA_MODE (R9_DB25)	LNA_GAIN (R9_DB[20:21])	MIXER_LINEARITY (R9_DB28)	Sensitivity (2FSK, DR = 4.8 kbps, f_{DEV} = 4 kHz)	Rx Current Consumption (mA)	Input IP3 (dBm)
High Sensitivity Mode (Default)	0	30	0	−118	24.6	−24
Enhanced Linearity High Gain	0	30	1	−114.5	24.6	−20
Medium Gain	1	10	0	−112	22.1	−13.5
Enhanced Linearity Medium Gain	1	10	1	−105.5	22.1	−9
Low Gain	1	3	0	−100	22.1	−5
Enhanced Linearity Low Gain	1	3	1	−92.3	22.1	−3

RSSI Formula (Converting to dBm)

The RSSI formula is

Input Power [dBm] =
−130 dBm + (*Readback Code* + *Gain Mode Correction*) × 0.5

where:
Readback Code is given by Bit RV7 to Bit RV1 in the readback register (see the Readback Format section).
Gain Mode Correction is given by the values in Table 15.

The LNA gain (LG2, LG1) and filter gain (FG2, FG1) values are also obtained from the readback register, as part of an RSSI readback.

Table 15. Gain Mode Correction

LNA Gain (LG2, LG1)	Filter Gain (FG2, FG1)	Gain Mode Correction
H (1, 0)	H (1, 0)	0
M (0, 1)	H (1, 0)	24
M (0, 1)	M (0, 1)	38
M (0, 1)	L (0, 0)	58
L (0, 0)	L (0, 0)	86

An additional factor should be introduced to account for losses in the front-end-matching network/antenna.

DEMODULATION, DETECTION, AND CDR

System Overview

An overview of the demodulation, detection, and clock and data recovery (CDR) of the received signal on the ADF7021 is shown in Figure 46.

The quadrature outputs of the IF filter are first limited and then fed to either the correlator FSK demodulator or the linear FSK demodulator. The correlator demodulator is used to demodulate 2FSK, 3FSK, and 4FSK. The linear demodulator is used for frequency measurement and is enabled when the AFC loop is active. The linear demodulator can also be used to demodulate 2FSK.

Following the demodulator, a digital post demodulator filter removes excess noise from the demodulator signal output. Threshold/slicer detection is used for data recovery of 2FSK and 4FSK. Data recovery of 3FSK can be implemented using either threshold detection or Viterbi detection.

An on-chip CDR PLL is used to resynchronize the received bit stream to a local clock. It outputs the retimed data and clock on the TxRxDATA and TxRxCLK pins, respectively.

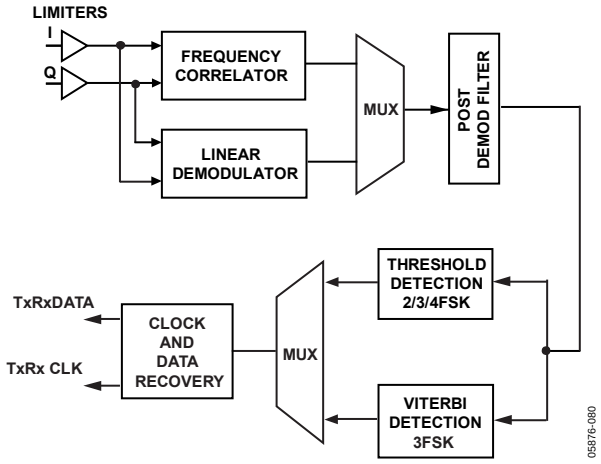


Figure 46. Overview of Demodulation, Detection, and CDR Process

Correlator Demodulator

The correlator demodulator can be used for 2FSK, 3FSK, and 4FSK demodulation. Figure 47 shows the operation of the correlator demodulator for 2FSK.

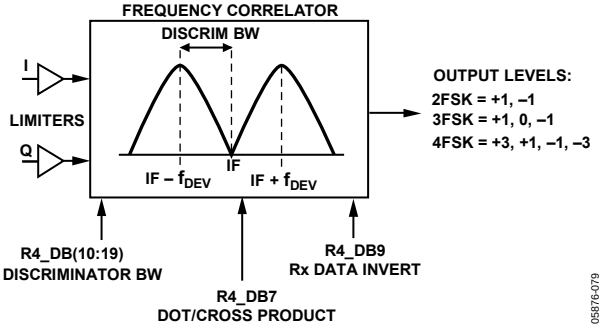


Figure 47. 2FSK Correlator Demodulator Operation

The quadrature outputs of the IF filter are first limited and then fed to a digital frequency correlator that performs filtering and frequency discrimination of the 2FSK/3FSK/4FSK spectrum.

For 2FSK modulation, data is recovered by comparing the output levels from two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of additive white Gaussian noise (AWGN). This method of FSK demodulation provides approximately 3 dB to 4 dB better sensitivity than a linear demodulator.

Linear Demodulator

Figure 48 shows a block diagram of the linear demodulator.

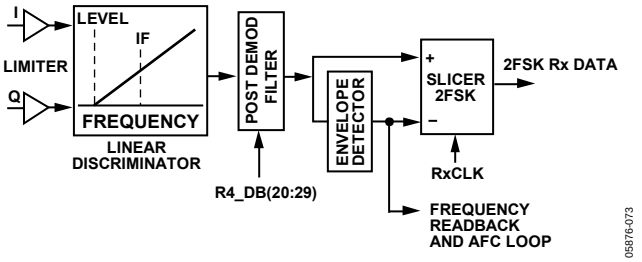


Figure 48. Block Diagram of Linear FSK Demodulator

A digital frequency discriminator provides an output signal that is linearly proportional to the frequency of the limiter outputs. The discriminator output is filtered and averaged using a combined averaging filter and envelope detector. The demodulated 2FSK data from the post demodulator filter is recovered by threshold detecting the envelope detector output, as shown in Figure 48. This method of demodulation corrects for frequency errors between transmitter and receiver when the received spectrum is close to or within the IF bandwidth. This envelope detector output is also used for AFC readback and provides the frequency estimate for the AFC control loop.

Post Demodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this post demodulator filter is programmable and must be optimized for the user's data rate and received modulation type. If the bandwidth is set too narrow, performance degrades due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the performance of the receiver. The POST_DEMODULATOR_BW bits (R4_DB[20:29]) set the bandwidth of this filter.

2FSK Bit Slicer/Threshold Detection

2FSK demodulation can be implemented using the correlator FSK demodulator or the linear FSK demodulator. In both cases, threshold detection is used for data recovery at the output of the post demodulation filter.

The output signal levels of the correlator demodulator are always centered about zero. Therefore, the slicer threshold level can be fixed at zero, and the demodulator performance is independent of the run-length constraints of the transmit data bit stream. This results in robust data recovery that does not suffer from the classic baseline wander problems that exist in the more traditional FSK demodulators.

When the linear demodulator is used for 2FSK demodulation, the output of the envelope detector is used as the slicer threshold, and this output tracks frequency errors that are within the IF filter bandwidth.

3FSK and 4FSK Threshold Detection

4FSK demodulation is implemented using the correlator demodulator followed by the post demodulator filter and threshold detection. The output of the post demodulation filter is a 4-level signal that represents the transmitted symbols (−3, −1, +1, +3). Threshold detection of 4FSK requires three threshold settings, one that is always fixed at 0 and two that are programmable and are symmetrically placed above and below 0 using the 3FSK/4FSK_SLICER_THRESHOLD bits (R13_DB[4:10]).

3FSK demodulation is implemented using the correlator demodulator, followed by a post demodulator filter. The output of the post demodulator filter is a 3-level signal that represents the transmitted symbols (−1, 0, +1). Data recovery of 3FSK can be implemented using threshold detection or Viterbi detection. Threshold detection is implemented using two thresholds that are programmable and are symmetrically placed above and below zero using the 3FSK/4FSK_SLICER_THRESHOLD bits (R13_DB[4:10]).

3FSK Viterbi Detection

Viterbi detection of 3FSK operates on a four-state trellis and is implemented using two interleaved Viterbi detectors operating at half the symbol rate. The Viterbi detector is enabled by R13_DB11.

To facilitate different run length constraints in the transmitted bit stream, the Viterbi path memory length is programmable in steps of 4 bits, 6 bits, 8 bits, or 32 bits by setting the VITERBI_PATH_MEMORY bits (R13_DB[13:14]). This should be set equal to or longer than the maximum number of consecutive 0s in the interleaved transmit bit stream.

When used with Viterbi detection, the receiver sensitivity for 3FSK is typically +3 dB better than that obtained using threshold detection. When the Viterbi detector is enabled, however, the receiver bit latency is increased by twice the Viterbi path memory length.

Clock Recovery

An oversampled digital clock and data recovery (CDR) PLL is used to resynchronize the received bit stream to a local clock in all modulation modes. The oversampled clock rate of the PLL (CDR CLK) must be set at 32 times the symbol rate (see the Register 3—Transmit/Receive Clock Register section). The maximum data/symbol rate tolerance of the CDR PLL is determined by the number of zero-crossing symbol transitions in the transmitted packet. For example, if using 2FSK with a 101010 preamble, a maximum tolerance of ±3.0% of the data rate is achieved. However, this tolerance is reduced during recovery of the remainder of the packet where symbol transitions may not be guaranteed to occur at regular intervals. To maximize the data rate tolerance of the CDR, some form of encoding and/or data scrambling is recommended that guarantees a number of transitions at regular intervals. For

example, using 2FSK with Manchester-encoded data achieves a data rate tolerance of ±2.0%.

The CDR PLL is designed for fast acquisition of the recovered symbols during preamble and typically achieves bit synchronization within 5-symbol transitions of preamble.

In 4FSK modulation, the tolerance using the +3, −3, +3, −3 preamble is ±3% of the symbol rate (or ±1.5% of the data rate). However, this tolerance is reduced during recovery of the remainder of the packet where symbol transitions may not be guaranteed to occur at regular intervals. To maximize the symbol/data rate tolerance, the remainder of the 4FSK packet should be constructed so that the transmitted symbols retain close to dc-free properties by using data scrambling and/or by inserting specific dc balancing symbols that are inserted in the transmitted bit stream at regular intervals such as after every 8 or 16 symbols.

In 3FSK modulation, the linear convolutional encoder scheme guarantees that the transmitted symbol sequence is dc-free, facilitating symbol detection. However, Tx data scrambling is recommended to limit the run length of zero symbols in the transmit bit stream. Using 3FSK, the CDR data rate tolerance is typically ±0.5%.

RECEIVER SETUP

Correlator Demodulator Setup

To enable the correlator for various modulation modes, refer to Table 16.

Table 16. Enabling the Correlator Demodulator

Received Modulation	DEMOD_SCHEME (R4_DB[4:6])
2FSK	001
3FSK	010
4FSK	011

To optimize receiver sensitivity, the correlator bandwidth must be optimized for the specific deviation frequency and modulation used by the transmitter. The discriminator bandwidth is controlled by R4_DB[10:19] and is defined as

$$DISCRIMINATOR_BW = \frac{(DEMOD\ CLK \times K)}{400 \times 10^3}$$

where:
DEMOD CLK is as defined in the Register 3—Transmit/Receive Clock Register section.
K is set for each modulation mode according to the following:

For 2FSK,

$$K = Round\left(\frac{100 \times 10^3}{f_{DEV}}\right)$$

For 3FSK,

$$K = Round\left(\frac{100 \times 10^3}{2 \times f_{DEV}}\right)$$

For 4FSK,

$$K = Round_{4FSK}\left(\frac{100 \times 10^3}{4 \times f_{DEV}}\right)$$

where:
Round is rounded to the nearest integer.
$Round_{4FSK}$ is rounded to the nearest of the following integers: 32, 31, 28, 27, 24, 23, 20, 19, 16, 15, 12, 11, 8, 7, 4, 3.
f_{DEV} is the transmit frequency deviation in Hz. For 4FSK, f_{DEV} is the frequency deviation used for the ±1 symbols (that is, the inner frequency deviations).

To optimize the coefficients of the correlator, R4_DB7 and R4_DB[8:9] must also be assigned. The value of these bits depends on whether K is odd or even. These bits are assigned according to Table 17 and Table 18.

Table 17. Assignment of Correlator K Value for 2FSK and 3FSK

K	K/2	(K + 1)/2	R4_DB7	R4_DB[8:9]
Even	Even	N/A	0	00
Even	Odd	N/A	0	10
Odd	N/A	Even	1	00
Odd	N/A	Odd	1	10

Table 18. Assignment of Correlator K Value for 4FSK

K	R4_DB7	R4_DB[8:9]
Even	0	00
Odd	1	00

Linear Demodulator Setup

The linear demodulator can be used for 2FSK demodulation. To enable the linear demodulator, set the DEMOD_SCHEME bits (R4_DB[4:6]) to 000.

Post Demodulator Filter Setup

The 3 dB bandwidth of the post demodulator filter should be set according to the received modulation type and data rate. The bandwidth is controlled by R4_DB[20:29] and is given by

$$POST_DEMOD_BW = \frac{2^{11} \times \pi \times f_{CUTOFF}}{DEMOD\ CLK}$$

where f_{CUTOFF} is the target 3 dB bandwidth in Hz of the post demodulator filter.

Table 19. Post Demodulator Filter Bandwidth Settings for 2FSK/3FSK/4FSK Modulation Schemes

Received Modulation	Post Demodulator Filter Bandwidth, f_{CUTOFF} (Hz)
2FSK	0.75 × data rate
3FSK	1 × data rate
4FSK	1.6 × symbol rate (= 0.8 × data rate)

3FSK Viterbi Detector Setup

The Viterbi detector can be used for 3FSK data detection. This is activated by setting R13_DB11 to Logic 1.

The Viterbi path memory length is programmable in steps of 4, 6, 8, or 32 bits (VITERBI_PATH_MEMORY, R13_DB[13:14]).

The path memory length should be set equal to or greater than the maximum number of consecutive 0s in the interleaved transmit bit stream.

The Viterbi detector also uses threshold levels to implement the maximum likelihood detection algorithm. These thresholds are programmable via the 3FSK/4FSK_SLICER_THRESHOLD bits (R13_DB[4:10]).

These bits are assigned as follows:

$$3FSK/4FSK_SLICER_THRESHOLD = 57 \times \left(\frac{Transmit\ Frequency\ Deviation \times K}{100 \times 10^3} \right)$$

where K is the value calculated for correlator discriminator bandwidth.

3FSK Threshold Detector Setup

To activate threshold detection of 3FSK, R13_DB11 should be set to Logic 0. The 3FSK/4FSK_SLICER_THRESHOLD bits (R13_DB[4:10]) should be set as outlined in the 3FSK Viterbi Detector Setup section.

3FSK CDR Setup

In 3FSK, a transmit preamble of at least 40 bits of continuous 1s is recommended to ensure a maximum number of symbol transitions for the CDR to acquire lock.

The clock and data recovery for 3FSK requires a number of parameters in Register 13 to be set (see Table 20).

4FSK Threshold Detector Setup

The threshold for the 4FSK detector is set using the 3FSK/4FSK_SLICER_THRESHOLD bits (R13_DB[4:10]). The threshold should be set according to

$$3FSK/4FSK_SLICER_THRESHOLD = 78 \times \left(\frac{4FSK\ Outer\ Tx\ Deviation \times K}{100 \times 10^3} \right)$$

where K is the value calculated for correlator discriminator bandwidth.

Table 20. 3FSK CDR Settings

Parameter	Recommended Setting	Purpose
PHASE_CORRECTION (R13_DB12)	1	Phase correction on
3FSK_CDR_THRESHOLD (R13_DB[15:21])	$62 \times \left(\frac{Transmit\ Frequency\ Deviation \times K}{100 \times 10^3} \right)$ where K is the value calculated for correlator discriminator bandwidth.	Sets CDR decision threshold levels
3FSK_PREAMBLE_TIME_VALIDATE (R13_DB [22:25])	1111	Preamble detector time qualifier

DEMODULATOR CONSIDERATIONS

2FSK Preamble

The recommended preamble bit pattern for 2FSK is a dc-free pattern (such as a 10101010… pattern). Preamble patterns with longer run-length constraints (such as 11001100…) can also be used but result in a longer synchronization time of the received bit stream in the receiver. The preamble needs to allow enough bits for AGC settling of the receiver and CDR acquisition. A minimum of 16 preamble bits is recommended. When the receiver is using the internal AFC, the minimum recommended number of preamble bits is 48.

The remaining fields that follow the preamble header do not have to use dc-free coding. For these fields, the ADF7021 can accommodate coding schemes with a run length of up to eight bits without any performance degradation. If longer run lengths are required, an encoding scheme such as 8B/10B or Manchester encoding is recommended.

4FSK Preamble and Data Coding

The recommended preamble bit pattern for 4FSK is a repeating 00100010… bit sequence. This 2-level sequence of repeating −3, +3, −3, +3 symbols is dc-free and maximizes the symbol timing performance and data recovery of the 4FSK preamble in the receiver. The minimum recommended length of the preamble is 32 bits (16 symbols).

The remainder of the 4FSK packet should be constructed so that the transmitted symbols retain close to dc-free property by using data scrambling and/or by inserting specific dc balancing symbols in the transmitted bit stream at regular intervals, such as after every 8 or 16 symbols.

2FSK Correlator Demodulator and Frequency Errors

The ADF7021 has a number of options to combat frequency errors that exist due to mismatches between the transmit and receive crystals/TCXOs.

With AFC disabled, the correlator demodulator is tolerant to frequency errors over the $\pm 0.4 \times f_{DEV}$ range, where f_{DEV} is the FSK frequency deviation. For larger frequency errors, the frequency tolerance can be widened to $\pm 0.8 \times f_{DEV}$ by adjusting the value of K and thus doubling the correlator bandwidth.

K should then be calculated as

$$K = Round\left(\frac{100 \times 10^3}{2 \times f_{DEV}}\right)$$

The DISCRIMINATOR_BW setting should also be recalculated using the new K value. Doubling the correlator bandwidth to improve frequency error tolerance in this manner typically results in a 1 dB to 2 dB loss in receiver sensitivity.

Correlator Demodulator and Low Modulation Indices

The modulation index in 2FSK is defined as

$$Modulation\ Index = \frac{2 \times f_{DEV}}{Data\ Rate}$$

The receiver sensitivity performance can be maximized at low modulation index by increasing the discriminator bandwidth of the correlator demodulator. For modulation indices of less than 0.4, it is recommended to double the correlator bandwidth by calculating K as follows:

$$K = Round\left(\frac{100\ e\ 3}{2 \times f_{DEV}}\right)$$

The DISCRIMINATOR_BW should be recalculated using the new K value. Figure 26 highlights the improved sensitivity that can be achieved for 2FSK modulation, at low modulation indices, by doubling the correlator bandwidth.

AFC OPERATION

The ADF7021 also supports a real-time AFC loop that is used to remove frequency errors due to mismatches between the transmit and receive crystals/TCXOs. The AFC loop uses the linear frequency discriminator block to estimate frequency errors. The linear FSK discriminator output is filtered and averaged to remove the FSK frequency modulation using a combined averaging filter and envelope detector. In receive mode, the output of the envelope detector provides an estimate of the average IF frequency.

Two methods of AFC supported on the ADF7021 are external and internal.

External AFC

Here, the user reads back the frequency information through the ADF7021 serial port and applies a frequency correction value to the fractional-N synthesizer-N divider.

The frequency information is obtained by reading the 16-bit signed AFC readback, as described in the Readback Format section, and by applying the following formula:

$$Frequency\ Readback\ [\text{Hz}] = (AFC_READBACK \times DEMOD\ CLK)/2^{18}$$

Although the AFC_READBACK value is a signed number, under normal operating conditions, it is positive. In the absence of frequency errors, the frequency readback value is equal to the IF frequency of 100 kHz.

Internal AFC

The ADF7021 supports a real-time, internal, automatic frequency control loop. In this mode, an internal control loop automatically monitors the frequency error and adjusts the synthesizer-N divider using an internal proportional integral (PI) control loop.

The internal AFC control loop parameters are controlled in Register 10. The internal AFC loop is activated by setting R10_DB4 to 1. A scaling coefficient must also be entered, based on the crystal frequency in use. This is set up in R10_DB[5:16] and should be calculated using

$$AFC_SCALING_FACTOR = Round\left(\frac{2^{24} \times 500}{XTAL}\right)$$

Maximum AFC Range

The maximum frequency correction range of the AFC loop is programmable on the ADF7021. This is set by R10_DB[24:31]. The maximum AFC correction range is the difference in frequency between the upper and lower limits of the AFC tuning range. For example, if the maximum AFC correction range is set to 10 kHz, the AFC can adjust the receiver LO within the
f_{LO} ± 5 kHz range.

However, when RF_DIVIDE_BY_2 (R1_DB18) is enabled, the programmed range is halved. The user should account for this halving by doubling the programmed maximum AFC range.

The recommended maximum AFC correction range should be ≤ 1.5 × IF filter bandwidth. If the maximum frequency correction range is set to be > 1.5 × IF bandwidth, the attenuation of the IF filter can degrade the AFC loop sensitivity.

The adjacent channel rejection (ACR) performance of the receivers can be degraded when AFC is enabled and the AFC correction range is close to the IF filter bandwidth. However, because the AFC correction range is programmable, the user can trade off correction range and ACR performance.

When AFC errors are removed using either the internal or external AFC, further improvement in receiver sensitivity can be obtained by reducing the IF filter bandwidth using the IF_BW bits (R4_DB[30:31]).

AUTOMATIC SYNC WORD DETECTION (SWD)

The ADF7021 also supports automatic detection of the sync or ID fields. To activate this mode, the sync (or ID) word must be preprogrammed into the ADF7021. In receive mode, this preprogrammed word is compared to the received bit stream. When a valid match is identified, the external SWD pin is asserted by the ADF7021 on the next Rx clock pulse.

This feature can be used to alert the microprocessor that a valid channel has been detected. It relaxes the computational requirements of the microprocessor and reduces the overall power consumption.

The SWD signal can also be used to frame the received packet by staying high for a preprogrammed number of bytes. The data packet length can be set in R12_DB[8:15].

The SWD pin status can be configured by setting R12_DB[6:7]. R11_DB[4:5] are used to set the length of the sync/ID word, which can be 12, 16, 20, or 24 bits long. A value of 24 bits is recommended to minimize false sync word detection in the receiver that can occur during recovery of the remainder of the packet or when noise/no signal is present at the receiver input. The transmitter must transmit the sync byte MSB first and the LSB last to ensure proper alignment in the receiver sync-byte-detection hardware.

An error tolerance parameter can also be programmed that accepts a valid match when up to 3 bits of the word are incorrect. The error tolerance value is assigned in R11_DB[6:7].

APPLICATIONS INFORMATION

IF FILTER BANDWIDTH CALIBRATION

The IF filter should be calibrated on every power-up in receive mode to correct for errors in the bandwidth and filter center frequency due to process variations. The automatic calibration requires no external intervention once it is initiated by a write to Register 5. Depending on numerous factors, such as IF filter bandwidth, received signal bandwidth, and temperature variation, the user must determine whether to carry out a coarse calibration or a fine calibration. For information on calibration setup, refer to the IF Filter section.

The performance of both calibration methods is outlined in Table 21.

Table 21. IF Filter Calibration Specifications

Filter Calibration Method	Center Frequency Accuracy[1]	Calibration Time (Typ)
Coarse Cal	100 kHz ± 2.5 kHz	200 µs
Fine Cal	100 kHz ± 0.5 kHz	5.2 ms

[1] After calibration.

When to Use Coarse Calibration

It is recommended to perform a coarse calibration on every receive mode power-up. This calibration typically takes 200 µs. The FILTER_CAL_COMPLETE signal from MUXOUT can be used to monitor the filter calibration duration or to signal the end of calibration. The ADF7021 should not be accessed during calibration.

When to Use a Fine Calibration

In cases where the receive signal bandwidth is very close to the bandwidth of the IF filter, it is recommended to perform a fine filter calibration every time the unit powers up in receive mode.

A fine calibration should be performed if

$$OBW + Coarse\ Calibration\ Variation > IF_FILTER_BW$$

where:
OBW is the 99% occupied bandwidth of the transmit signal.
Coarse Calibration Variation is 2.5 kHz.
IF_FILTER_BW is set by R4_DB[30:31].

The FILTER_CAL_COMPLETE signal from MUXOUT (set by R0_DB[29:31]) can be used to monitor the filter calibration duration or to signal the end of calibration. A coarse filter calibration is automatically performed prior to a fine filter calibration.

When to Use Single Fine Calibration

In applications where the receiver powers up numerous times in a short period, it is only necessary to perform a one-time fine calibration on the initial receiver power-up.

After the initial coarse calibration and fine calibration, the result of the fine calibration can be read back through the serial interface using the FILTER_CAL_READBACK result (refer to the Filter Bandwidth Calibration Readback section). On subsequent power-ups in receive mode, the filter is manually adjusted using the previous fine filter calibration result. This manual adjust is performed using the IF_FILTER_ADJUST bits (R5_DB[14:19]).

This method should only be used if the successive power-ups in receive mode are over a short duration, during which time there is little variation in temperature (>15°C).

IF Filter Variation with Temperature

When calibrated, the filter center frequency can vary with changes in temperature. If the ADF7021 is used in an application where it remains in receive mode for a considerable length of time, the user must consider this variation of filter center frequency with temperature. This variation is typically 0.7 kHz per 10°C, which means that if a coarse filter calibration and fine filter calibration are performed at 25°C, the initial maximum error is ±0.5 kHz, and the maximum possible change in the filter center frequency over temperature (−40°C and +85°C) is ±4.5 kHz. This gives a total error of ±5 kHz.

If the receive signal occupied bandwidth is considerably less than the IF filter bandwidth, the variation of filter center frequency over the operating temperature range may not be an issue. Alternatively, if the IF filter bandwidth is not wide enough to tolerate the variation with temperature, a periodic filter calibration can be performed, or alternatively, the on-chip temperature sensor can be used to determine when a filter calibration is necessary by monitoring for changes in temperature.

LNA/PA MATCHING

The ADF7021 exhibits optimum performance in terms of sensitivity, transmit power, and current consumption, only if its RF input and output ports are properly matched to the antenna impedance. For cost sensitive applications, the ADF7021 is equipped with an internal Rx/Tx switch that facilitates the use of a simple, combined passive PA/LNA matching network. Alternatively, an external Rx/Tx switch such as the ADG919 can be used, which yields a slightly improved receiver sensitivity and lower transmitter power consumption.

Internal Rx/Tx Switch

Figure 49 shows the ADF7021 in a configuration where the internal Rx/Tx switch is used with a combined LNA/PA matching network. This is the configuration used on the EVAL-ADF7021DBX evaluation board. For most applications, the slight performance degradation of 1 dB to 2 dB caused by the internal Rx/Tx switch is acceptable, allowing the user to take advantage of the cost saving potential of this solution. The design of the combined matching network must compensate for the reactance presented by the networks in the Tx and the Rx paths, taking the state of the Rx/Tx switch into consideration.

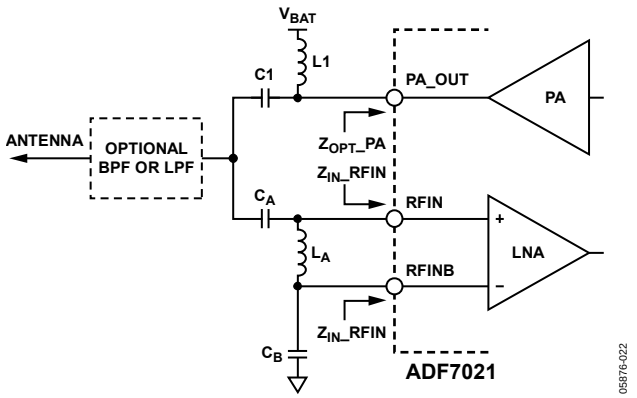


Figure 49. ADF7021 with Internal Rx/Tx Switch

The procedure typically requires several iterations until an acceptable compromise has been reached. The successful implementation of a combined LNA/PA matching network for the ADF7021 is critically dependent on the availability of an accurate electrical model for the PCB. In this context, the use of a suitable CAD package is strongly recommended. To avoid this effort, a small form-factor reference design for the ADF7021 is provided, including matching and harmonic filter components. The design is on a 2-layer PCB to minimize cost. Gerber files are available at www.analog.com.

External Rx/Tx Switch

Figure 50 shows a configuration using an external Rx/Tx switch. This configuration allows an independent optimization of the matching and filter network in the transmit and receive path. Therefore, it is more flexible and less difficult to design than the configuration using the internal Rx/Tx switch. The PA is biased through Inductor L1, while C1 blocks dc current. Together, L1 and C1 form the matching network that transforms the source impedance into the optimum PA load impedance, Z_{OPT}_PA.

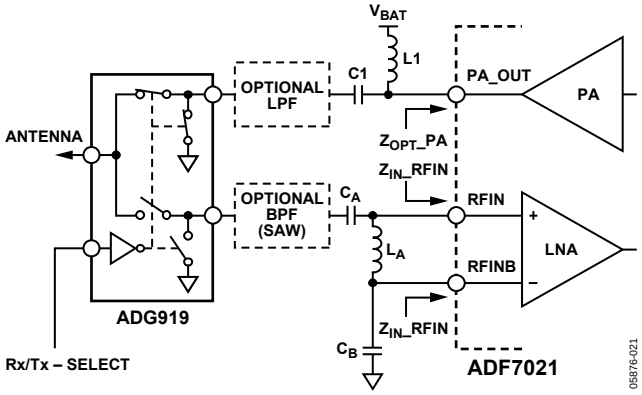


Figure 50. ADF7021 with External Rx/Tx Switch

Z_{OPT}_PA depends on various factors, such as the required output power, the frequency range, the supply voltage range, and the temperature range. Selecting an appropriate Z_{OPT}_PA helps to minimize the Tx current consumption in the application. Application Note AN-764 contains a number of Z_{OPT}_PA values for representative conditions. Under certain conditions, however, it is recommended to obtain a suitable Z_{OPT}_PA value by means of a load-pull measurement.

Due to the differential LNA input, the LNA matching network must be designed to provide both a single-ended-to-differential conversion and a complex, conjugate impedance match. The network with the lowest component count that can satisfy these requirements is the configuration shown in Figure 50, consisting of two capacitors and one inductor. A first-order implementation of the matching network can be obtained by understanding the arrangement as two L-type matching networks in a back-to-back configuration. Due to the asymmetry of the network with respect to ground, a compromise between the input reflection coefficient and the maximum differential signal swing at the LNA input must be established. The use of appropriate CAD software is strongly recommended for this optimization.

Depending on the antenna configuration, the user may need a harmonic filter at the PA output to satisfy the spurious emission requirement of the applicable government regulations. The harmonic filter can be implemented in various ways, such as a discrete LC pi or T-stage filter. Dielectric low-pass filter components, such as the LFL18924MTC1A052 (for operation in the 915 MHz and 868 MHz band) by Murata Manufacturing Co. Ltd., represent an attractive alternative to discrete designs. The immunity of the ADF7021 to strong out-of-band interference can be improved by adding a band-pass filter in the Rx path. Apart from discrete designs, SAW or dielectric filter components such as the SAFCH869MAM0T00, SAFCH915MAL0N00, DCFB2869MLEJAA-TT1, or DCFB3915MLDJAA-TT1, all by Murata Manufacturing Co. Ltd., are well-suited for this purpose. Alternatively, the ADF7021 blocking performance can be improved by selecting one of the enhanced linearity modes, as described in Table 14.

IMAGE REJECTION CALIBRATION

The image channel in the ADF7021 is 200 kHz below the desired signal. The polyphase filter rejects this image with an asymmetric frequency response. The image rejection performance of the receiver is dependent on how well matched the I and Q signals are in amplitude, and how well matched the quadrature is between them (that is, how close to 90° apart they are). The uncalibrated image rejection performance is approximately 29 dB (at 450 MHz). However, it is possible to improve on this performance by as much as 20 dB by finding the optimum I/Q gain and phase adjust settings.

Calibration Using Internal RF Source

With the LNA powered off, an on-chip generated, low level RF tone is applied to the mixer inputs. The LO is adjusted to make the tone fall at the image frequency where it is attenuated by the image rejection of the IF filter. The power level of this tone is then measured using the RSSI readback. The I/Q gain and phase adjust DACs (R5_DB[20:31]) are adjusted and the RSSI is remeasured. This process is repeated until the optimum values for the gain and phase adjust are found that provide the lowest RSSI readback level, thereby maximizing the image rejection performance of the receiver.

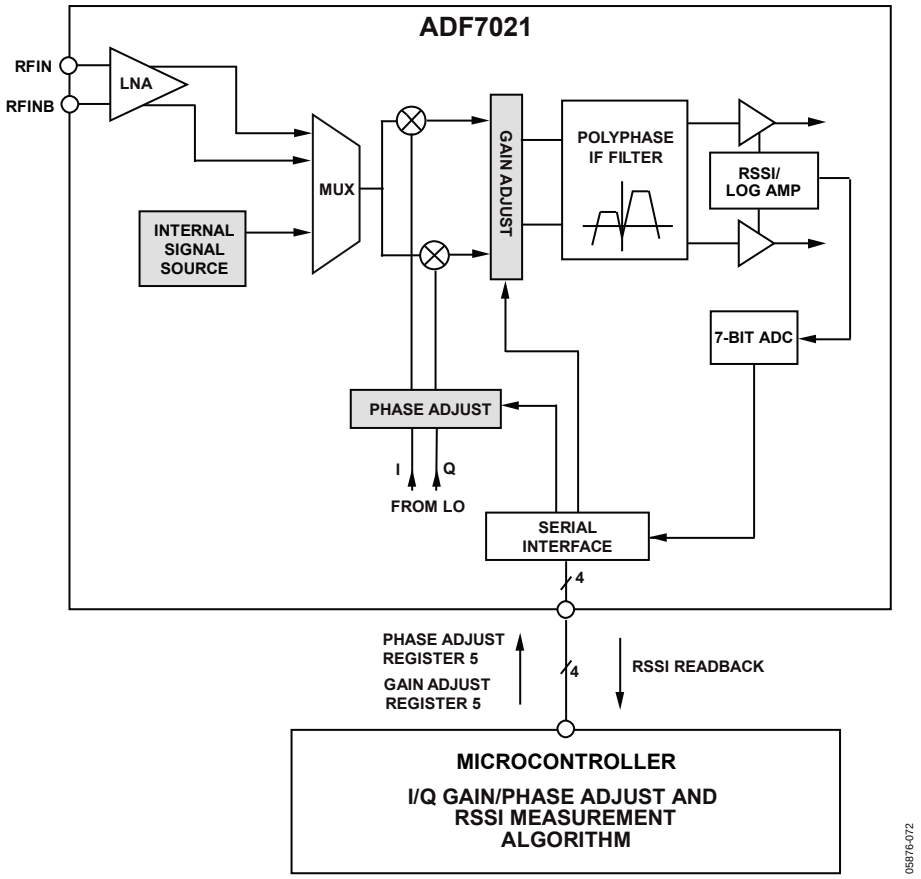


Figure 51. Image Rejection Calibration Using the Internal Calibration Source and a Microcontroller

Using the internal RF source, the RF frequencies that can be utilized for image calibration are programmable and are odd multiples of the reference frequency.

Calibration Using External RF Source

IR calibration can also be implemented using an external RF source. The IR calibration procedure is the same as that used for the internal RF source, except that an RF tone is applied to the LNA input.

Calibration Procedure and Setup

The IR calibration algorithm available from Analog Devices, Inc. is based on a low complexity, 2D optimization algorithm that can be implemented in an external microprocessor or microcontroller.

To enable the internal RF source, the IR_CAL_SOURCE_ DRIVE_LEVEL bits (R6_DB[28:29]) should be set to the maximum level. The LNA should be set to its minimum gain setting, and the AGC should be disabled if the internal source is being used. Alternatively, an external RF source can be used.

The magnitude of the phase adjust is set by using the IR_PHASE_ ADJUST_MAG bits (R5_DB[20:23]). This correction can be applied to either the I channel or Q channel, depending on the value of the IR_PHASE_ADJUST_DIRECTION bit (R5_DB24).

The magnitude of the I/Q gain is adjusted by the IR_GAIN_ ADJUST_MAG bits (R5_DB[25:29]). This correction can be applied to either the I or Q channel, depending on the value of IR_GAIN_ADJUST_I/Q bit (R5_DB30), whereas the IR_GAIN_ADJUST_UP/DN bit (R5_DB31) sets whether the gain adjustment defines a gain or an attenuation adjust.

The calibration results are valid over changes in the ADF7021 supply voltage. However, there is some variation with temperature. A typical plot of variation in image rejection over temperature after initial calibrations at −40°C, +25°C, and +85°C is shown in Figure 52. The internal temperature sensor on the ADF7021 can be used to determine if a new IR calibration is required.

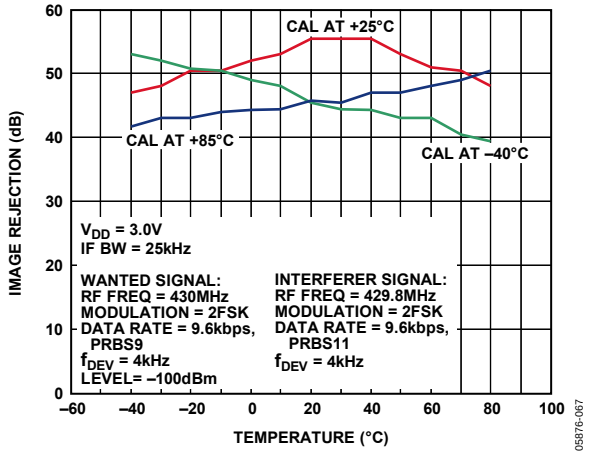


Figure 52. Image Rejection Variation with Temperature after Initial Calibrations at −40°C, +25°C, and +85°C

PACKET STRUCTURE AND CODING

The suggested packet structure to use with the ADF7021 is shown in Figure 53.

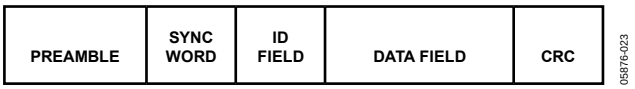


Figure 53. Typical Format of a Transmit Protocol

Refer to the Receiver Setup section for information on the required preamble structure and length for the various modulation schemes.

PROGRAMMING AFTER INITIAL POWER-UP

Table 22 lists the minimum number of writes needed to set up the ADF7021 in either Tx or Rx mode after CE is brought high. Additional registers can also be written to tailor the part to a particular application, such as setting up sync byte detection or enabling AFC. When going from Tx to Rx or vice versa, the user needs to toggle the Tx/Rx bit and write only to Register 0 to alter the LO by 100 kHz.

Table 22. Minimum Register Writes Required for Tx/Rx Setup

Mode	Registers				
Tx	Reg 1	Reg 3	Reg 0	Reg 2	
Rx	Reg 1	Reg 3	Reg 0	Reg 5	Reg 4
Tx to Rx and Rx to Tx	Reg 0				

The recommended programming sequences for transmit and receive are shown in Figure 54 and Figure 55, respectively. The difference in the power-up routine for a TCXO and XTAL reference is shown in these figures.

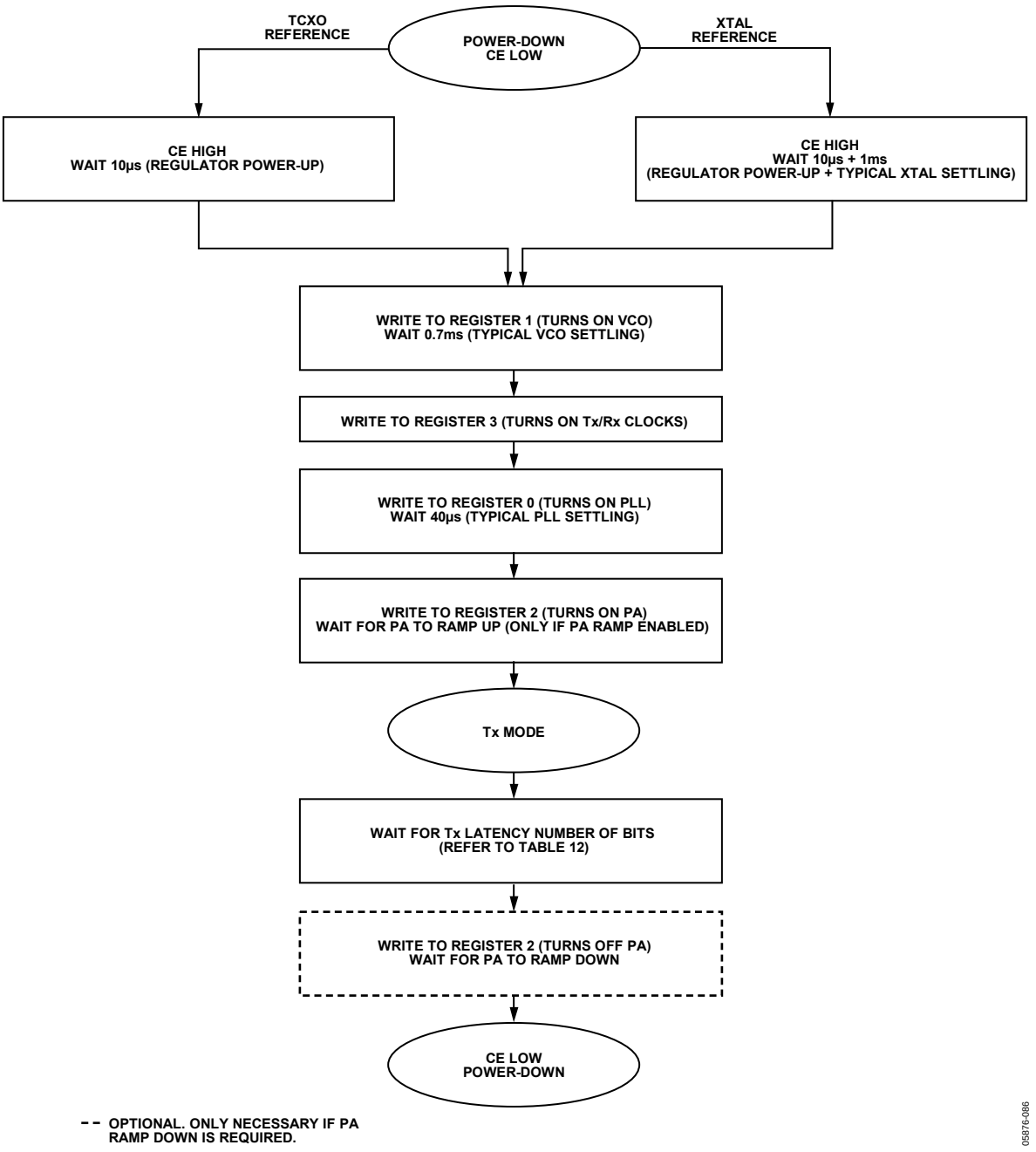


Figure 54. Power-Up Sequence for Transmit Mode

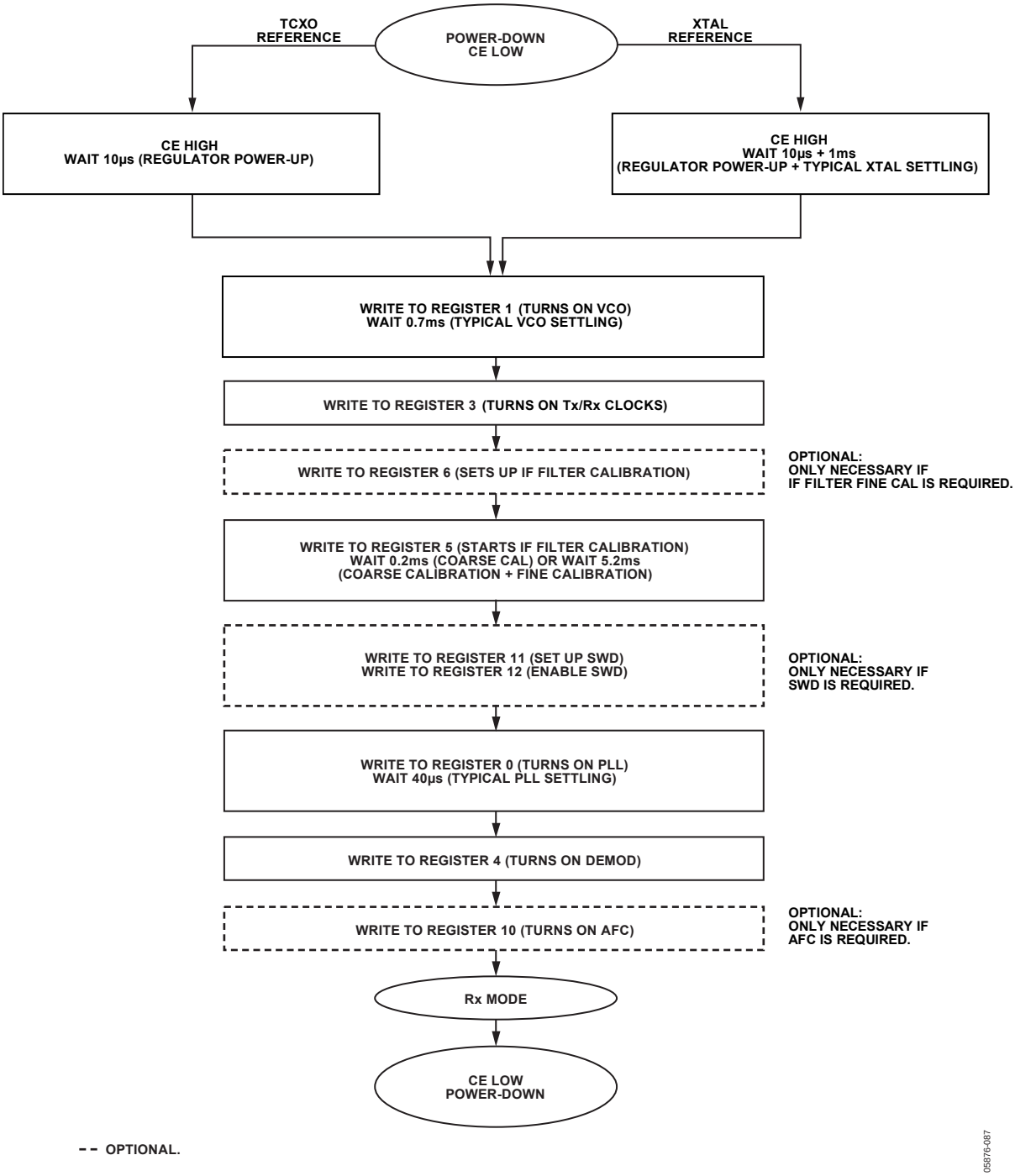
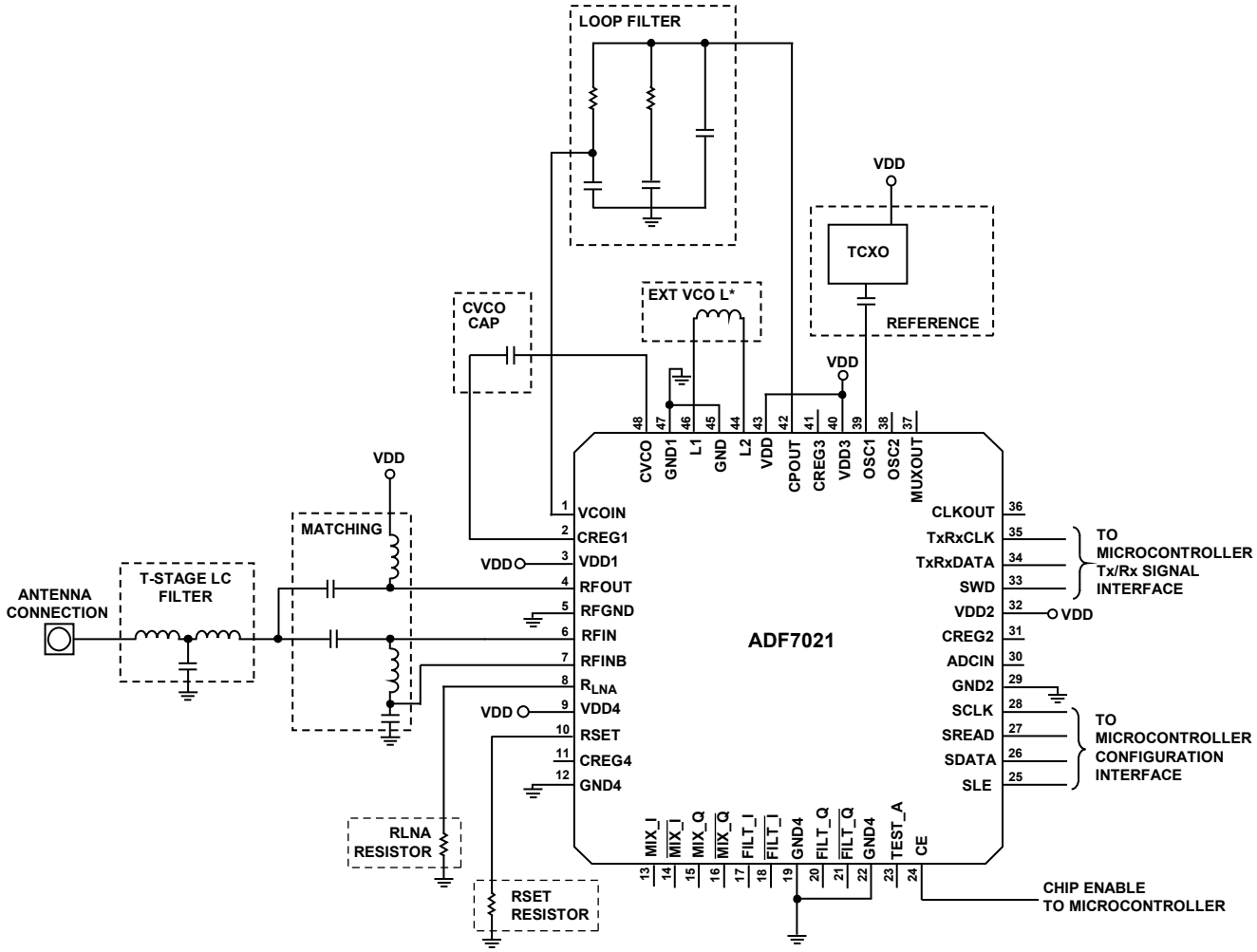


Figure 55. Power-Up Sequence for Receive Mode

APPLICATONS CIRCUIT

The ADF7021 requires very few external components for operation. Figure 56 shows the recommended application circuit. Note that the power supply decoupling and regulator capacitors are omitted for clarity.

For recommended component values, refer to the ADF7021 evaluation board data sheet and AN-915 application note accessible from the ADF7021 product page. Follow the reference design schematic closely to ensure optimum performance in narrow-band applications.



*PIN 44 AND PIN 46 CAN BE LEFT FLOATING IF EXTERNAL INDUCTOR VCO IS NOT USED.

NOTES
1. PINS [13:18], PINS [20:21], AND PIN 23 ARE TEST PINS AND ARE NOT USED IN NORMAL OPERATION.

Figure 56. Typical Application Circuit (Regulator Capacitors and Power Supply Decoupling Not Shown)

SERIAL INTERFACE

The serial interface allows the user to program the 16-/32-bit registers using a 3-wire interface (SCLK, SDATA, and SLE). It consists of a level shifter, 32-bit shift register, and 16 latches. Signals should be CMOS compatible. The serial interface is powered by the regulator, and, therefore, is inactive when CE is low.

Data is clocked into the register, MSB first, on the rising edge of each clock (SCLK). Data is transferred to one of 16 latches on the rising edge of SLE. The destination latch is determined by the value of the four control bits (C4 to C1); these are the bottom 4 LSBs, DB3 to DB0, as shown in Figure 2. Data can also be read back on the SREAD pin.

READBACK FORMAT

The readback operation is initiated by writing a valid control word to the readback register and enabling the READBACK bit (R7_DB8 = 1). The readback can begin after the control word has been latched with the SLE signal. SLE must be kept high while the data is being read out. Each active edge at the SCLK pin successively clocks the readback word out at the SREAD pin, as shown in Figure 57, starting with the MSB first. The data appearing at the first clock cycle following the latch operation must be ignored. An extra clock cycle is needed after the 16th readback bit to return the SREAD pin to tristate. Therefore, 18 total clock cycles are needed for each read back. After the 18th clock cycle, SLE should be brought low.

AFC Readback

The AFC readback is valid only during the reception of FSK signals with either the linear or correlator demodulator active. The AFC readback value is formatted as a signed 16-bit integer comprising Bit RV1 to Bit RV16 and is scaled according to the following formula:

$$FREQ\ RB\ [\text{Hz}] = (AFC_READBACK \times DEMOD\ CLK)/2^{18}$$

In the absence of frequency errors, FREQ RB is equal to the IF frequency of 100 kHz. Note that, for the AFC readback to yield a valid result, the down converted input signal must not fall outside the bandwidth of the analog IF filter. At low input signal levels, the variation in the readback value can be improved by averaging.

RSSI Readback

The format of the readback word is shown in Figure 57. It comprises the RSSI-level information (Bit RV1 to Bit RV7), the current filter gain (FG1, FG2), and the current LNA gain (LG1, LG2) setting. The filter and LNA gain are coded in accordance with the definitions in the Register 9—AGC Register section. For signal levels below −100 dBm, averaging the measured RSSI values improves accuracy. The input power can be calculated from the RSSI readback value as outlined in the RSSI/AGC section.

Battery Voltage/ADCIN/Temperature Sensor Readback

The battery voltage is measured at Pin VDD4. The readback information is contained in Bit RV1 to Bit RV7. This also applies for the readback of the voltage at the ADCIN pin and the temperature sensor. From the readback information, the battery or ADCIN voltage can be determined using

$$V_{BATTERY} = (BATTERY_VOLTAGE_READBACK)/21.1$$

$$V_{ADCIN} = (ADCIN_VOLTAGE_READBACK)/42.1$$

The temperature can be calculated using

$$Temp\ [°\text{C}] = -40 + (68.4 - TEMP_READBACK) \times 9.32$$

Silicon Revision Readback

The silicon revision readback word is valid without setting any other registers. The silicon revision word is coded with four quartets in BCD format. The product code (PC) is coded with three quartets extending from Bit RV5 to Bit RV16. The revision code (RC) is coded with one quartet extending from Bit RV1 to Bit RV4. The product code for the ADF7021 should read back as PC = 0x210. The current revision code should read as RC = 0x4.

Filter Bandwidth Calibration Readback

The filter calibration readback word is contained in Bit RV1 to Bit RV8. This readback can be used for manual filter adjust, thereby avoiding the need to do an IF filter calibration in some instances. The manual adjust value is programmed by R5_DB[14:19]. To calculate the manual adjust based on a filter calibration readback, use the following formula:

$$IF_FILTER_ADJUST = FILTER_CAL_READBACK - 128$$

The result should be programmed into R5_DB[14:19] as outlined in the Register 5—IF Filter Setup Register section.

READBACK MODE	READBACK VALUE															
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AFC READBACK	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
RSSI READBACK	X	X	X	X	X	LG2	LG1	FG2	FG1	RV7	RV6	RV5	RV4	RV3	RV2	RV1
BATTERY VOLTAGE/ADCIN/ TEMP. SENSOR READBACK	X	X	X	X	X	X	X	X	X	RV7	RV6	RV5	RV4	RV3	RV2	RV1
SILICON REVISION	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
FILTER CAL READBACK	0	0	0	0	0	0	0	0	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1

05876-029

Figure 57. Readback Value Table

INTERFACING TO MICROCONTROLLER/DSP

Standard Transmit/Receive Data Interface

The standard transmit/receive signal and configuration interface to a microcontroller is shown in Figure 58. In transmit mode, the ADF7021 provides the data clock on the TxRxCLK pin, and the TxRxDATA pin is used as the data input. The transmit data is clocked into the ADF7021 on the rising edge of TxRxCLK.

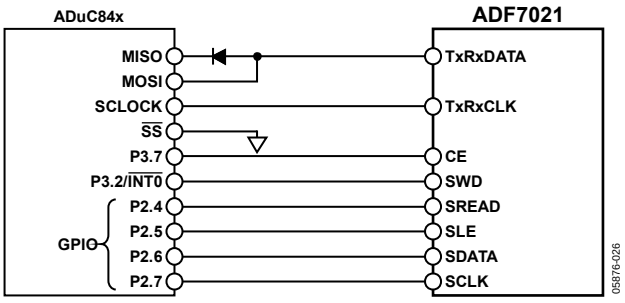


Figure 58. ADuC84x to ADF7021 Connection Diagram

In receive mode, the ADF7021 provides the synchronized data clock on the TxRxCLK pin. The receive data is available on the TxRxDATA pin. The rising edge of TxRxCLK should be used to clock the receive data into the microcontroller. Refer to Figure 4 and Figure 5 for the relevant timing diagrams.

In 4FSK transmit mode, the MSB of the transmit symbol is clocked into the ADF7021 on the first rising edge of the data clock from the TxRxCLK pin. In 4FSK receive mode, the MSB of the first payload symbol is clocked out on the first negative edge of the data clock after the SWD, and should be clocked into the microcontroller on the following rising edge. Refer to Figure 6 and Figure 7 for the relevant timing diagrams.

UART Mode

In UART mode, the TxRxCLK pin is configured to input transmit data in transmit mode. In receive mode, the receive data is available on the TxRxDATA pin, thus providing an asynchronous data interface. The UART mode can only be used with oversampled 2FSK. Figure 59 shows a possible interface to a microcontroller using the UART mode of the ADF7021. To enable this UART interface mode, set R0_DB28 high. Figure 8 and Figure 9 show the relevant timing diagrams for UART mode.

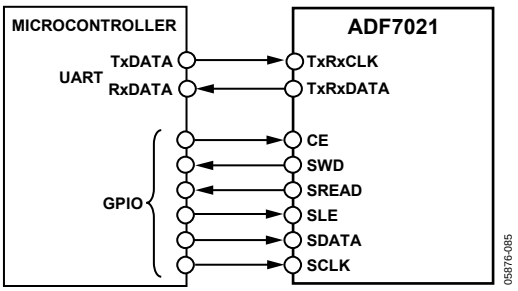


Figure 59. ADF7021(UART Mode) to Asynchronous Microcontroller Interface

SPI Mode

In SPI mode, the TxRxCLK pin is configured to input transmit data in transmit mode. In receive mode, the receive data is available on the TxRxDATA pin. The data clock in both transmit and receive modes is available on the CLKOUT pin. In transmit mode, data is clocked into the ADF7021 on the positive edge of CLKOUT. In receive mode, the TxRxDATA data pin should be sampled by the microcontroller on the positive edge of the CLKOUT.

To enable SPI interface mode, set R0_DB28 high and set R15_DB[17:19] to 0x7. Figure 8 and Figure 9 show the relevant timing diagrams for SPI mode, while Figure 60 shows the recommended interface to a microcontroller using the SPI mode of the ADF7021.

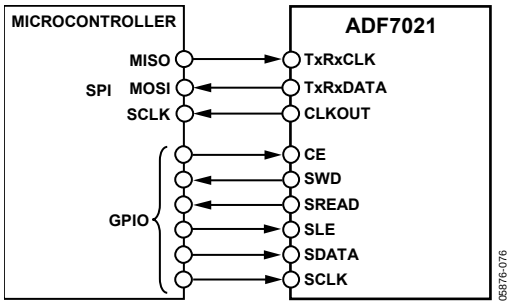


Figure 60. ADF7021 (SPI Mode) to Microcontroller Interface

ADSP-BF533 interface

The suggested method of interfacing to the Blackfin® ADSP-BF533 is given in Figure 61.

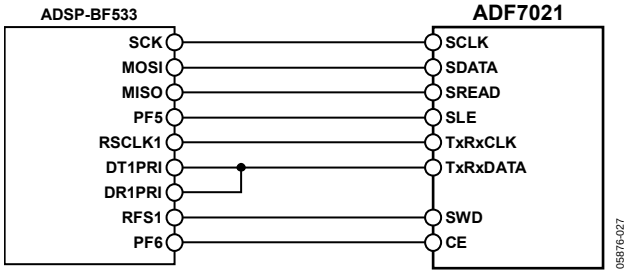


Figure 61. ADSP-BF533 to ADF7021 Connection Diagram

REGISTER 0—N REGISTER

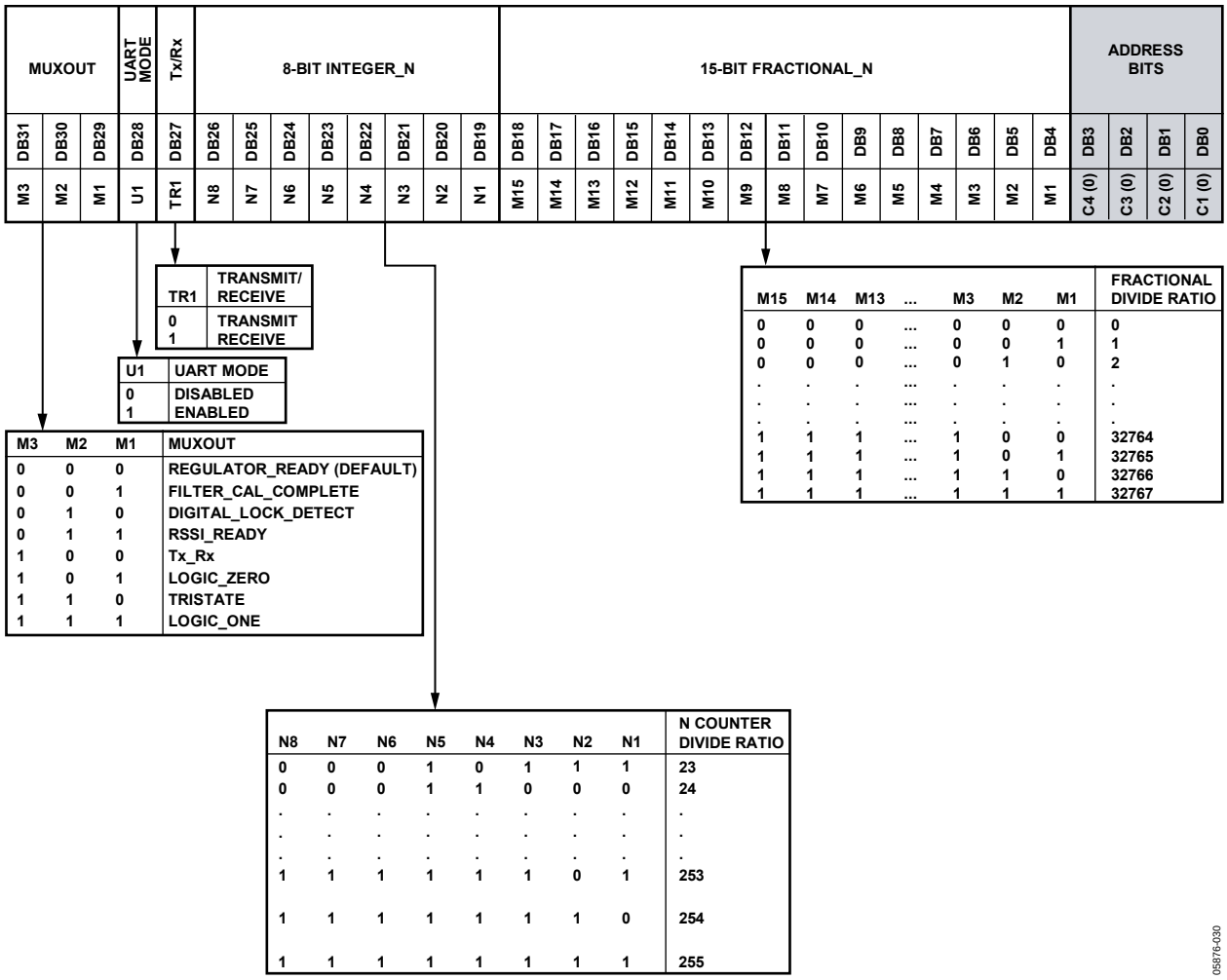


Figure 62. Register 0—N Register Map

The RF output frequency is calculated by the following:

For the direct output

$$RF_{OUT} = PFD \times \left(Integer_N + \frac{Fractional_N}{2^{15}} \right)$$

For the RF_DIVIDE_BY_2 (DB18) selected

$$RF_{OUT} = PFD \times 0.5 \times \left(Integer_N + \frac{Fractional_N}{2^{15}} \right)$$

In UART/SPI mode, the TxRxCLK pin is used to input the Tx data. The Rx Data is available on the TxRxDATA pin.

In the MUXOUT map in Figure 62, the FILTER_CAL_COMPLETE indicates when a coarse or coarse plus fine IF filter calibration has finished. The DIGITAL_LOCK_DETECT indicates when the PLL has locked. The RSSI_READY indicates that the RSSI signal has settled and an RSSI readback can be performed. Tx_Rx gives the status of DB27 in this register, which can be used to control an external Tx/Rx switch.

REGISTER 1—VCO/OSCILLATOR REGISTER

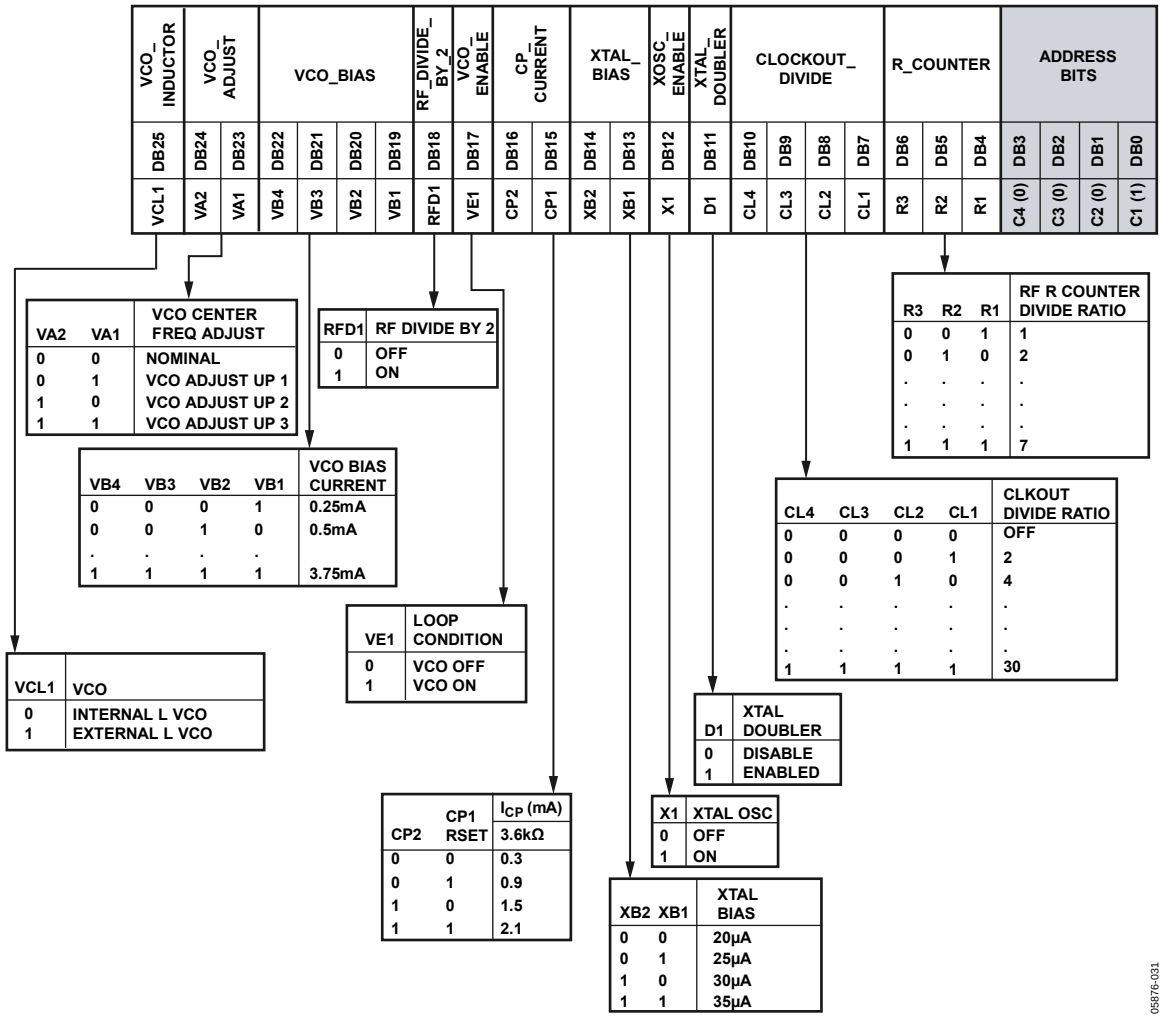


Figure 63. Register 1—VCO/Oscillator Register Map

The R_COUNTER and XTAL_DOUBLER relationship is expressed as follows:

If XTAL_DOUBLER = 0,

$$PFD = \frac{XTAL}{R_COUNTER}$$

If XTAL_DOUBLER =1,

$$PFD = \frac{XTAL \times 2}{R_COUNTER}$$

The CLOCKOUT_DIVIDE is a divided-down and inverted version of the XTAL and is available on Pin 36 (CLKOUT).

Set XOSC_ENABLE high when using an external crystal. If using an external oscillator (such as TCXO) with CMOS-level outputs into Pin OSC2, set XOSC_ENABLE low. If using an external oscillator with a 0.8 V p-p clipped sine wave output into Pin OSC1, set XOSC_ENABLE high.

The VCO_BIAS bits should be set according to Table 9.

The VCO_ADJUST bits adjust the center of the VCO operating band. Each bit typically adjusts the VCO band up by 1% of the RF operating frequency (0.5% if RF_DIVIDE_BY_2 is enabled).

Setting VCO_INDUCTOR to external allows the use of the external inductor VCO, which gives RF operating frequencies of 80 Hz to 650 MHz. If the internal inductor VCO is being used for operation, set this bit low.

REGISTER 2—TRANSMIT MODULATION REGISTER

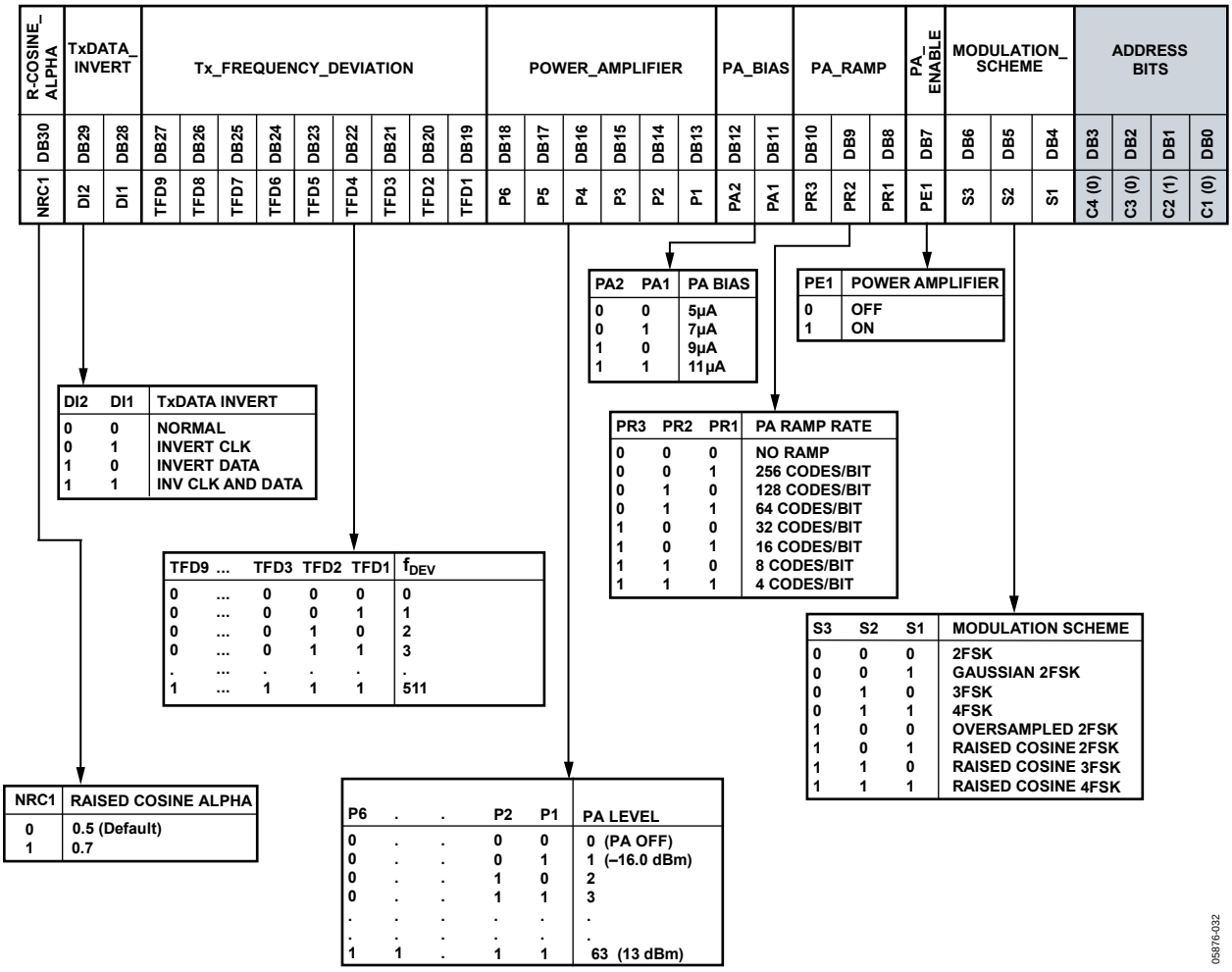


Figure 64. Register 2—Transmit Modulation Register Map

The 2FSK/3FSK/4FSK frequency deviation is expressed by the following:

Direct output

$$\textit{Frequency Deviation}\ [\text{Hz}] = \frac{\textit{Tx_FREQUENCY_DEVIATION} \times \textit{PFD}}{2^{16}}$$

With RF_DIVIDE_BY_2 (R1_DB18) enabled

$$\textit{Frequency Deviation}\ [\text{Hz}] = 0.5 \times \frac{\textit{Tx_FREQUENCY_DEVIATION} \times \textit{PFD}}{2^{16}}$$

where *Tx_FREQUENCY_DEVIATION* is set by DB[19:27] and *PFD* is the PFD frequency.

In the case of 4FSK, there are tones at ±3 × the frequency deviation and at ±1 × the deviation. The power amplifier (PA) ramps at the programmed rate (R2_DB[8:10]) until it reaches its programmed level DB[13:18]. If the PA is enabled/disabled by the PA_ENABLE bit (DB7), it ramps up and down. If it is enabled/disabled by the Tx/Rx bit (R0_DB27), it ramps up and turns hard off.

R-COSINE_ALPHA sets the roll-off factor (alpha) of the raised cosine data filter to either 0.5 or 0.7. The alpha is set to 0.5 by default, but the raised cosine filter bandwidth can be increased to provide less aggressive data filtering by using an alpha of 0.7.

REGISTER 3—TRANSMIT/RECEIVE CLOCK REGISTER

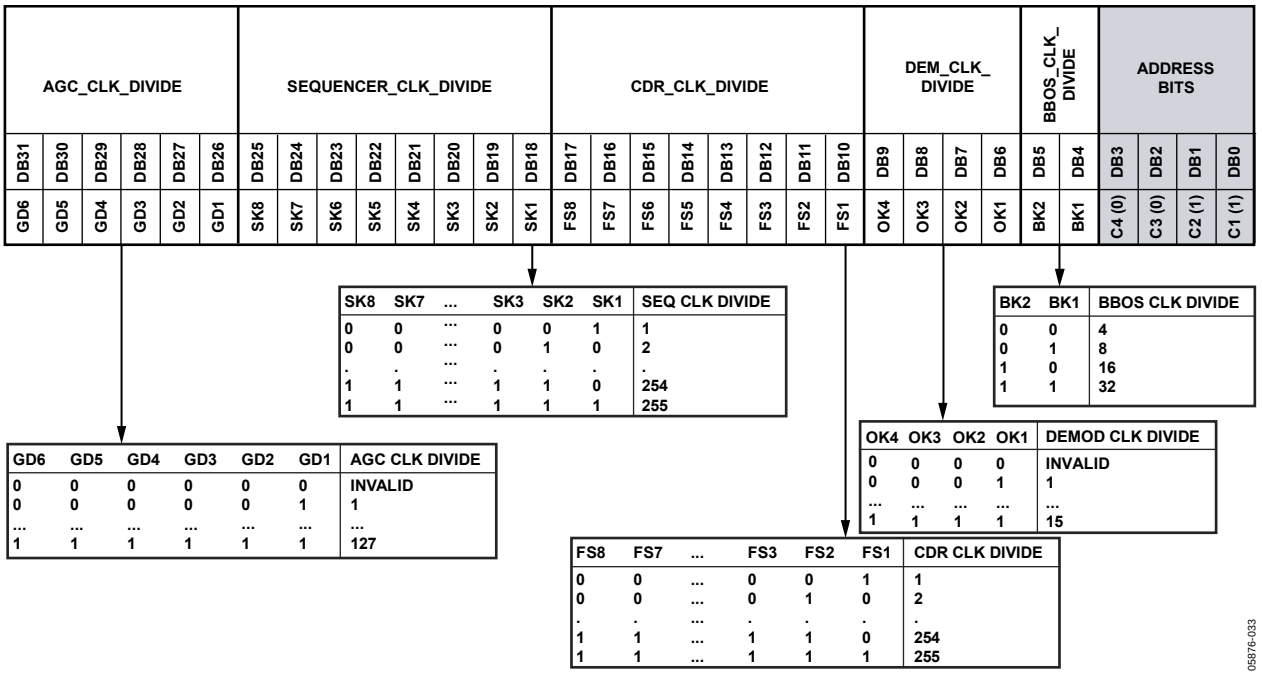


Figure 65. Register 3—Transmit/Receive Clock Register Map

Baseband offset clock frequency (BBOS CLK) must be greater than 1 MHz and less than 2 MHz, where

$$BBOS\ CLK = \frac{XTAL}{BBOS_CLK_DIVIDE}$$

Set the demodulator clock (DEMOD CLK) such that 2 MHz ≤ DEMOD CLK ≤ 15 MHz, where

$$DEMOD\ CLK = \frac{XTAL}{DEMOD_CLK_DIVIDE}$$

For 2FSK/3FSK, the data/clock recovery frequency (CDR CLK) needs to be within 2% of (32 × data rate). For 4FSK, the CDR CLK needs to be within 2% of (32 × symbol rate).

$$CDR\ CLK = \frac{DEMOD\ CLK}{CDR_CLK_DIVIDE}$$

The sequencer clock (SEQ CLK) supplies the clock to the digital receive block. It should be as close to 100 kHz as possible.

$$SEQ\ CLK = \frac{XTAL}{SEQ_CLK_DIVIDE}$$

The time allowed for each AGC step to settle is determined by the AGC update rate. It should be set close to 10 kHz.

$$AGC\ Update\ Rate\ [\text{Hz}] = \frac{SEQ\ CLK}{AGC_CLK_DIVIDE}$$

REGISTER 4—DEMODULATOR SETUP REGISTER

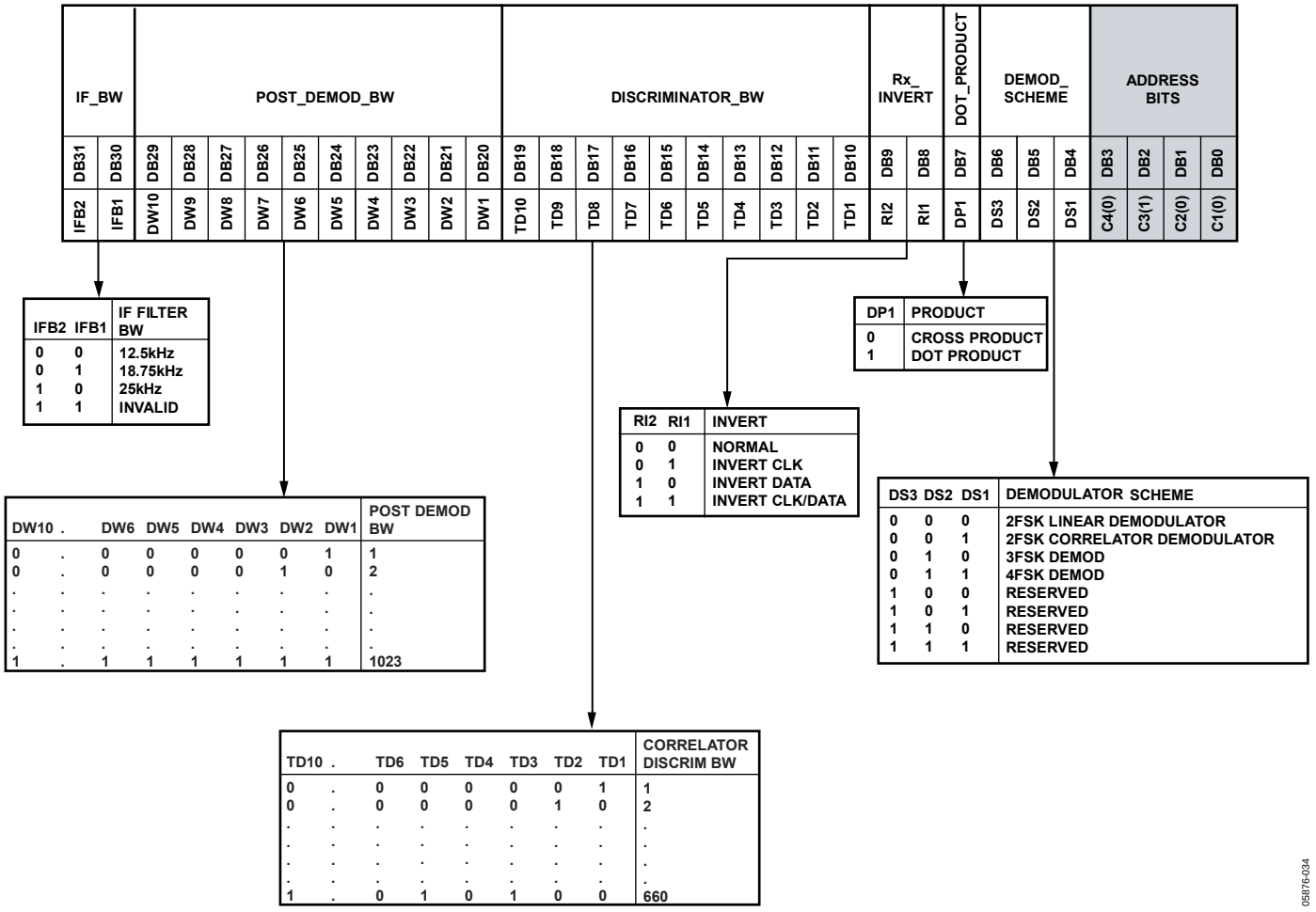


Figure 66. Register 4—Demodulator Setup Register Map

To solve for DISCRIMINATOR_BW, use the following equation:

$$DISCRIMINATOR_BW = \frac{DEMOD\ CLK \times K}{400 \times 10^3}$$

where the maximum value = 660.

For 2FSK,

$$K = Round\left(\frac{100 \times 10^3}{f_{DEV}}\right)$$

For 3FSK,

$$K = Round\left(\frac{100 \times 10^3}{2 \times f_{DEV}}\right)$$

For 4FSK,

$$K = Round_{4FSK}\left(\frac{100 \times 10^3}{4 \times f_{DEV}}\right)$$

where:

Round is rounded to the nearest integer.

$Round_{4FSK}$ is rounded to the nearest of the following integers: 32, 31, 28, 27, 24, 23, 20, 19, 16, 15, 12, 11, 8, 7, 4, 3.

f_{DEV} is the transmit frequency deviation in Hz. For 4FSK, f_{DEV} is the frequency deviation used for the ±1 symbols (that is, the inner frequency deviations).

Rx_INVERT (DB[8:9]) and DOT_PRODUCT (DB7) need to be set as outlined in Table 17 and Table 18.

$$POST_DEMOD_BW = \frac{2^{11} \times \pi \times f_{CUTOFF}}{DEMOD\ CLK}$$

where the cutoff frequency (f_{CUTOFF}) of the post demodulator filter should typically be 0.75 × the data rate in 2FSK. In 3FSK, it should be set equal to the data rate, while in 4FSK, it should be set equal to 1.6 × symbol rate.

REGISTER 5—IF FILTER SETUP REGISTER

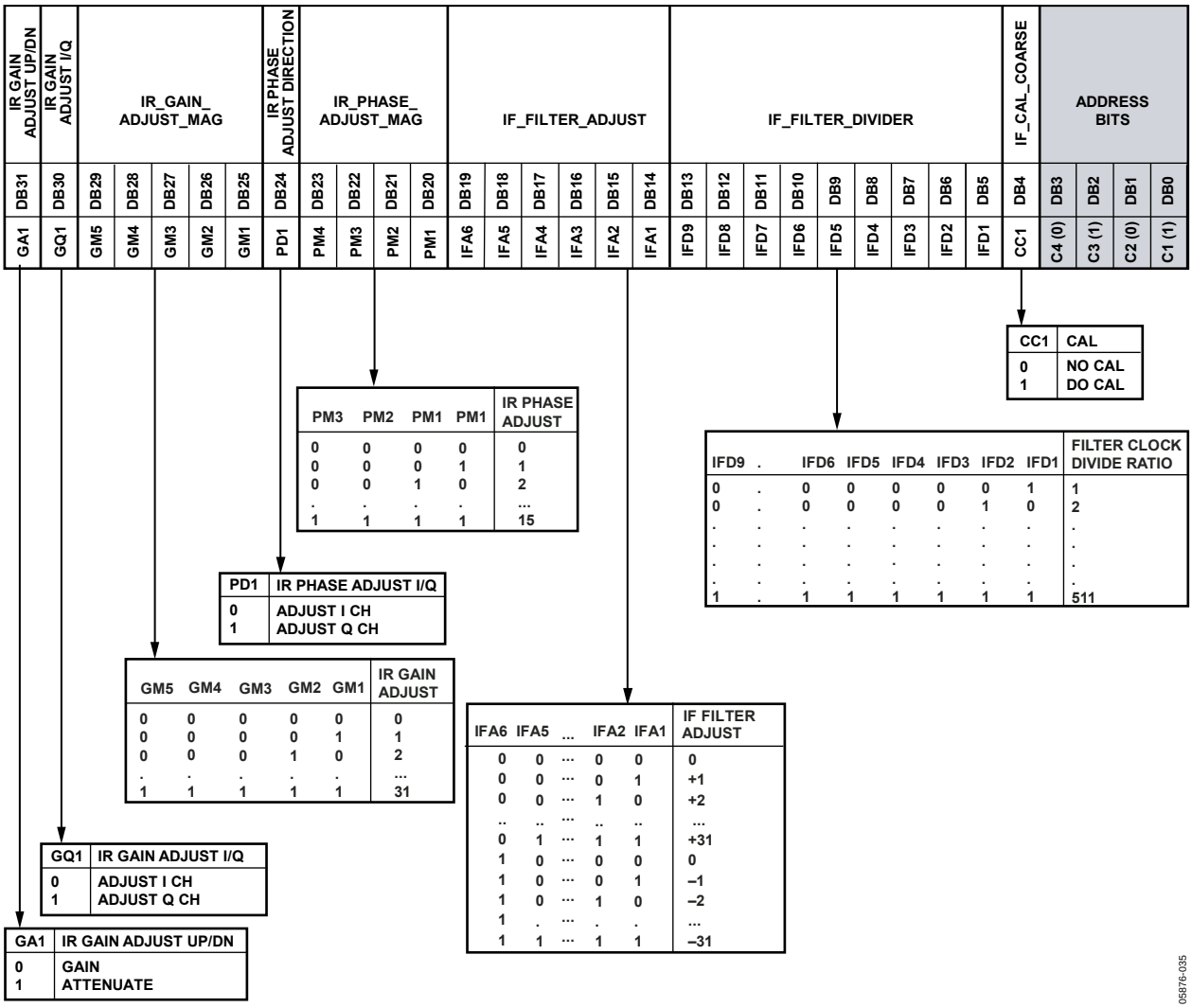


Figure 67. Register 5—IF Filter Setup Register Map

A coarse IF filter calibration is performed when the IF_CAL_COARSE bit (DB4) is set. If the IF_FINE_CAL bit (R6_DB4) has been previously set, a fine IF filter calibration is automatically performed after the coarse calibration.

Set IF_FILTER_DIVIDER such that

$$\frac{XTAL}{IF_FILTER_DIVIDER} = 50\,\text{kHz}$$

IF_FILTER_ADJUST allows the IF fine filter calibration result to be programmed directly on subsequent receiver power-ups, thereby saving on the need to redo a fine filter calibration in some instances. Refer to the Filter Bandwidth Calibration Readback section for information about using the IF_FILTER_ADJUST bits.

DB[20:31] are used for image rejection calibration. Refer to the Image Rejection Calibration section for details on how to program these parameters.

REGISTER 6—IF FINE CAL SETUP REGISTER

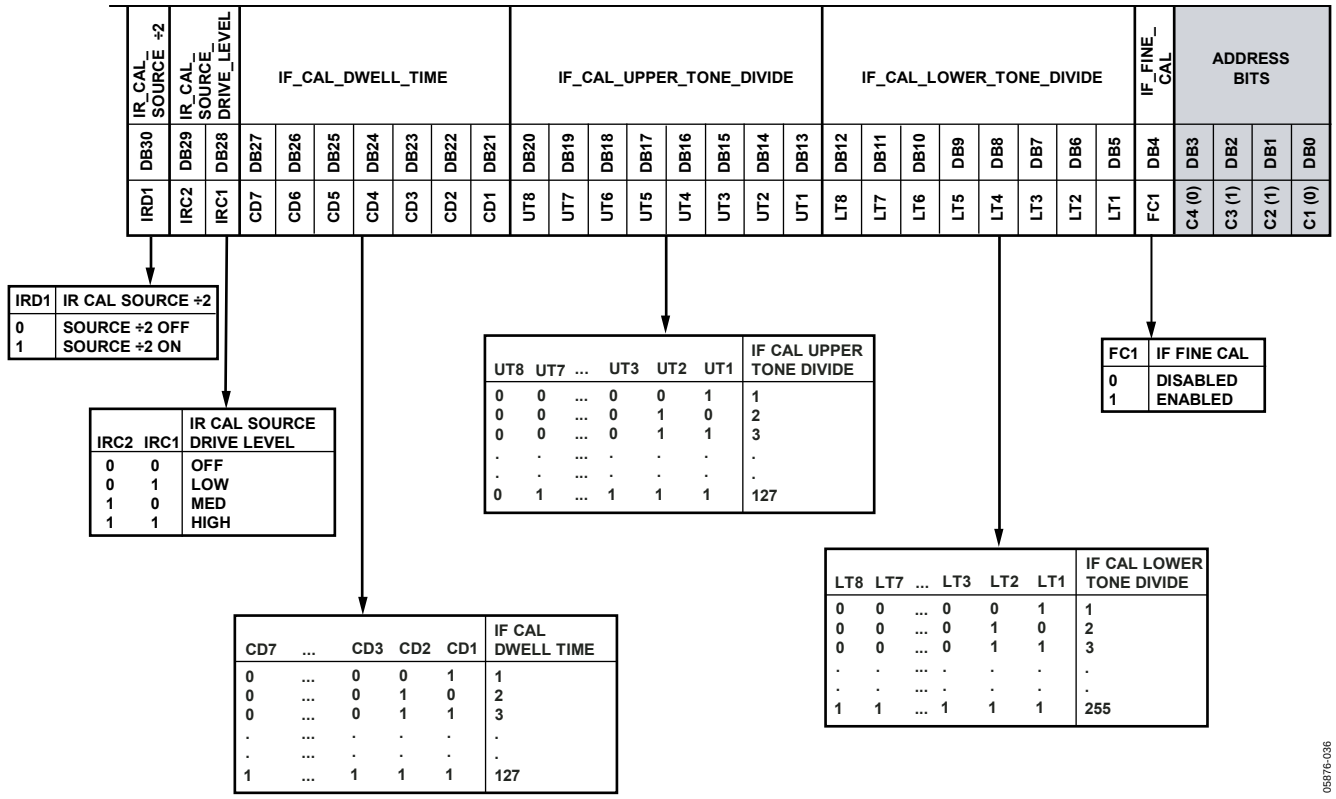


Figure 68. Register 6—IF Fine Cal Setup Register Map

A fine IF filter calibration is set by enabling the IF_FINE_CAL Bit (R6_DB4). A fine calibration is then carried out only when Register 5 is written to and R5_DB4 is set.

Set the IF upper and lower tones used during fine filter calibration as follows:

$$\frac{XTAL}{IF_CAL_LOWER_TONE_DIVIDE \times 2} = 65.8\,\text{kHz}$$

$$\frac{XTAL}{IF_CAL_UPPER_TONE_DIVIDE \times 2} = 131.5\,\text{kHz}$$

The IF tone calibration time is the amount of time that is spent at an IF calibration tone. It is dependent on the sequencer clock.

For best practice, is recommended to have the IF tone calibration time be at least 500 µs.

$$IF\ Tone\ Calibration\ Time = \frac{IF_CAL_DWELL_TIME}{SEQ\ CLK}$$

The total time for a fine IF filter calibration is

IF Tone Calibration Time × 10.

DB[28:30] control the internal source for the image rejection (IR) calibration. The IR_CAL_SOURCE_DRIVE_LEVEL bits (DB[28:29]) set the drive strength of the source, whereas the IR_CAL_SOURCE_÷2 bit (DB30) allows the frequency of the internal signal source to be divided by 2.

REGISTER 7—READBACK SETUP REGISTER

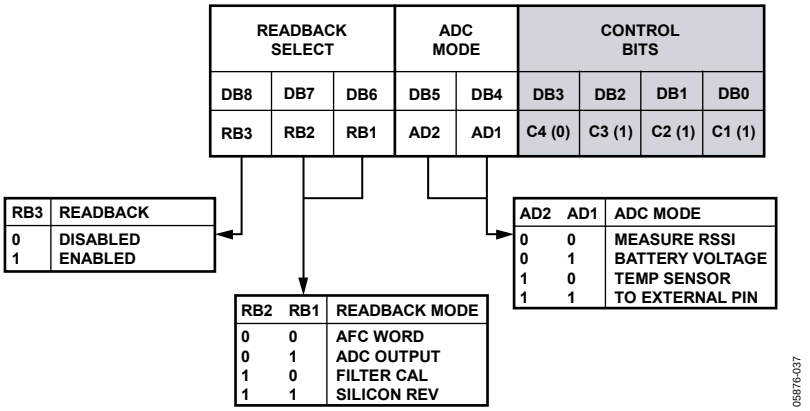


Figure 69. Register 7—Readback Setup Register Map

Readback of the measured RSSI value is valid only in Rx mode. Readback of the battery voltage, temperature sensor, or voltage at the external pin is not valid in Rx mode.

To read back the battery voltage, the temperature sensor, or the voltage at the external pin in Tx mode, users should first power up the ADC using R8_DB8 because it is turned off by default in Tx mode to save power.

For AFC readback, use the following equations (see the Readback Format section):

$$FREQ\ RB\ [\text{Hz}] = (AFC_READBACK \times DEMOD\ CLK)/2^{18}$$

$$V_{BATTERY} = BATTERY_VOLTAGE_READBACK/21.1$$

$$V_{ADCIN} = ADCIN_VOLTAGE_READBACK/42.1$$

$$Temperature\ [°\text{C}] = -40 + (68.4 - TEMP_READBACK) \times 9.32$$

REGISTER 8—POWER-DOWN TEST REGISTER

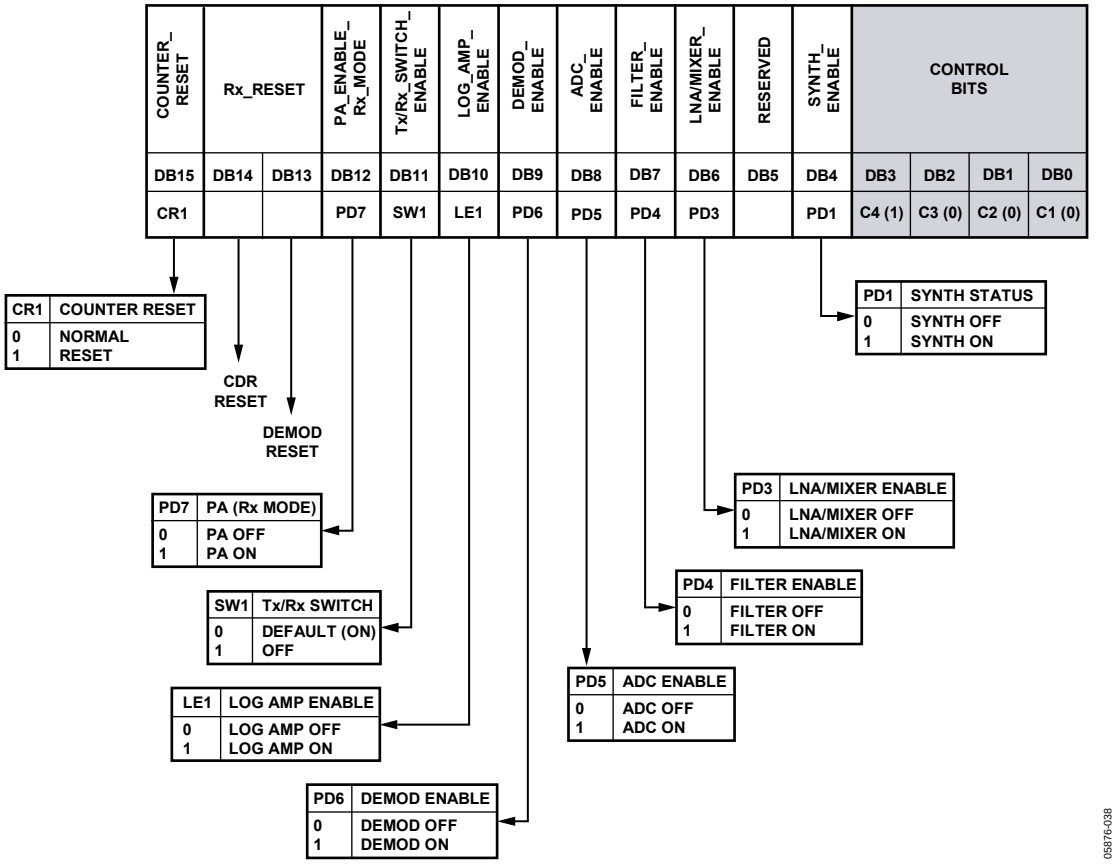


Figure 70. Register 8—Power-Down Test Register Map

It is not necessary to write to this register under normal operating conditions.

For a combined LNA/PA matching network, DB11 should always be set to 0, which enables the internal Tx/Rx switch. This is the power-up default condition.

REGISTER 9—AGC REGISTER

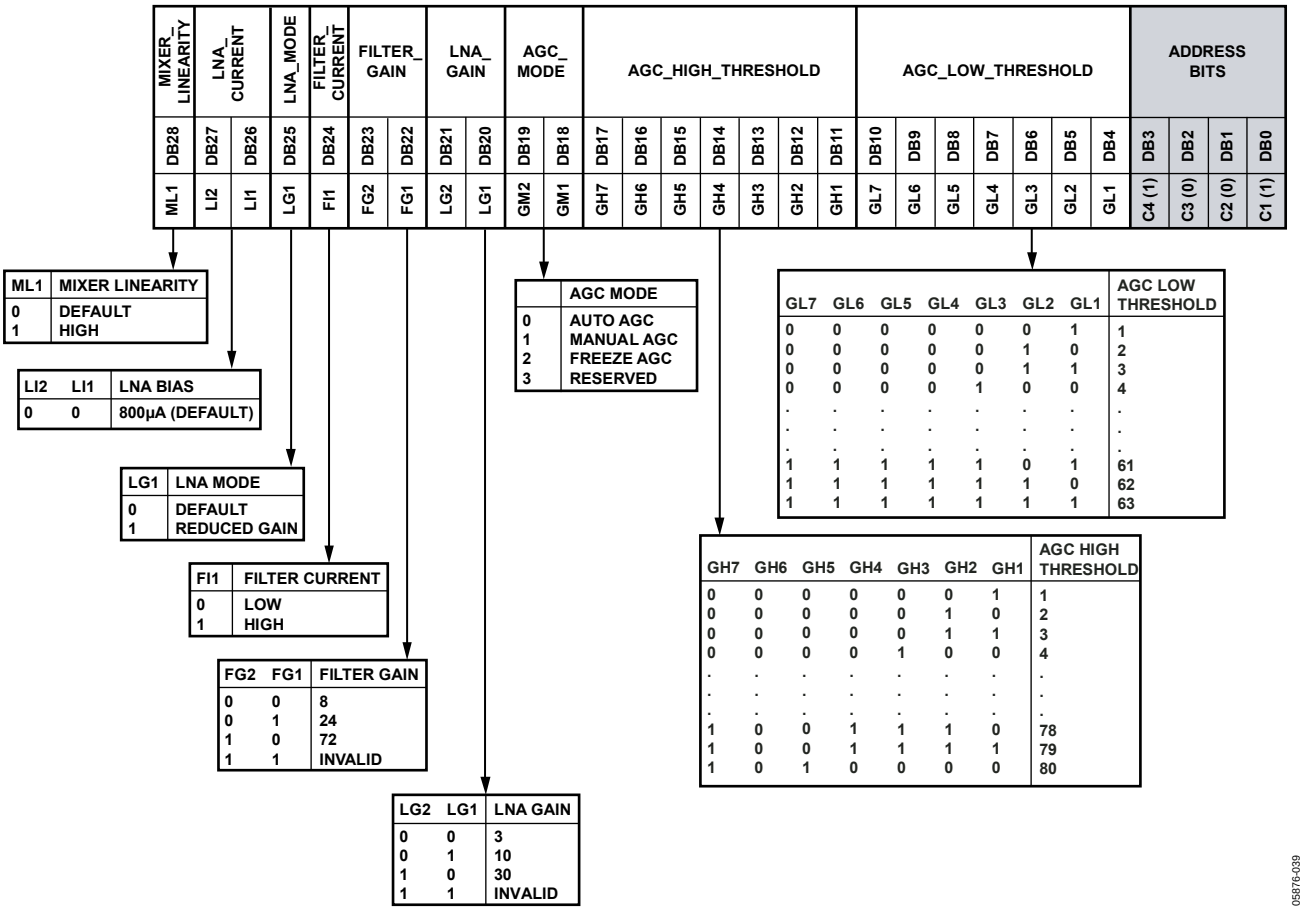


Figure 71. Register 9—AGC Register Map

In receive mode, AGC is set to automatic AGC by default on power-up. The default thresholds are AGC_LOW_THRESHOLD = 30 and AGC_HIGH_THRESHOLD = 70. See the RSSI/AGC section for details. It is only necessary to program this register if AGC settings, other than the defaults, are required.

AGC high and low settings must be more than 30 apart to ensure correct operation.

An LNA gain of 30 is available only if LNA_MODE (DB25) is set to 0.

REGISTER 10—AFC REGISTER

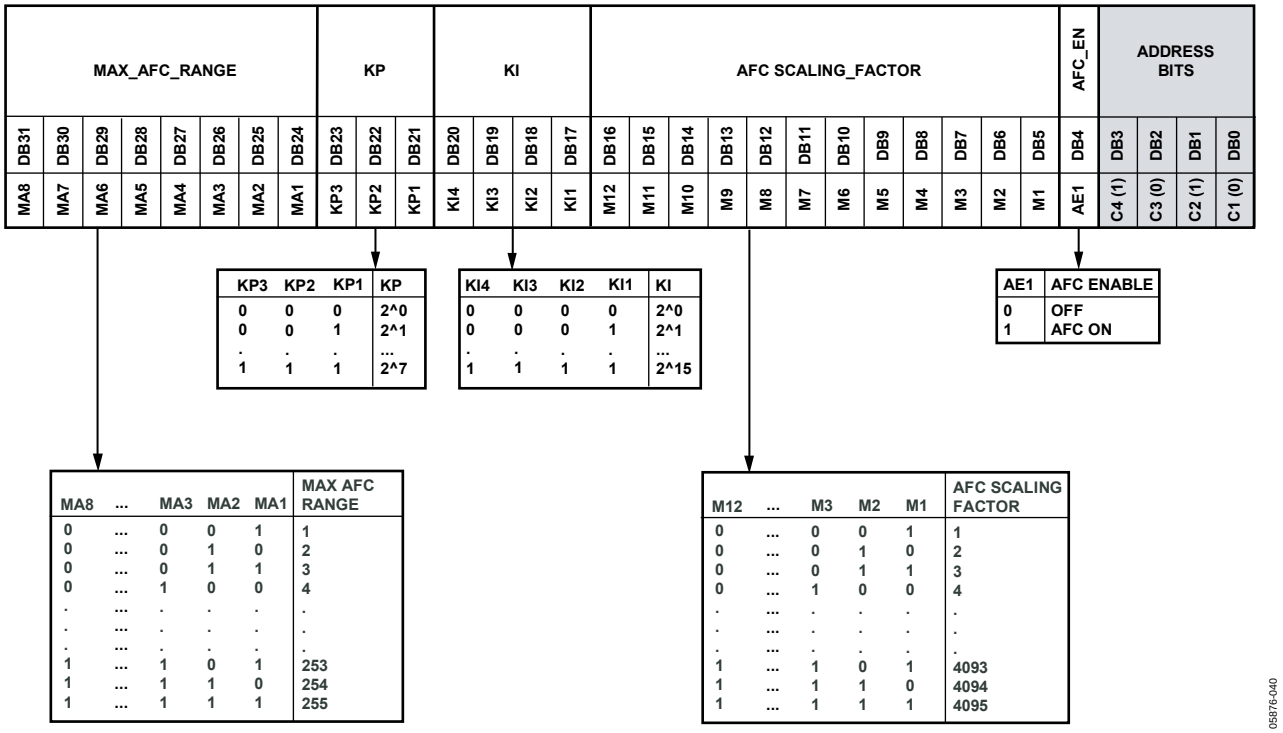


Figure 72. Register 10—AFC Register Map

The AFC_SCALING_FACTOR can be expressed as

$$AFC_SCALING_FACTOR = Round\left(\frac{2^{24} \times 500}{XTAL}\right)$$

The settings for KI and KP affect the AFC settling time and AFC accuracy. The allowable range of each parameter is

$KI > 6$ and $KP < 7$

The recommended settings to give optimal AFC performance are KI = 11 and KP = 4.

To tradeoff between AFC settling time and AFC accuracy, the KI and KP parameters can be adjusted from the recommended settings (staying within the allowable range) such that

$$AFC\ Correction\ Range = MAX_AFC_RANGE \times 500\ \text{Hz}$$

When the RF_DIVIDE_BY_2 (R1_DB18) is enabled, the programmed AFC correction range is halved. The user accounts for this halving by doubling the programmed MAX_AFC_RANGE value.

Signals that are within the AFC pull-in range but outside the IF filter bandwidth are attenuated by the IF filter. As a result, the signal can be below the sensitivity point of the receiver and, therefore, not detectable by the AFC.

REGISTER 11—SYNC WORD DETECT REGISTER

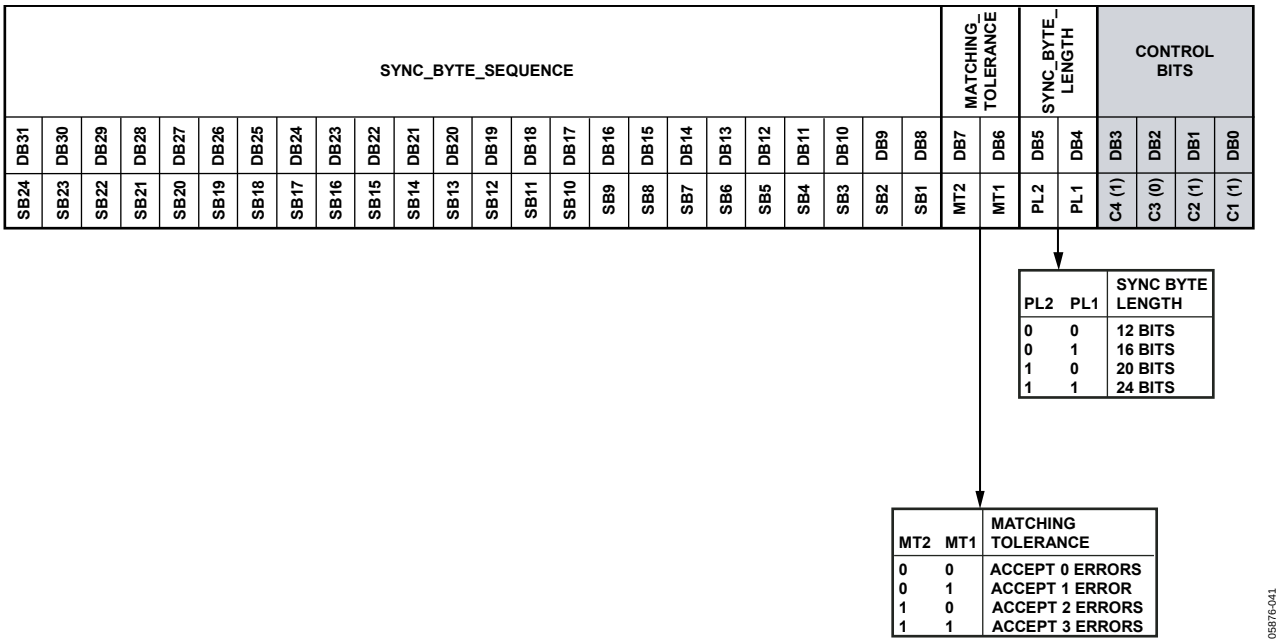


Figure 73. Register 11—Sync Word Detect Register Map

REGISTER 12—SWD/THRESHOLD SETUP REGISTER

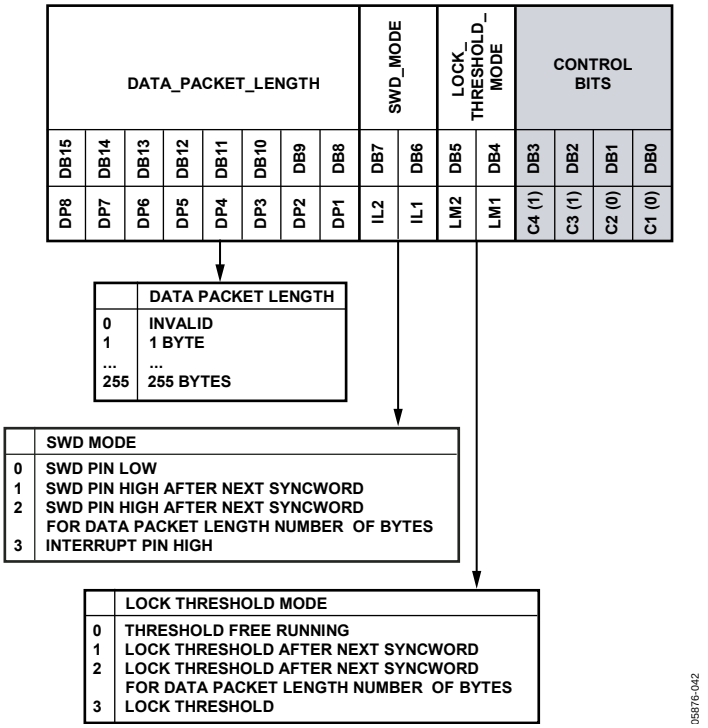


Figure 74. Register 12—SWD/Threshold Setup Register Map

Lock threshold locks the threshold of the envelope detector. This has the effect of locking the slicer in linear demodulation and locking the AFC and AGC loops when using linear or correlator demodulation.

REGISTER 13—3FSK/4FSK DEMOD REGISTER

Refer to the Receiver Setup section for information about programming these settings.

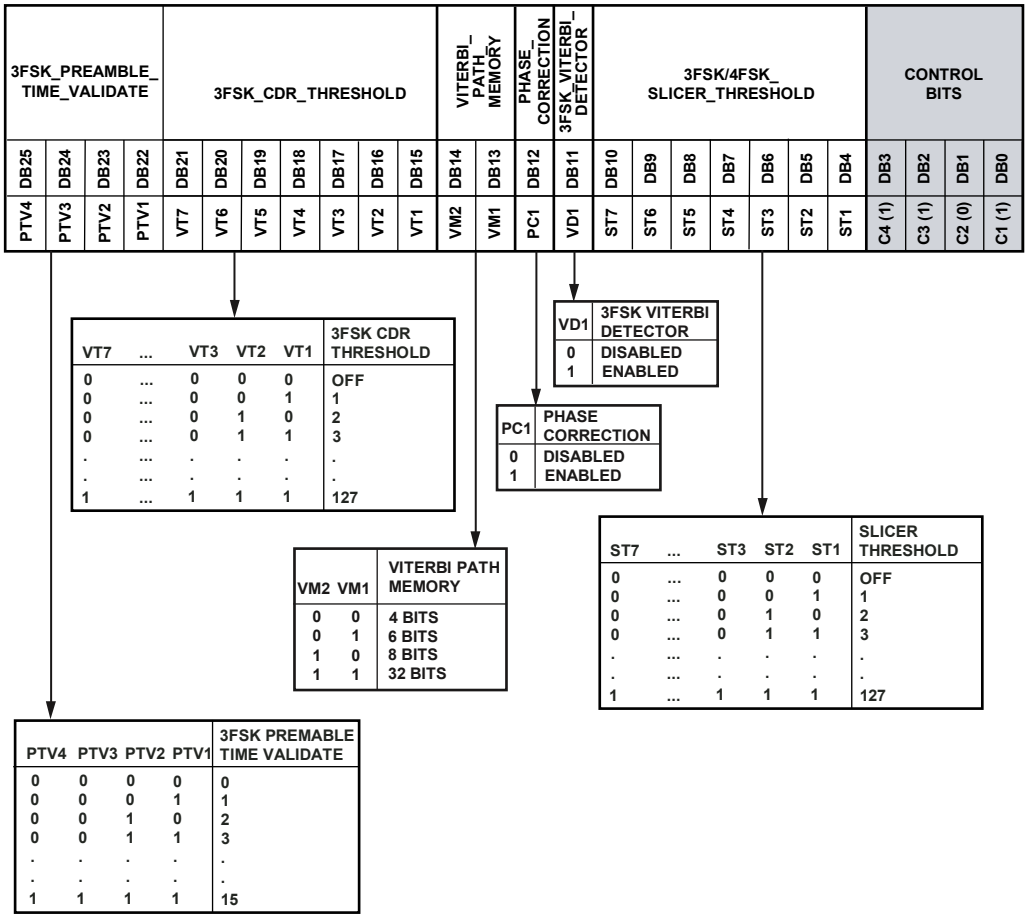


Figure 75. Register 13—3FSK/4FSK Demod Register Map

REGISTER 14—TEST DAC REGISTER

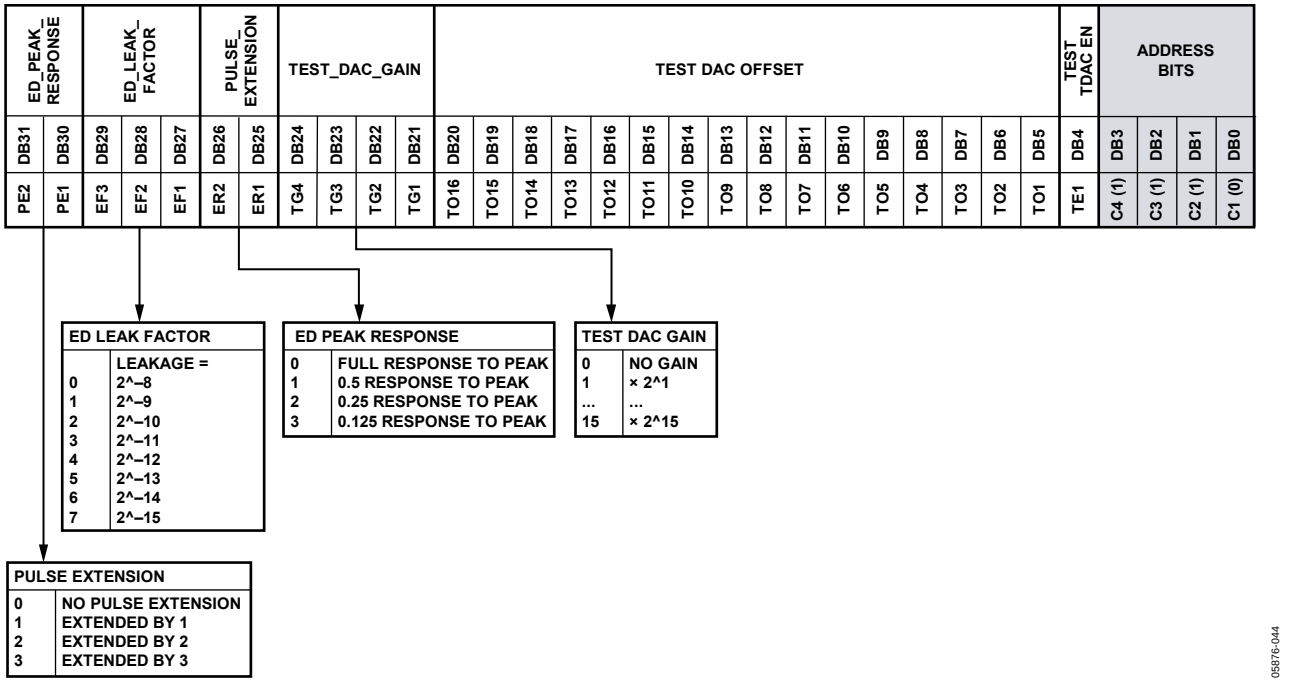


Figure 76. Register 14—Test DAC Register Map

The demodulator tuning parameters, PULSE_EXTENSION, ED_LEAK_FACTOR, and ED_PEAK_RESPONSE, can only be enabled by setting R15_DB[4:7] to 0x9.

Using the Test DAC to Implement Analog FM DEMOD and Measuring SNR

The test DAC allows the post demodulator filter out for both linear and correlator demodulators to be viewed externally. The test DAC also takes the 16-bit filter output and converts it to a high frequency, single-bit output using a second-order, error feedback Σ-Δ converter. The output can be viewed on the SWD pin. This signal, when filtered appropriately, can then be used to do the following:

- Monitor the signals at the FSK post demodulator filter output. This allows the demodulator output SNR to be measured. Eye diagrams of the received bit stream can also be constructed to measure the received signal quality.
- Provide analog FM demodulation.

While the correlators and filters are clocked by DEMOD CLK, CDR CLK clocks the test DAC. Note that although the test DAC functions in regular user mode, the best performance is achieved when the CDR_CLK is increased to or above the frequency of DEMOD CLK. The CDR block does not function when this condition exists.

Programming Register 14 enables the test DAC. Both the linear and correlator/demodulator outputs can be multiplexed into the DAC.

Register 14 allows a fixed offset term to be removed from the signal (to remove the IF component in the ddt case). It also has a signal gain term to allow the usage of the maximum dynamic range of the DAC.

REGISTER 15—TEST MODE REGISTER

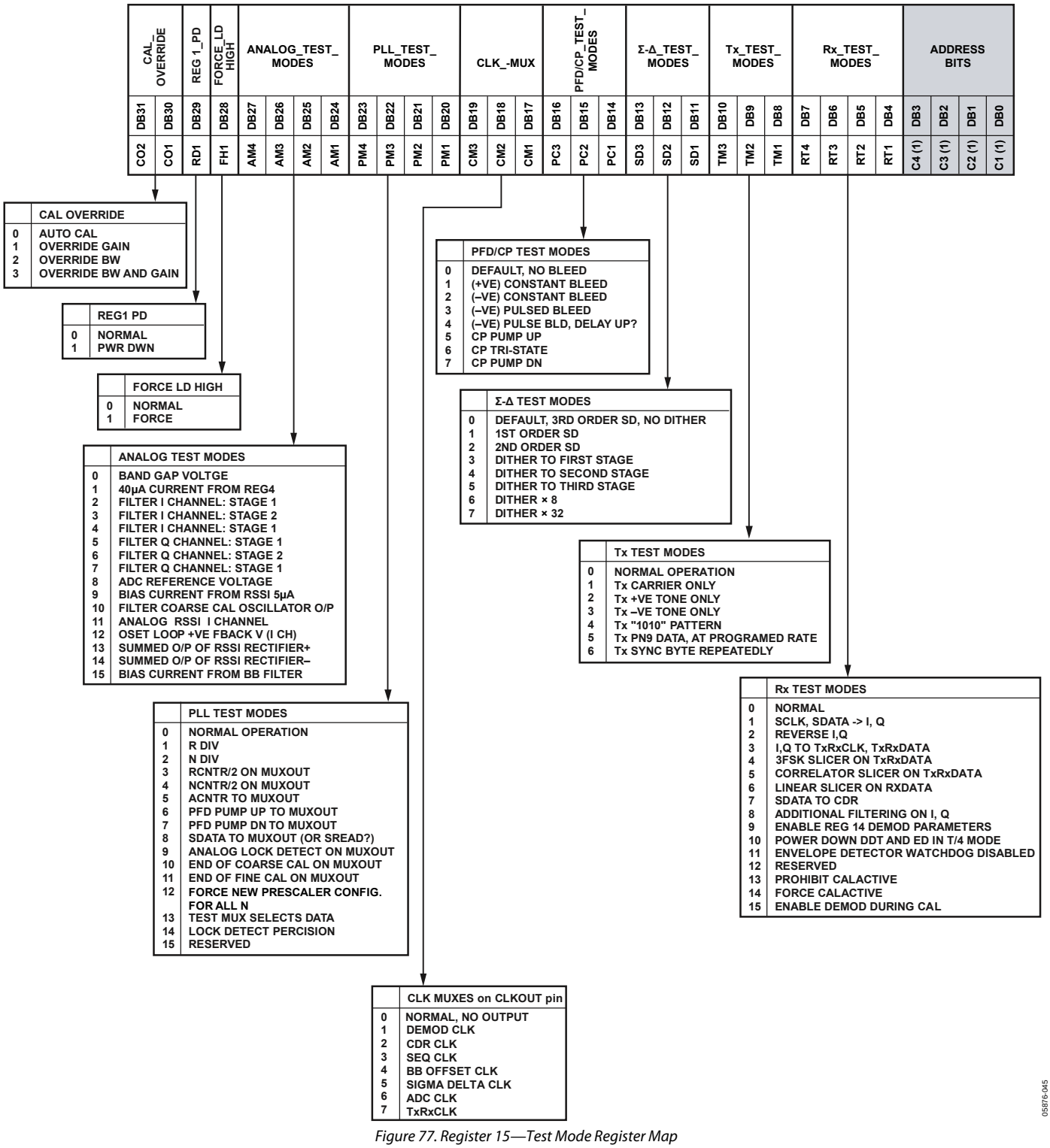


Figure 77. Register 15—Test Mode Register Map

OUTLINE DIMENSIONS

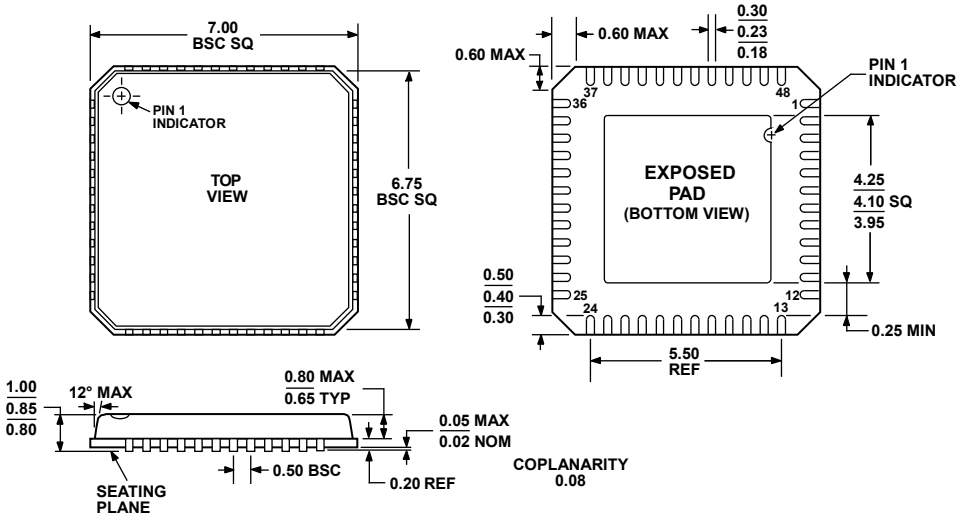


Figure 78. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7021BCPZ[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-3
ADF7021BCPZ-RL[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-3
ADF7021BCPZ-RL7[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-3
EVAL-ADF70XXMBZ[1]		Control Mother Board	
EVAL-ADF70XXMBZ2[1]		Evaluation Platform	
EVAL-ADF7021DBJZ[1]		426 MHz to 429 MHz Daughter Board	
EVAL-ADF7021DBZ2[1]		860 MHz to 870 MHz Daughter Board	
EVAL-ADF7021DBZ3[1]		431 MHz to 470 MHz Daughter Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А