Cyclone V Device Overview

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The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Key Advantages of Cyclone V Devices

Table 1: Key Advantages of the Cyclone V Device Family

Advantage	Supporting Feature
Lower power consumption	• Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks • Up to 40% lower power consumption than the previous generation device
Improved logic integration and differentiation capabilities	• 8-input adaptive logic module (ALM) • Up to 13.59 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks
Increased bandwidth capacity	• 3.125 gigabits per second (Gbps) and 5 Gbps transceivers • Hard memory controllers
Hard processor system (HPS) with integrated ARM® Cortex™-A9 MPCore processor	• Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) FPGA • Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Lowest system cost	• Requires only two core voltages to operate • Available in low-cost wirebond packaging • Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration

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ISO 9001:2008 Registered

Summary of Cyclone V Features

Table 2: Summary of Features for Cyclone V Devices

Feature	Description	
Technology	• TSMC's 28-nm low-power (28LP) process technology • 1.1 V core voltage	
Packaging	• Wirebond low-halogen packages • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS-compliant options	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) • Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block • 64-bit accumulator and cascade • Embedded internal coefficient memory • Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express® (PCIe®) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	• Up to 550 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode	
FPGA General-purpose I/Os (GPIOs)	• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter • 400 MHz/800 Mbps external memory interface • On-chip termination (OCT) • 3.3 V support with up to 16 mA drive strength	
Low-power high-speed serial interface	• 614 Mbps to 5.0 Gbps integrated transceiver speed • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels	

Feature	Description
HPS (Cyclone V SE, SX, and ST devices only)	• Single or dual-core ARM Cortex-A9 MPCore processor-up to 800 MHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller • ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced advanced encryption standard (AES) design security features • CvP • Partial and dynamic reconfiguration of the FPGA • Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options

Cyclone V Device Variants and Packages

Table 3: Device Variants for the Cyclone V Device Family

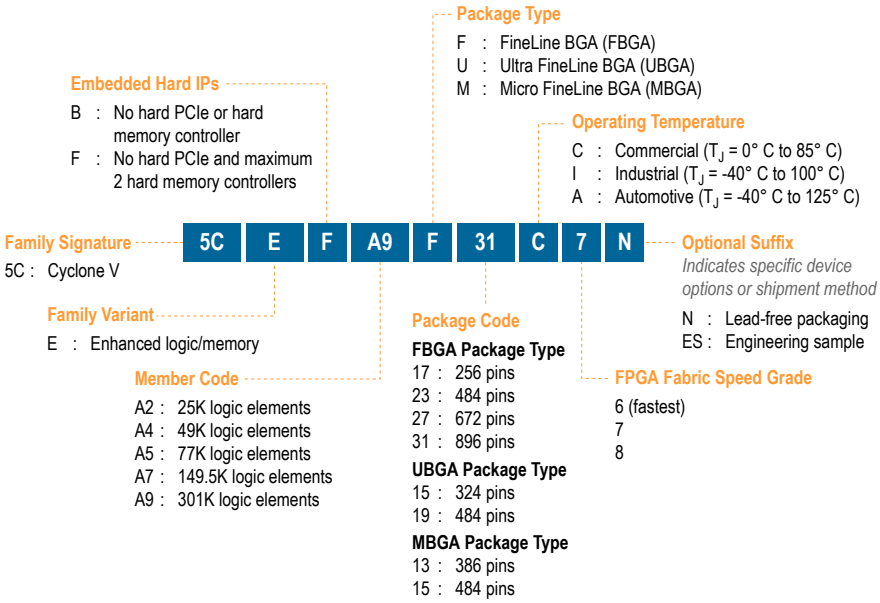
Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 5 Gbps transceiver applications
Cyclone V SE	SoC FPGA with integrated ARM-based HPS
Cyclone V SX	SoC FPGA with integrated ARM-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC FPGA with integrated ARM-based HPS and 5 Gbps transceivers

Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

Available Options

Figure 1: Sample Ordering Code and Available Options for Cyclone V E Devices—Preliminary



Maximum Resources

Table 4: Maximum Resource Counts for Cyclone V E Devices—Preliminary

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	149.5	301
ALM		9,434	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO[1]		224	224	240	480	480

[1] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.

Resource	Member Code				
	A2	A4	A5	A7	A9
LVDS[2]	56	56	60	120	120
Hard Memory Controller	1	1	2	2	2

Package Plan

Table 5: Package Plan for Cyclone V E Devices—Preliminary

Member Code	M386 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	208	—	176	128	224	224	—	—
A4	208	—	176	128	224	224	—	—
A5	208	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

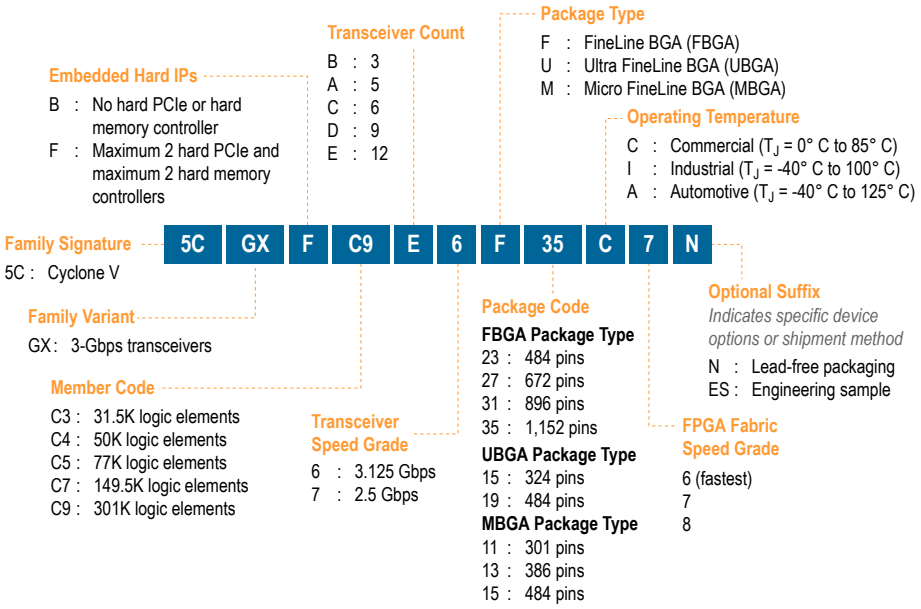
This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

Available Options

The following figure shows sample ordering code and lists the options available for Cyclone V GX devices.

[2] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.

Figure 2: Sample Ordering Code and Available Options for Cyclone V GX Devices—Preliminary



Maximum Resources

Table 6: Maximum Resource Counts for Cyclone V GX Devices—Preliminary

Resource		Member Code				
		C3	C4	C5	C7	C9
Logic Elements (LE) (K)		31.5	50	77	149.5	301
ALM		11,900	18,868	29,080	56,480	113,560
Register		47,600	75,472	116,320	225,920	454,240
Memory (Kb)	M10K	1,190	2,500	4,460	6,860	12,200
	MLAB	159	295	424	836	1,717
Variable-precision DSP Block		51	70	150	156	342
18 x 18 Multiplier		102	140	300	312	684
PLL[3]		4	6	6	7	8
3 Gbps Transceiver		3	6	6	9	12
GPIO[4]		208	336	336	480	560
LVDS[5]		52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

[3] The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs.
[4] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
[5] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.

Package Plan

Table 7: Package Plan for Cyclone V GX Devices—Preliminary

Member Code	M301 (11 mm)		M386 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)		F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3	208	3	—	—	—	—	—	—
C4	127	4	175	6	—	—	—	—	224	6	240	6	336	6	—	—	—	—
C5	127	4	175	6	—	—	—	—	224	6	240	6	336	6	—	—	—	—
C7	—	—	—	—	240	3	—	—	240	6	240	6	336	9	480	9	—	—
C9	—	—	—	—	—	—	—	—	240	5	224	6	336	9	480	12	560	12

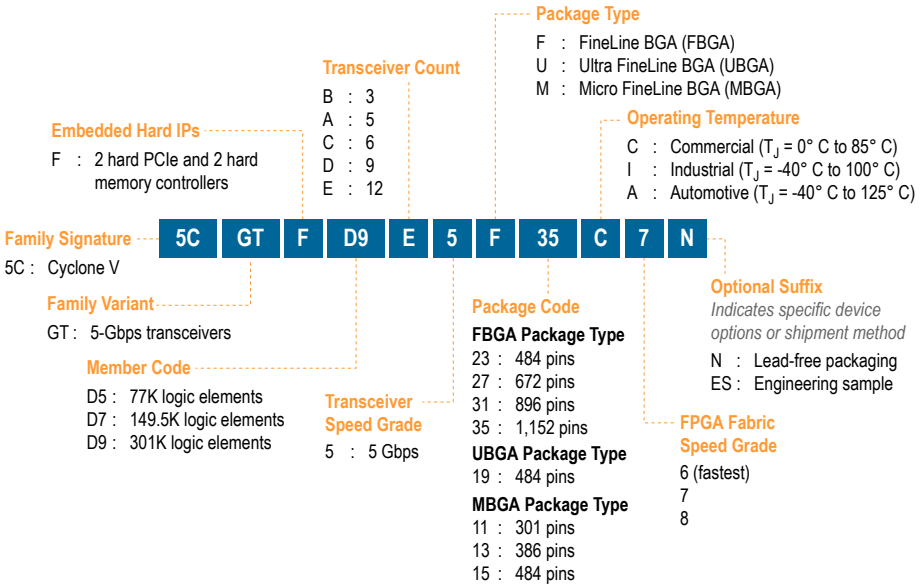
Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

Available Options

The following figure shows sample ordering code and lists the options available for Cyclone V GT devices.

Figure 3: Sample Ordering Code and Available Options for Cyclone V GT Devices—Preliminary



Maximum Resources

Table 8: Maximum Resource Counts for Cyclone V GT Devices—Preliminary

Resource	Member Code		
	D5	D7	D9
Logic Elements (LE) (K)	77	149.5	301

Resource		Member Code		
		D5	D7	D9
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL[6]		6	7	8
5 Gbps Transceiver		6	9	12
GPIO[7]		336	480	560
LVDS[8]		84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Package Plan

Table 9: Package Plan for Cyclone V GT Devices—Preliminary

Member Code	M301 (11 mm)		M386 (13 mm)		M484 (15 mm)		U484 (19 mm)		F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	127	4	175	6	—	—	224	6	240	6	336	6	—	—	—	—
D7	—	—	—	—	240	3	240	6	240	6	336	9[9]	480	9[9]	—	—
D9	—	—	—	—	—	—	240	5	224	6	336	9[9]	480	12[10]	560	12[10]

Cyclone V SE

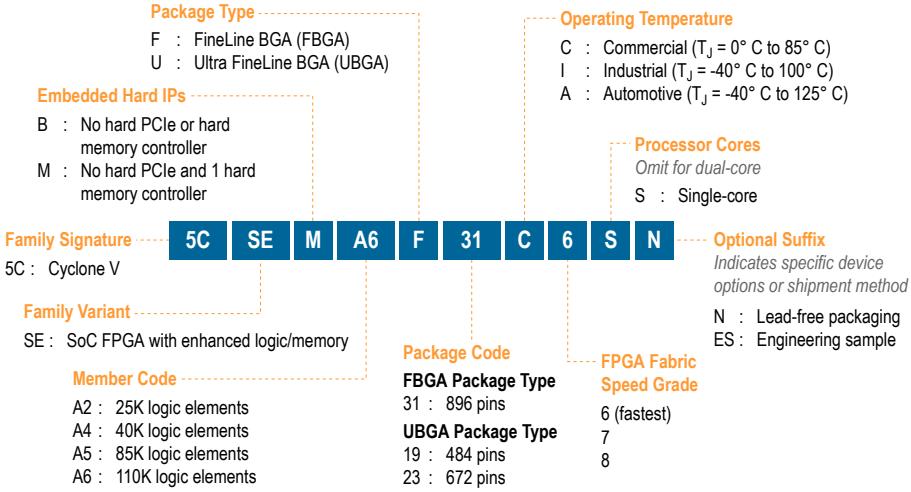
This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

[6] The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs.
[7] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
[8] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.
[9] If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Altera recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.
[10] If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Altera recommends that you use only up to 10 full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Available Options

The following figure shows sample ordering code and lists the options available for Cyclone V SE devices.

Figure 4: Sample Ordering Code and Available Options for Cyclone V SE Devices—Preliminary



Maximum Resources

Table 10: Maximum Resource Counts for Cyclone V SE Devices—Preliminary

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,434	15,094	32,075	41,509
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,240	3,970	5,140
	MLAB	138	220	480	621
Variable-precision DSP Block		36	58	87	112
18 x 18 Multiplier		72	116	174	224
FPGA PLL[11]		4	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO[12]		145	145	288	288
HPS I/O		188	188	188	188
LVDS[13]		31	31	72	72
FPGA Hard Memory Controller		1	1	1	1

[11] The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs.
[12] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
[13] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.

Resource	Member Code			
	A2	A4	A5	A6
HPS Hard Memory Controller	1	1	1	1
ARM Cortex-A9 MPCore Processor	Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Package Plan

Table 11: Package Plan for Cyclone V SE Devices—Preliminary

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	161	145	188	—	—
A4	66	161	145	188	—	—
A5	66	161	145	188	288	188
A6	66	161	145	188	288	188

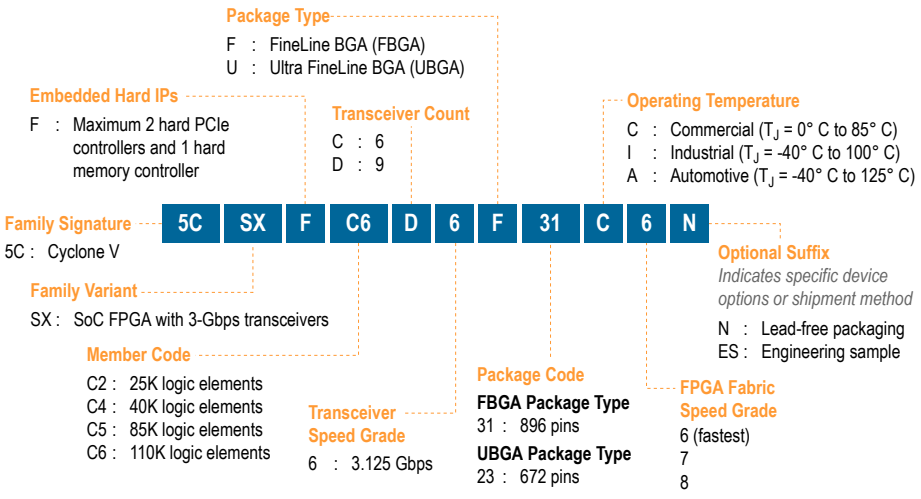
Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

Available Options

The following figure shows sample ordering code and lists the options available for Cyclone V SX devices.

Figure 5: Sample Ordering Code and Available Options for Cyclone V SX Devices—Preliminary



Maximum Resources

Table 12: Maximum Resource Counts for Cyclone V SX Devices—Preliminary

Resource		Member Code			
		C2	C4	C5	C6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,434	15,094	32,075	41,509
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,240	3,970	5,140
	MLAB	138	220	480	621
Variable-precision DSP Block		36	58	87	112
18 x 18 Multiplier		72	116	174	224
FPGA PLL[14]		4	5	6	6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO[15]		145	145	288	288
HPS I/O		188	188	188	188
LVDS[16]		31	31	72	72
PCIe Hard IP Block		2	2	2	2
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Package Plan

Table 13: Package Plan for Cyclone V SX Devices—Preliminary

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	188	6	—	—	—
C4	145	188	6	—	—	—
C5	145	188	9	288	188	9
C6	145	188	9	288	188	9

[14] The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs.
[15] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
[16] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.

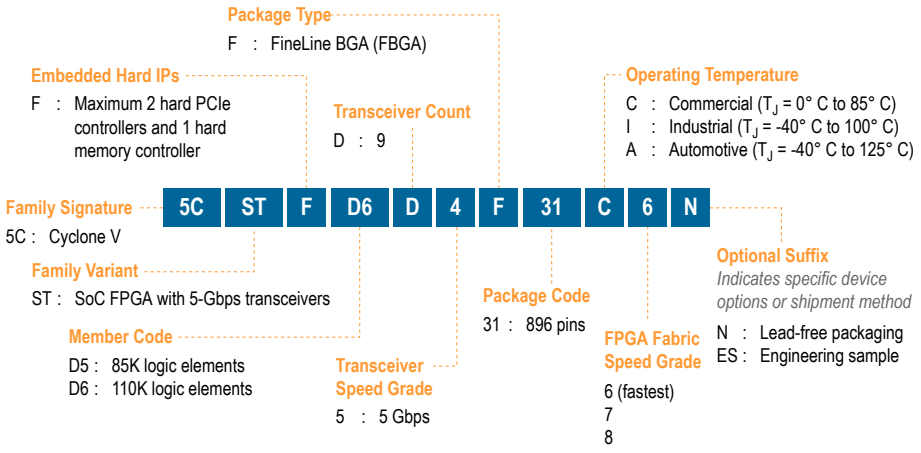
Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

Available Options

The following figure shows sample ordering code and lists the options available for Cyclone V ST devices.

Figure 6: Sample Ordering Code and Available Options for Cyclone V ST Devices—Preliminary



Maximum Resources

Table 14: Maximum Resource Counts for Cyclone V ST Devices—Preliminary

Resource		Member Code	
		D5	D6
Logic Elements (LE) (K)		85	110
ALM		32,075	41,509
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,140
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL[17]		6	6
HPS PLL		3	3
5 Gbps Transceiver		9	9
FPGA GPIO[18]		288	288
HPS I/O		188	188

[17] The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs.
[18] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.

Resource	Member Code	
	D5	D6
LVDS[19]	72	72
PCIe Hard IP Block	2	2
FPGA Hard Memory Controller	1	1
HPS Hard Memory Controller	1	1
ARM Cortex-A9 MPCore Processor	Dual-core	Dual-core

Package Plan

Table 15: Package Plan for Cyclone V ST Devices—Preliminary

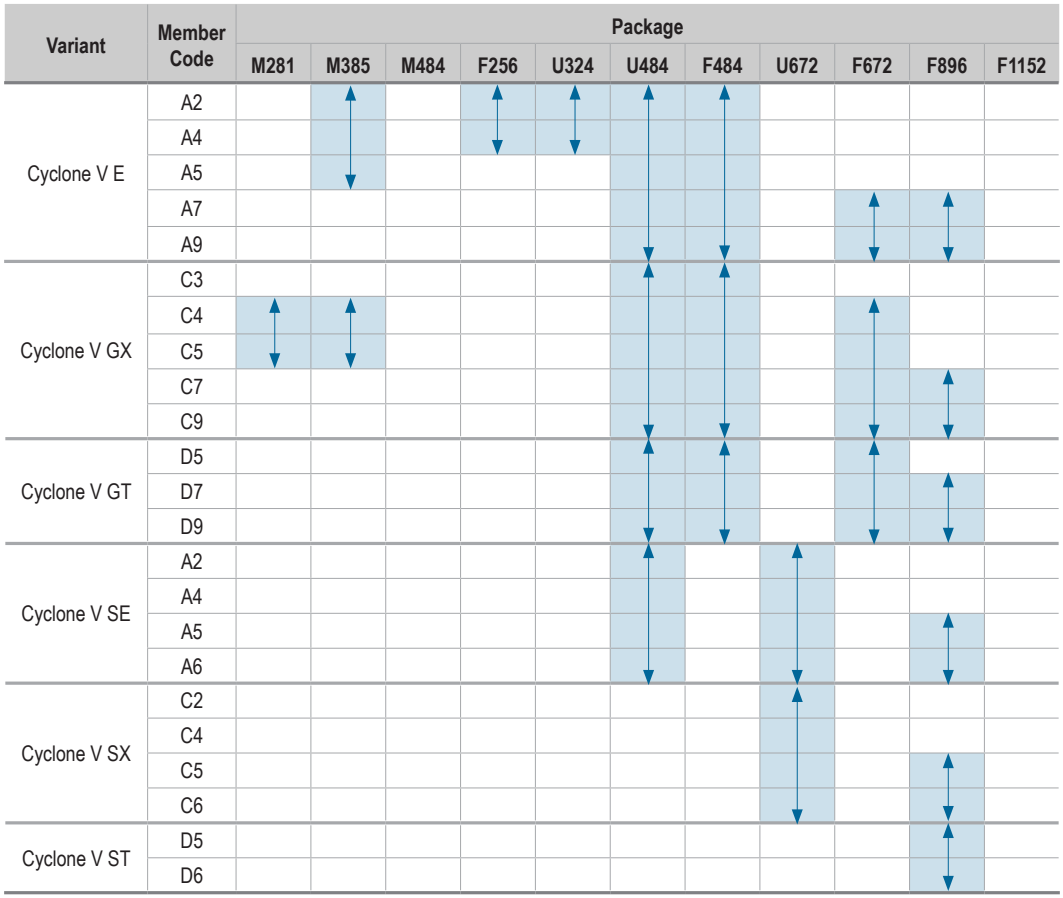
Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	188	9[20]
D6	288	188	9[20]

[19] For the number of LVDS channels in each package, refer to the *I/O Features in Cyclone V Devices* chapter.
[20] IIf you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Altera recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

I/O Vertical Migration for Cyclone V Devices

Figure 7: Vertical Migration Capability Across Cyclone V Device Packages and Densities—Preliminary

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



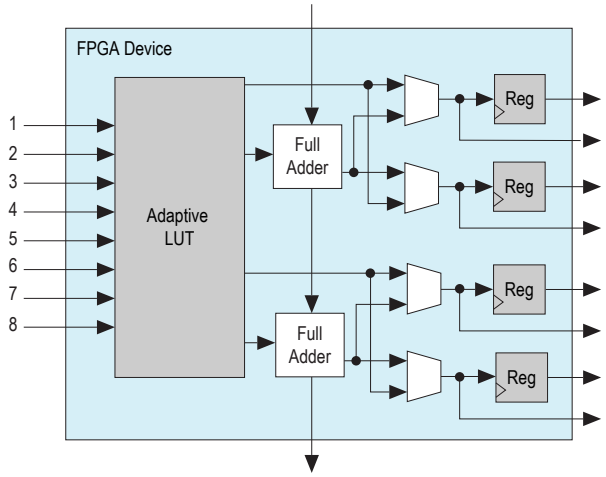
Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus® II software Pin Planner. For more information, refer to the *"I/O Management"* chapter in the *Quartus II Handbook*.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 8: ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs. For more information, refer to *Embedded Memory Capacity in Cyclone V Devices* on page standalone-17.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus II design software

Table 16: Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17: Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V GX	C3	51	153	102	51	51	51
	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	58	174	116	58	58	58
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	58	174	116	58	58	58
	C5	87	261	174	87	87	87
	C6	112	336	224	112	112	112
Cyclone V ST	D5	87	261	174	87	87	87
	D6	112	336	224	112	112	112

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks blocks—blocks of dedicated memory resources. The M10K blocks blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Cyclone V Devices

Table 18: Embedded Memory Capacity and Distribution in Cyclone V Devices

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V E	A2	176	1,760	314	196	1,956
	A4	308	3,080	485	303	3,383
	A5	446	4,460	679	424	4,884
	A7	686	6,860	1338	836	7,696
	A9	1,220	12,200	2748	1,717	13,917
Cyclone V GX	C3	119	1,190	255	159	1,349
	C4	250	2,500	472	295	2,795
	C5	446	4,460	679	424	4,884
	C7	686	6,860	1338	836	7,696
	C9	1,220	12,200	2748	1,717	13,917
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	224	2,240	352	220	2,460
	A5	397	3,970	768	480	4,450
	A6	514	5,140	994	621	5,761

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	224	2,240	352	220	2,460
	C5	397	3,970	768	480	4,450
	C6	514	5,140	994	621	5,761
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	514	5,140	994	621	5,761

Embedded Memory Configurations

Table 19: Supported Embedded Memory Block Configurations for Cyclone V Devices

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

Clock Networks and PLL Clock Sources

Cyclone V devices have 16 global clock networks capable of up to 550 MHz operation. The clock network architecture is based on Altera's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Quartus II software identifies all unused sections of the clock network and powers them down.

PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs

- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

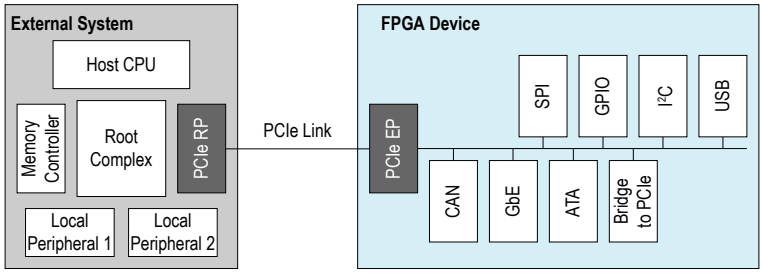
PCIe Gen1, Gen2, and Gen 3 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 9: PCIe Multifunction for Cyclone V Devices



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC FPGA devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

External Memory Performance

Table 20: External Memory Interface Performance in Cyclone V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDR3 SDRAM	1.5	400	300
	1.35	400	300
DDR2 SDRAM	1.8	400	300
LPDDR2 SDRAM	1.2	333	300

HPS External Memory Performance

Table 21: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC FPGA devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
	1.5	400
LPDDR2 SDRAM	1.2	333

Low-Power Serial Transceivers

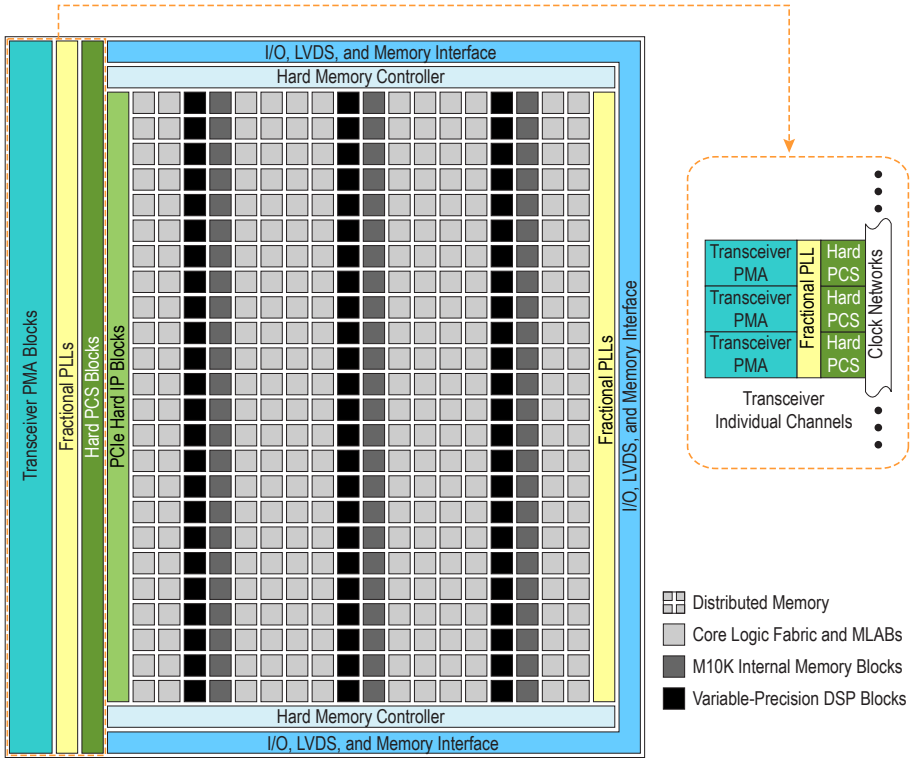
Cyclone V devices deliver the industry's lowest power 5 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

Figure 10: Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22: PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 5 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	• Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 5 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, XAUI, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 5.0 Gbps are supported.

Table 23: Transceiver PCS Features for Cyclone V Devices

PCS Support	Data Rates(Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
3-Gbps and 5-Gbps Basic	0.614 to 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Transmitter bit-slip	• Word aligner • Deskew FIFO • Rate-match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • Receiver phase compensation FIFO
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic
PCIe Gen2 (x1, x2, x4)[21]			
GbE	1.25	• Custom PHY IP core with preset feature • GbE transmitter synchronization state machine	• Custom PHY IP core with preset feature • GbE receiver synchronization state machine
XAUI	3.125	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for bonding four channels	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for realigning four channels
HiGig	3.75		
SRIO 1.3 and 2.1	1.25 to 3.125	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 channel bonding	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 deskew state machine

[21] PCIe Gen2 is supported only for Cyclone V GT devices. The PCIe Gen2 x4 support is PCIe-compatible.

PCS Support	Data Rates(Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
SDI, SD/HD, and 3G-SDI	0.27[22], 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature
JESD204A	0.3125[23] to 3.125		
Serial ATA Gen1 and Gen2	1.5 and 3.0	• Custom PHY IP core with preset feature • Electrical idle	• Custom PHY IP core with preset feature • Signal detect • Wider spread of asynchronous SSC
CPRI 4.1[24]	0.6144 to 4.9152	• Dedicated deterministic latency PHY IP core • Transmitter (TX) manual bit-slip mode	• Dedicated deterministic latency PHY IP core • Receiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	• Custom PHY IP core • Wider spread of asynchronous SSC
DisplayPort 1.2[25]	1.62 and 2.7		

SoC FPGA with HPS

Each SoC FPGA combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

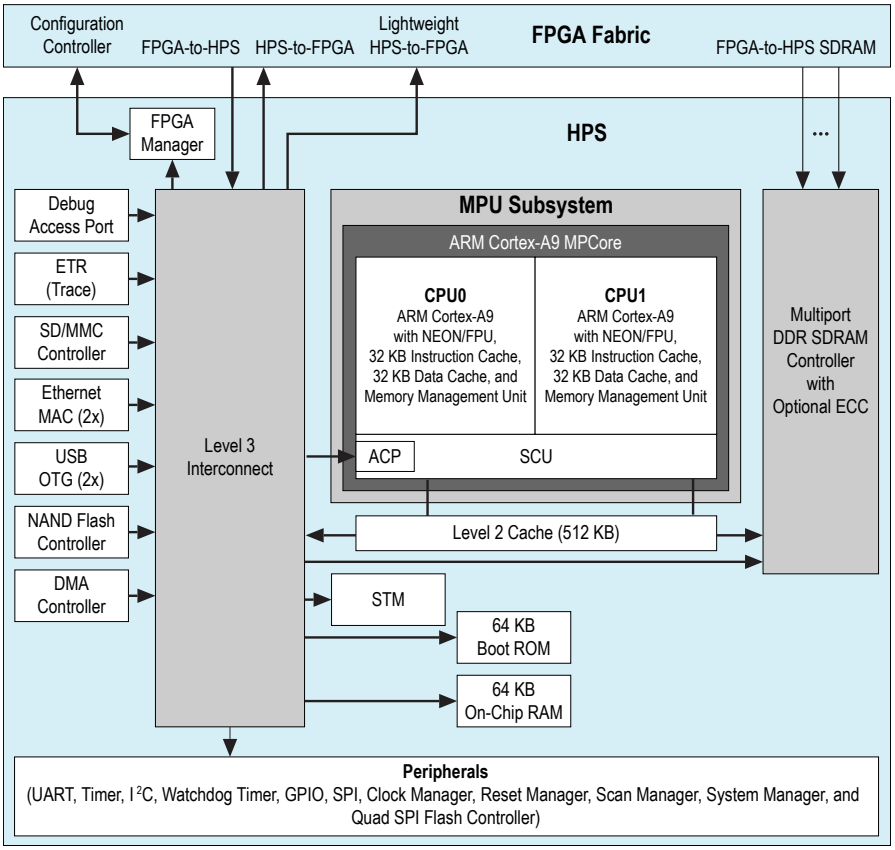
- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

[22] The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.
[23] The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.
[24] High-voltage output mode (1000-BASE-CX) is not supported.
[25] Pending characterization.

Figure 11: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower performance 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the

FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC FPGA are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus II software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems will be available for the SoC FPGAs. For more information on the operating systems support availability, contact the *Altera sales team*.

You can begin device-specific firmware and software development on the Altera SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus II design software. With the Altera® solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration modes.

Table 24: Configuration Modes and Features Supported by Cyclone V Devices

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration	Remote System Update
CvP (PCIe)	x1, x2, and x4 lanes	—	—	—	Yes	—	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

For more information about CvP, refer to the *Configuration via Protocol (CvP) Implementation in Altera FPGAs User Guide*.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History

Date	Version	Changes
December 2012	2012.12.28	• Updated the pin counts for the MBGA packages. • Updated the GPIO and transceiver counts for the MBGA packages. • Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. • Updated the vertical migration table for vertical migration of the U484 packages. • Updated the MLAB supported programmable widths at 32 bits depth.

Date	Version	Changes
November 2012	2012.11.19	• Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. • Added ordering code for five-transceiver devices for Cyclone V GT and ST. • Updated the vertical migration table to add MBGA packages. • Added performance information for HPS memory controller. • Removed DDR3U support. • Updated Cyclone V ST speed grade information. • Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. • Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. • Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	• Restructured the document. • Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. • Added Table 1, Table 3, Table 16, Table 19, and Table 20. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18. • Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. • Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. • Text edits throughout the document.
February 2012	1.2	• Updated Table 1–2, Table 1–3, and Table 1–6. • Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15. • Updated Figure 1–1 and Figure 1–6.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. • Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8. • Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20. • Minor text edits.
October 2011	1.0	Initial release.

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