19-2490; Rev 0; 7/02

EVALUATION KIT AVAILABLE

Integrated Temperature Controllers for Peltier Modules

General Description

The MAX1978/MAX1979 are the smallest, safest, most accurate complete single-chip temperature controllers for Peltier thermoelectric cooler (TEC) modules. On-chip power FETs and thermal control-loop circuitry minimize external components while maintaining high efficiency. Selectable 500kHz/1MHz switching frequency and a unique ripple-cancellation scheme optimize component size and efficiency while reducing noise. Switching speeds of internal MOSFETs are optimized to reduce noise and EMI. An ultra-low-drift chopper amplifier maintains ±0.001°C temperature stability. Output current, rather than voltage, is directly controlled to eliminate current surges. Individual heating and cooling current and voltage limits provide the highest level of TEC protection.

The MAX1978 operates from a single supply and provides bipolar ±3A output by biasing the TEC between the outputs of two synchronous buck regulators. True bipolar operation controls temperature without "dead zones" or other nonlinearities at low load currents. The control system does not hunt when the set point is very close to the natural operating point, where only a small amount of heating or cooling is needed. An analog control signal precisely sets the TEC current. The MAX1979 provides unipolar output up to 6A.

A chopper-stabilized instrumentation amplifier and a high-precision integrator amplifier are supplied to create a proportional-integral (PI) or proportional-integral-derivative (PID) controller. The instrumentation amplifier can interface to an external NTC or PTC thermistor, thermocouple, or semiconductor temperature sensor. Analog outputs are provided to monitor TEC temperature and current. In addition, separate overtemperature and undertemperature outputs indicate when the TEC temperature is out of range. An on-chip voltage reference provides bias for a thermistor bridge.

The MAX1978/MAX1979 are available in a low-profile 48-lead thin QFN-EP package and is specified over the -40°C to +85°C temperature range. The thermally enhanced QFN-EP package with exposed metal pad minimizes operating junction temperature. An evaluation kit is available to speed designs.

Applications

Fiber Optic Laser Modules

WDM, DWDM Laser-Diode Temperature Control

Fiber Optic Network Equipment

EDFA Optical Amplifiers

Telecom Fiber Interfaces

ATE

Typical Operating Circuit appears at end of data sheet.

Features

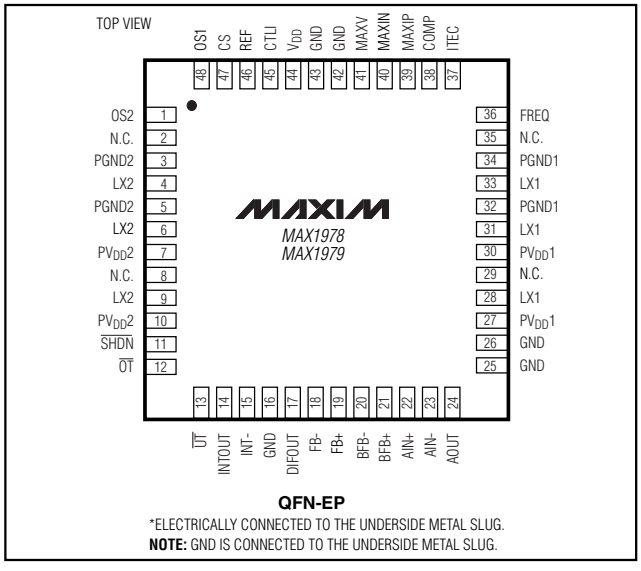
- **Smallest, Safest, Most Accurate Complete Single-Chip Controller**
- **On-Chip Power MOSFETS—No External FETs**
- **Circuit Footprint < 0.93in²**
- **Circuit Height < 3mm**
- **Temperature Stability to 0.001°C**
- **Integrated Precision Integrator and Chopper Stabilized Op Amps**
- **Accurate, Independent Heating and Cooling Current Limits**
- **Eliminates Surges By Directly Controlling TEC Current**
- **Adjustable Differential TEC Voltage Limit**
- **Low-Ripple and Low-Noise Design**
- **TEC Current Monitor**
- **Temperature Monitor**
- **Over- and Undertemperature Alarm**
- **Bipolar ±3A Output Current (MAX1978)**
- **Unipolar +6A Output Current (MAX1979)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1978ETM	-40°C to +85°C	48 Thin QFN-EP*
MAX1979ETM	-40°C to +85°C	48 Thin QFN-EP

**EP = Exposed pad.*

Pin Configuration



QFN-EP

*ELECTRICALLY CONNECTED TO THE UNDERSIDE METAL SLUG.
NOTE: GND IS CONNECTED TO THE UNDERSIDE METAL SLUG.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Integrated Temperature Controllers for Peltier Modules

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
$\overline{SHDN}$, MAXV, MAXIP, MAXIN, CTLI, $\overline{OT}$, $\overline{UT}$ to GND.....-0.3V to +6V
FREQ, COMP, OS1, OS2, CS, REF, ITEC, AIN+, AIN-, AOUT, INT-, INTOUT, BFB+, BFB-, FB+, FB-, DIFOUT to GND.....-0.3V to (V_{DD} + 0.3V)
$PV_{DD}1$, $PV_{DD}2$ to V_{DD} .....-0.3V to +0.3V
$PV_{DD}1$, $PV_{DD}2$ to GND.....-0.3V to (V_{DD} + 0.3V)
PGND1, PGND2 to GND .....-0.3V to +0.3V
COMP, REF, ITEC, $\overline{OT}$, $\overline{UT}$, INTOUT, DIFOUT, BFB-, BFB+, AOUT Short to GND .....Indefinite
Peak LX Current (MAX1978) (Note 1).....±4.5A
Peak LX Current (MAX1979) (Note 1).....+9A
Continuous Power Dissipation (T_A = +70°C)
48-Lead Thin QFN-EP
(derate 26.3mW/°C above +70°C) (Note 2).....2.105W
Operating Temperature Ranges
MAX1978ETM .....-40°C to +85°C
MAX1979ETM .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND and PV_{DD}. Applications that forward bias these diodes should not exceed the IC's package power dissipation limits.

Note 2: Solder underside metal slug to PC board ground plane.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, FREQ = GND, CTLI = FB+ = FB- = MAXV = MAXIP = MAXIN = REF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}			3.0		5.5	V
Output Voltage Range	V_{OUT}	V_{DD} = 5V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1978)		-4.3		+4.3	V
		V_{DD} = 5V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1979)				4.3	
		V_{DD} = 3V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1978)		-2.3		+2.3	
		V_{DD} = 3V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1979)				2.3	
Maximum TEC Current	$I_{TEC(MAX)}$	MAX1978				±3	A
		MAX1979				6	
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.485	1.500	1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = +10µA to -1mA			1.2	5	mV
Current-Sense Threshold		V_{OS1} < V_{CS}	$V_{MAXI_}$ = V_{REF}	135	150	160	mV
			$V_{MAXI_}$ = V_{REF}/3	40	50	60	
		V_{OS1} > V_{CS}	$V_{MAXI_}$ = V_{REF}	135	150	160	
			$V_{MAXI_}$ = V_{REF}/3	40	50	60	
NFET On-Resistance	$R_{DS(ON-N)}$	V_{DD} = 5V, I = 0.5A			0.04	0.07	Ω
		V_{DD} = 3V, I = 0.5A			0.06	0.08	
PFET On-Resistance	$R_{DS(ON-P)}$	V_{DD} = 5V, I = 0.5A			0.06	0.10	Ω
		V_{DD} = 3V, I = 0.5A			0.09	0.12	
NFET Leakage	$I_{LEAK(N)}$	V_{LX} = V_{DD} = 5V, T_A = +25°C			0.02	10	µA
		V_{LX} = V_{DD} = 5V, T_A = +85°C			1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, FREQ = GND, CTLI = FB+ = FB- = MAXV = MAXIP = MAXIN = REF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PFET Leakage	$I_{LEAK(P)}$	V_{LX} = 0, T_A = +25°C		0.02	10	µA
		V_{LX} = 0, T_A = +85°C		1		
No-Load Supply Current	$I_{DD(NO\ LOAD)}$	V_{DD} = 5V		30	50	mA
		V_{DD} = 3.3V		15	30	
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = GND, V_{DD} = 5V (Note 3)		2	3	mA
Thermal Shutdown	$T_{SHUTDOWN}$	Hysteresis = 15°C		165		°C
UVLO Threshold	V_{UVLO}	V_{DD} rising	2.4	2.6	2.8	V
		V_{DD} falling	2.25	2.5	2.75	
Switching Frequency Internal Oscillator	f_{SW-INT}	FREQ = GND	450	500	650	kHz
		FREQ=V_{DD}	800	1000	1200	
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0 or V_{DD}	-100		+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, I_{FREQ}	0 or V_{DD}	-5		+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V			0.25 × V_{DD}	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V	0.75 × V_{DD}			V
MAXV Threshold Accuracy		V_{MAXV} = V_{REF} × 0.67, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V	-1		+1	%
		V_{MAXV} = V_{REF} × 0.33, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V	-2		+2	
MAXV, MAXIP, MAXIN Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	V_{MAXV} = $V_{MAXI_}$ = 0.1V or 1.5V	-0.1		+0.1	µA
CTLI Gain	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 4)	9.5	10	10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF	0.5	1.0	2.0	MΩ
Error Amp Transconductance	g_m		50	100	175	µS
ITEC Accuracy		V_{OS1} to V_{CS} = +100mV or -100mV	-10		+10	%
ITEC Load Regulation	ΔV_{ITEC}	V_{OS1} to V_{CS} = +100mV or -100mV, I_{ITEC} = ±10µA	-0.1		+0.1	%
Instrumentation Amp Input Bias Current	$I_{DIF-BIAS}$		-10	0	+10	nA
Instrumentation Amp Offset Voltage	V_{DIF-OS}	V_{DD} = 3V to 5.5V	-200	+20	+200	µV
Instrumentation Amp Offset-Voltage Drift with Temperature		V_{DD} = 3V to 5.5V		0.1		µV/°C
Instrumentation Amp Preset Gain	A_{DIF}	R_{LOAD} = 10kΩ to REF	45	50	55	V/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, FREQ = GND, CTLI = FB+ = FB- = MAXV = MAXIP = MAXIN = REF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integrator Amp Open-Loop Gain	A_{OL-INT}	R_{LOAD} = 10kΩ to REF		120		dB
Integrator Amp CMRR	$CMRR_{INT}$			100		dB
Integrator Amp Input Bias Current	$I_{INT-BIAS}$	V_{DD} = 3V to 5.5V			1	nA
Integrator Amp Voltage Offset	V_{INT-OS}	V_{DD} = 3V to 5.5V	-3	+0.1	+3	mV
Integrator Amp Gain Bandwidth	GBW_{INT}			100		kHz
Undedicated Chopper Amp Open-Loop Gain	A_{OL-AIN}	R_{LOAD} = 10kΩ to REF		120		dB
Undedicated Chopper Amp CMRR	$CMRR_{AIN}$			85		dB
Undedicated Chopper Amp Input Bias Current	$I_{AIN-BIAS}$	V_{DD} = 3V to 5.5V	-10	0	+10	nA
Undedicated Chopper Amp Offset Voltage	V_{AIN-OS}	V_{DD} = 3V to 5.5V	-200	+10	+200	µV
Undedicated Chopper Amp Gain Bandwidth	GBW_{AIN}			100		kHz
Undedicated Chopper Amp Output Ripple	V_{RIPPLE}	A = 5		20		mV
BFB_ Buffer Error		C_{LOAD} < 100pF	-200	0	+200	µV
$\overline{UT}$ and $\overline{OT}$ Leakage Current	I_{LEAK}	$V_{\overline{UT}}$ = $V_{\overline{OT}}$ = 5.5V			1	µA
$\overline{UT}$ and $\overline{OT}$ Output Low Voltage	V_{OL}	Sinking 4mA		50	150	mV
$\overline{UT}$ Trip Threshold		FB+ - FB- (see *Typical Application Circuit*)		-20		mV
$\overline{OT}$ Trip Threshold		FB+ - FB- (see *Typical Application Circuit*)		20		mV

ELECTRICAL CHARACTERISTICS

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, FREQ = GND, CTLI = FB+ = FB- = MAXV = MAXIP = MAXIN = REF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Supply Range	V_{DD}			3	5.5	V
Output Voltage Range	V_{OUT}	V_{DD} = 5V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} -V_{OS2} (MAX1978)		-4.3	+4.3	V
		V_{DD} = 5V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1979)			4.3	
		V_{DD} = 3V, I_{TEC} = 0 to ±3A, V_{OUT} = V_{OS1} - V_{OS2} (MAX1978)		-2.3	+2.3	
		V_{DD} = 3V, I_{TEC} = 0 to 6A, V_{OUT} = V_{OS1} (MAX1979)			2.3	
Maximum TEC Current	$I_{TEC(MAX)}$	MAX1978			±3	A
		MAX1979			6	
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.475	1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 10µA to -1mA			5	mV
Current-Sense Threshold		V_{OS1} < V_{CS}	$V_{MAXI_}$ = V_{REF}	135	160	mV
			$V_{MAXI_}$ = V_{REF}/3	40	60	
		V_{OS1} > V_{CS}	$V_{MAXI_}$ = V_{REF}	135	160	
			$V_{MAXI_}$ = V_{REF}/3	40	60	
No-Load Supply Current	$I_{DD(NO\ LOAD)}$	V_{DD} = 5V			50	mA
		V_{DD} = 3.3V			30	
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = GND, V_{DD} = 5V (Note 3)			3	mA
UVLO Threshold	V_{UVLO}	V_{DD} rising		2.4	2.8	V
		V_{DD} falling		2.25	2.75	
Switching Frequency Internal Oscillator	f_{SW-INT}	FREQ = GND		450	650	kHz
		FREQ = V_{DD}		800	1200	
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0 or V_{DD}		-100	+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, $I_{\overline{FREQ}}$	0 or V_{DD}		-5	+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V			0.25 × V_{DD}	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V		0.75 × V_{DD}		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $PV_{DD}1$ = $PV_{DD}2$ = $\overline{SHDN}$ = 5V, FREQ = GND, CTLI = FB+ = FB- = MAXV = MAXIP = MAXIN = REF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
MAXV Threshold Accuracy		$V_{MAXV} = V_{REF} \times 0.67$, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V	-1	+1	%
		$V_{MAXV} = V_{REF} \times 0.33$, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V	-2	+2	
MAXV, MAXIP, MAXIN Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	$V_{MAXV} = V_{MAXI_}$ = 0.1V or 1.5V	-0.1	+0.1	µA
CTLI Gain	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 4)	9.5	10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF	0.5	2.0	MΩ
Error Amp Transconductance	g_m		50	175	µS
ITEC Accuracy		V_{OS1} to V_{CS} = +100mV or -100mV	-10	+10	%
ITEC Load Regulation	ΔV_{ITEC}	V_{OS1} to V_{CS} = +100mV or -100mV, I_{ITEC} = ±10µA	-0.125	+0.125	%
Instrumentation Amp Input Bias Current	$I_{DIF-BIAS}$		-10	+10	nA
Instrumentation Amp Offset Voltage	V_{DIF-OS}	V_{DD} = 3V to 5.5V	-200	+200	µV
Instrumentation Amp Preset Gain	A_{DIF}	R_{LOAD} = 10kΩ to REF	45	55	V/V
Integrator Amp Input Bias Current	$I_{INT-BIAS}$	V_{DD} = 3V to 5.5V		1	nA
Integrator Amp Voltage Offset	V_{INT-OS}	V_{DD} = 3V to 5.5V	-3	+3	mV
Undedicated Chopper Amp Input Bias Current	$I_{AIN-BIAS}$	V_{DD} = 3V to 5.5V	-10	+10	nA
Undedicated Chopper Amp Offset Voltage	V_{AIN-OS}	V_{DD} = 3V to 5.5V	-200	+200	µV
BFB_ Buffer Error		C_{LOAD} < 100pF	-200	+200	µV
$\overline{UT}$ and $\overline{OT}$ Leakage Current	I_{LEAK}	$V_{\overline{UT}} = V_{\overline{OT}}$ = 5.5V		1	µA
$\overline{UT}$ and $\overline{OT}$ Output Low Voltage	V_{OL}	Sinking 4mA		150	mV

Note 3: Includes power FET leakage.

Note 4: CTLI gain is defined as:

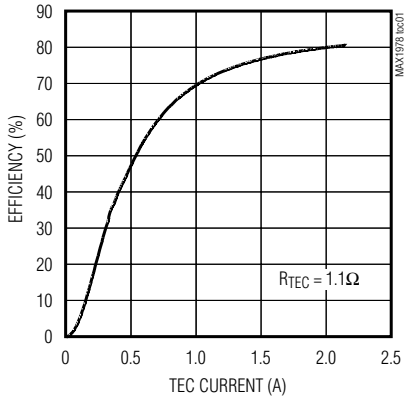
$$A_{CTLI} = \frac{(V_{CTLI} - V_{REF})}{(V_{OSI} - V_{CS})}$$

Note 5: Specifications to -40°C are guaranteed by design, not production tested.

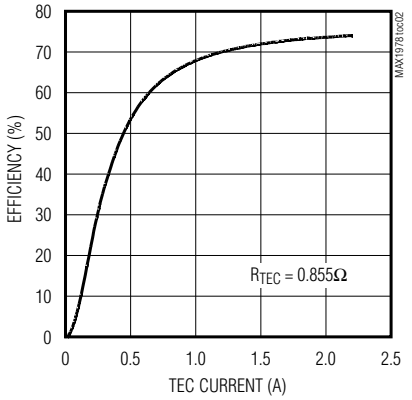
Typical Operating Characteristics

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, RTEC = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

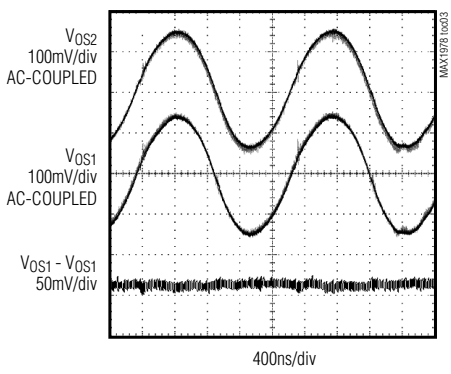
EFFICIENCY vs. TEC CURRENT
V_{DD} = 5V



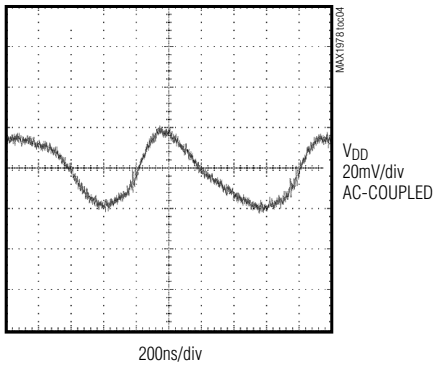
EFFICIENCY vs. TEC CURRENT
V_{DD} = 3.3V



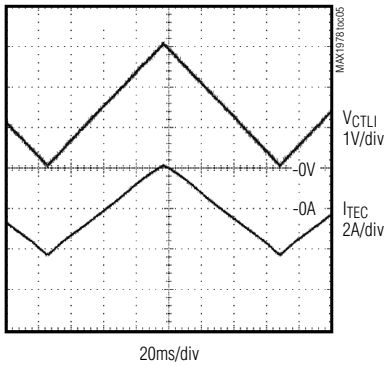
OUTPUT-VOLTAGE RIPPLE WAVEFORMS



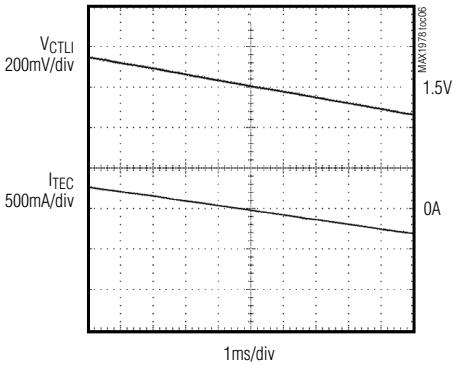
INPUT SUPPLY RIPPLE



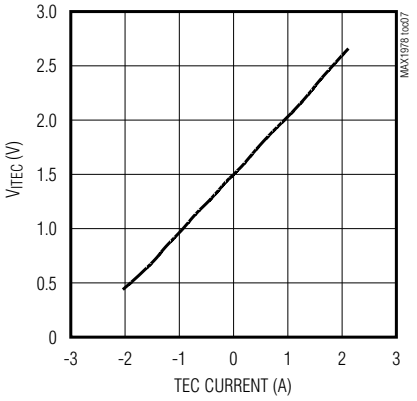
TEC CURRENT vs. CTLI VOLTAGE



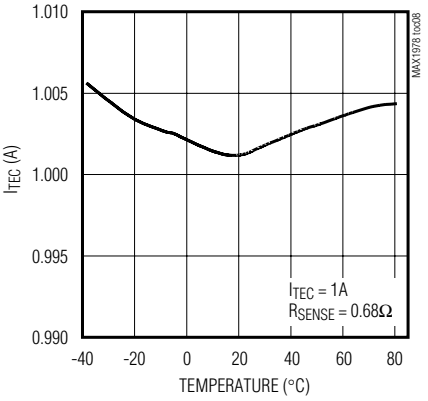
ZERO-CROSSING TEC CURRENT



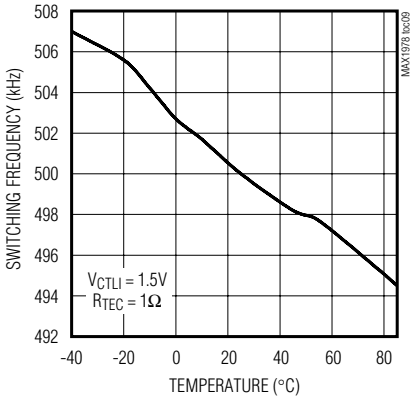
V_{ITEC} vs. TEC CURRENT



TEC CURRENT vs. TEMPERATURE



SWITCHING FREQUENCY vs. TEMPERATURE

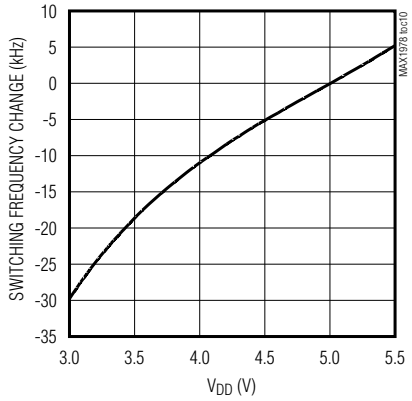


Integrated Temperature Controllers for Peltier Modules

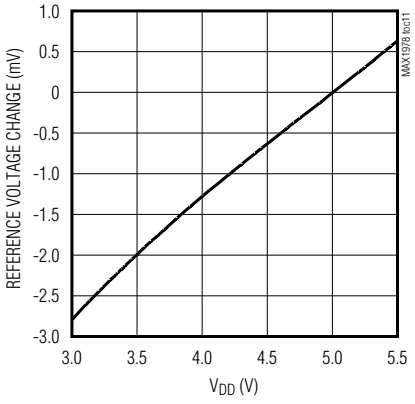
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, RTEC = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

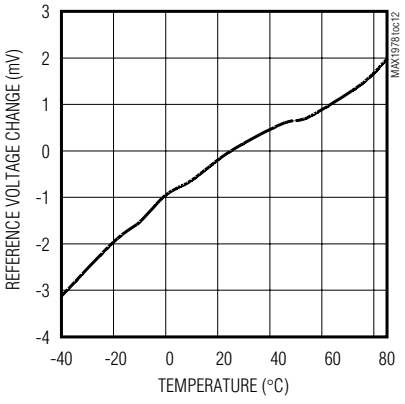
SWITCHING FREQUENCY CHANGE vs. INPUT SUPPLY



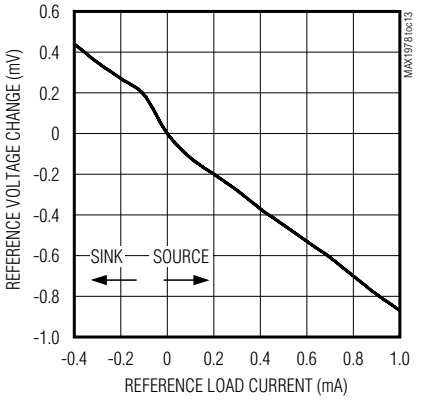
REFERENCE VOLTAGE CHANGE vs. INPUT SUPPLY



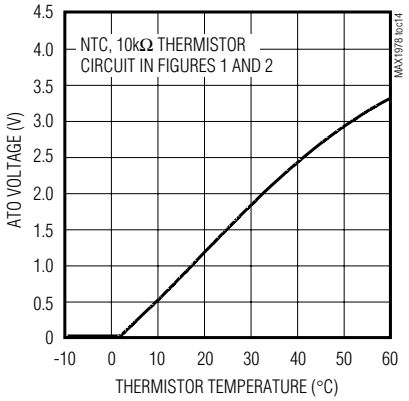
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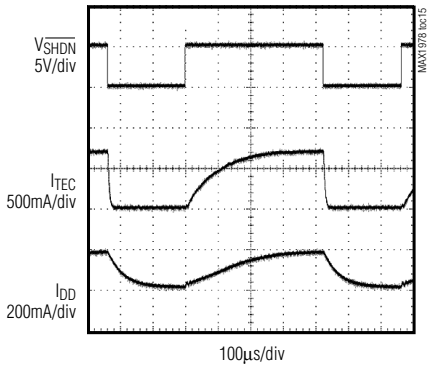
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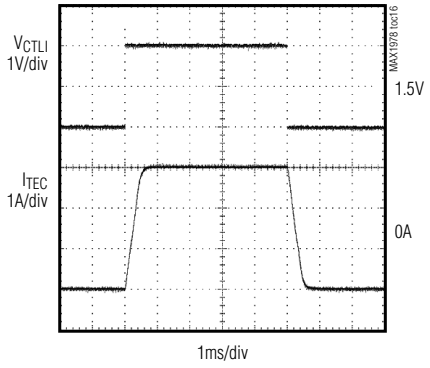
ATO VOLTAGE vs. THERMISTOR TEMPERATURE



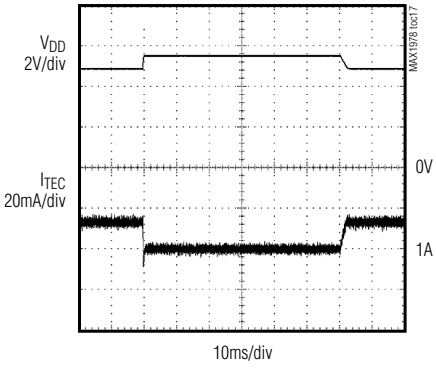
STARTUP AND SHUTDOWN WAVEFORMS



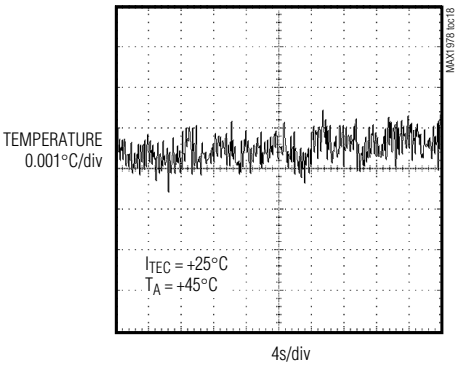
CTLI STEP RESPONSE



INPUT SUPPLY STEP RESPONSE



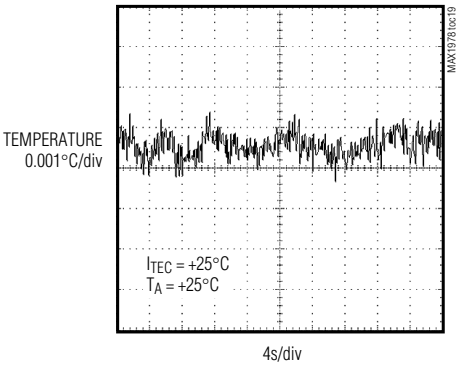
THERMAL STABILITY, COOLING MODE



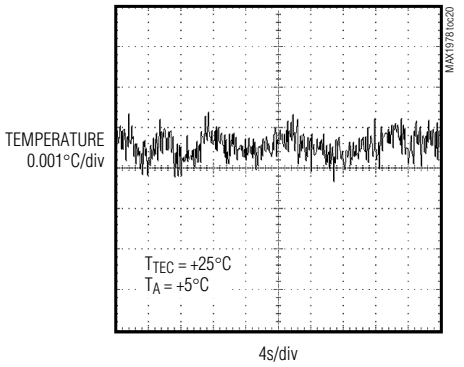
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{CTLI} = 1V, V_{FREQ} = GND, RTEC = 1Ω, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

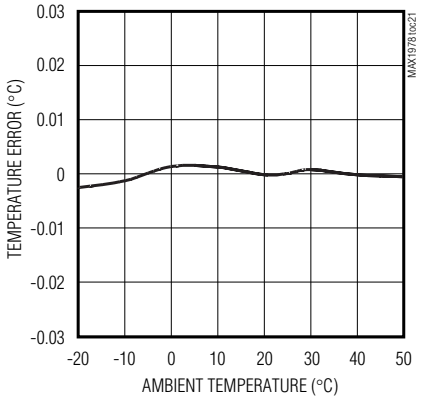
THERMAL STABILITY, ROOM TEMPERATURE



THERMAL STABILITY, HEATING MODE



TEMPERATURE ERROR vs. AMBIENT TEMPERATURE



Pin Description

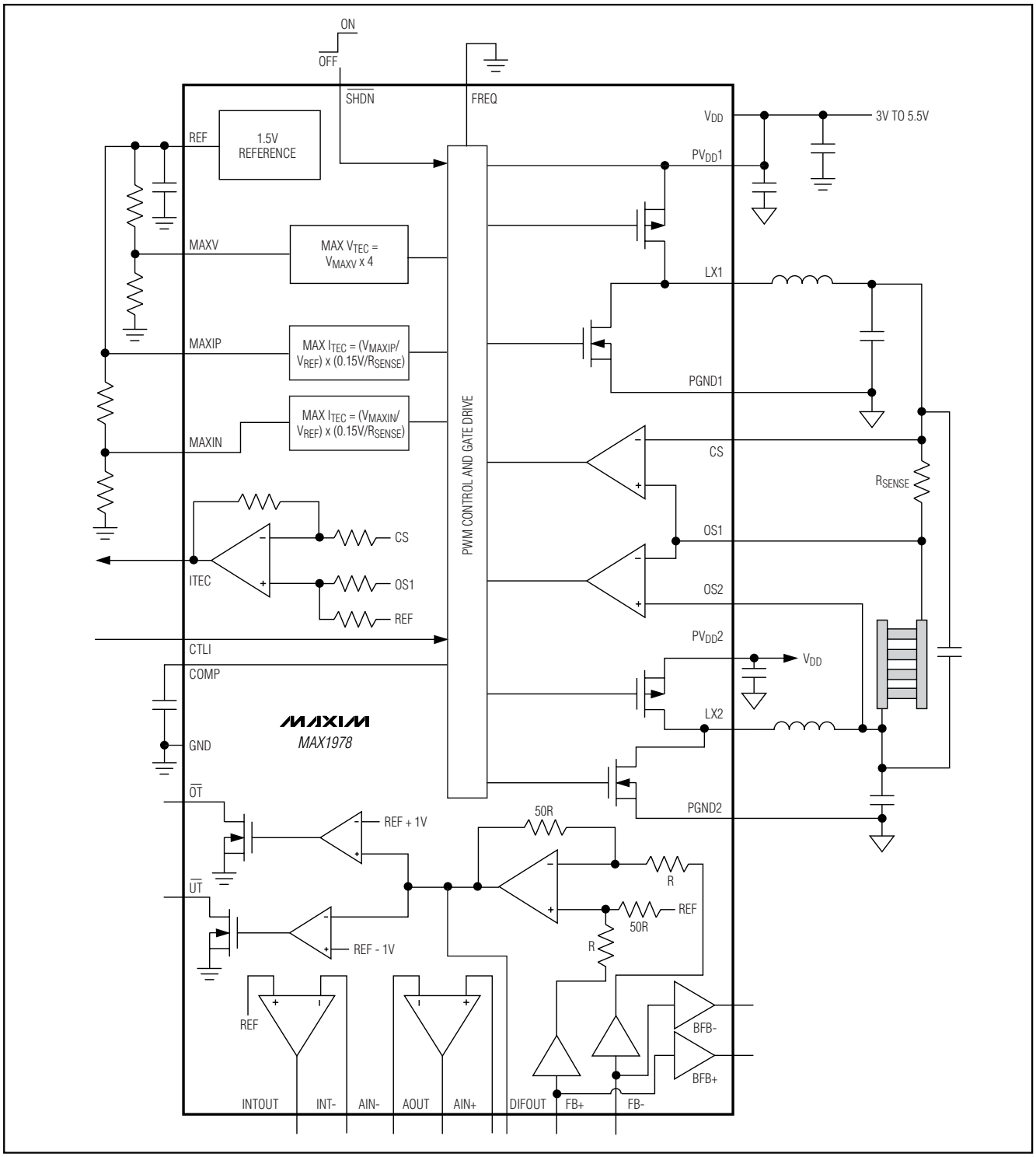
PIN	NAME	FUNCTION
1	OS2	Output Sense 2. OS2 senses one side of the differential TEC voltage. OS2 is a sense point, not a power output.
2, 8, 29, 35	N.C.	Not Internally Connected
3, 5	PGND2	Power Ground 2. Internal synchronous rectifier ground connections. Connect all PGND pins together at power ground plane.
4, 6, 9	LX2	Inductor 2 Connection. Connect all LX2 pins together. Connect LX2 to LX1 when using the MAX1979.
7, 10	$PV_{DD}2$	Power 2 Inputs. Must be same voltage as V_{DD}. Connect all $PV_{DD}2$ inputs together at the V_{DD} power plane. Bypass to PGND2 with a 10µF ceramic capacitor.
11	$\overline{SHDN}$	Shutdown Control Input. Active-low shutdown control.
12	$\overline{OT}$	Under-Temperature Alarm. Open-drain output pulls low if temperature feedback falls 20mV (typically +1.5°C) below the set-point voltage.
13	$\overline{UT}$	Under-Temperature Alarm. Open-drain output pulls low if temperature feedback falls 20mV (typically +1.5°C) below the set-point voltage.
14	INTOUT	Integrator Amp Output. Normally connected to CTLI.
15	INT-	Integrator Amp Inverting Input. Normally connected to DIFOUT through thermal-compensation network.
16, 25, 26, 42, 43	GND	Analog Ground. Connect all GND pins to analog ground plane.
17	DIFOUT	Chopper-Stabilized Instrumentation Amp Output. Differential gain is 50 × (FB+ - FB-).
18	FB-	Chopper-Stabilized Instrumentation Amp Inverting Input. Connect to thermistor bridge.
19	FB+	Chopper-Stabilized Instrumentation Amp Noninverting Input. Connect to thermistor bridge.
20	BFB-	Chopper-Stabilized Buffered FB- Output. Used to monitor thermistor bridge voltage.
21	BFB+	Chopper-Stabilized Buffered FB+ Output. Used to monitor thermistor bridge voltage.
22	AIN+	Undedicated Chopper-Stabilized Amplifier Noninverting Input

Integrated Temperature Controllers for Peltier Modules

Pin Description (continued)

PIN	NAME	FUNCTION
23	AIN-	Undedicated Chopper-Stabilized Amplifier Inverting Input
24	AOUT	Undedicated Chopper-Stabilized Amplifier Output
27, 30	$PV_{DD}1$	Power 1 Inputs. Must be same voltage as V_{DD}. Connect all $PV_{DD}1$ inputs together at the V_{DD} power plane. Bypass to PGND1 with a 10µF ceramic capacitor.
28, 31, 33	LX1	Inductor 1 Connection. Connect all LX1 pins together. Connect LX1 to LX2 when using the MAX1979.
32, 34	PGND1	Power Ground 1. Internal synchronous-rectifier ground connections. Connect all PGND pins together at power ground plane.
36	FREQ	Switching-Frequency Select. Low = 500kHz, high = 1MHz.
37	ITEC	TEC Current Monitor Output. The ITEC output voltage is a function of the voltage across the TEC current-sense resistor. $V_{ITEC} = 1.50V + (V_{OS1} - V_{CS}) \times 8$.
38	COMP	Current-Control Loop Compensation. For most designs, connect a 10nF capacitor from COMP to GND.
39	MAXIP	Maximum Positive TEC Current. Connect MAXIP to REF to set default positive current limit +150mV / R_{SENSE}.
40	MAXIN	Maximum Negative TEC Current. Connect MAXIN to REF to set default negative current limit -150mV / R_{SENSE}. Connect MAXIN to GND when using the MAX1979.
41	MAXV	Maximum Bipolar TEC Voltage. Connect an external resistive divider from REF to GND to set the maximum voltage across the TEC. The maximum TEC voltage is $4 \times V_{MAXV}$.
44	V_{DD}	Analog Supply Voltage Input. Bypass to GND with a 10µF ceramic capacitor.
45	CTLI	TEC Current-Control Input. Sets differential current into the TEC. Center point is 1.50V (no TEC current). Connect to INTOUT when using the thermal control loop. $I_{TEC} = (V_{OS1} - V_{CS}) / R_{SENSE} = (V_{CTLI} - 1.50) / (10 \times R_{SENSE})$. When $(V_{CLTI} - V_{REF}) > 0$, $V_{OS2} > V_{OS1} > V_{CS}$.
46	REF	1.5V Reference Voltage Output. Bypass REF to GND with a 1µF ceramic capacitor.
47	CS	Current-Sense Input. The current through the TEC is monitored between CS and OS1. The maximum TEC current is given by 150mV / R_{SENSE} and is bipolar for the MAX1978. The MAX1979 TEC current is unipolar.
48	OS1	Output Sense 1. OS1 senses one side of the differential TEC voltage. OS1 is a sense point, not a power output.

Functional Diagram



Integrated Temperature Controllers for Peltier Modules

Detailed Description

Power Stage

The power stage of the MAX1978/MAX1979 thermoelectric cooler (TEC) temperature controllers consists of two switching buck regulators that operate together to directly control TEC current. This configuration creates a differential voltage across the TEC, allowing bidirectional TEC current for controlled cooling and heating. Controlled cooling and heating allow accurate TEC temperature control within the tight tolerances of laser driver specifications.

The voltage at CTLI directly sets the TEC current. The internal thermal-control loop drives CTLI to regulate TEC temperature. The on-chip thermal-control circuitry can be configured to achieve temperature control stability of 0.001°C. Figure 1 shows a typical TEC thermal-control circuit.

Ripple Cancellation

Switching regulators like those used in the MAX1978/MAX1979 inherently create ripple voltage on each common-mode output. The regulators in the MAX1978 switch in phase and provide complementary in-phase duty cycles, so ripple waveforms at the differential TEC output are greatly reduced. This feature suppresses ripple currents and electrical noise at the TEC to prevent interference with the laser diode while minimizing output capacitor filter size.

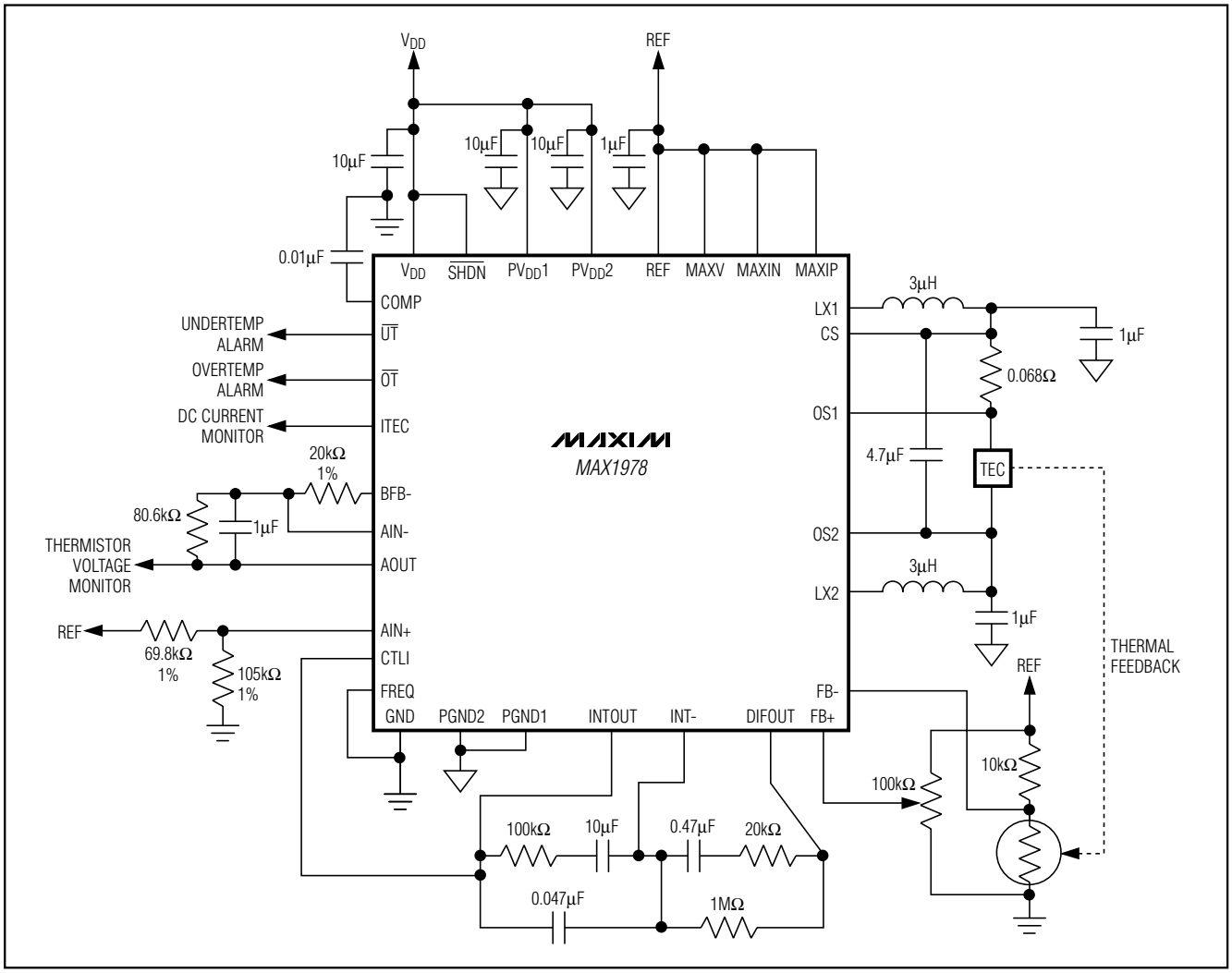


Figure 1. MAX1978 Typical Application Circuit

Switching Frequency

FREQ sets the switching frequency of the internal oscillator. The oscillator frequency is 500kHz when FREQ = GND. The oscillator frequency is 1MHz when FREQ = V_{DD}. The 1MHz setting allows minimum inductor and filter-capacitor values. Efficiency is optimized with the 500kHz setting.

Voltage and Current-Limit Settings

The MAX1978 and MAX1979 provide settings to limit the maximum differential TEC voltage. Applying a voltage to MAXV limits the maximum voltage across the TEC to $\pm(4 \times V_{MAXV})$.

The MAX1978 also limits the maximum positive and negative TEC current. The voltages applied to MAXIP and MAXIN independently set the maximum positive and negative output current limits. The MAX1979 controls TEC current in only one direction, so the maximum current is set only with MAXIP. MAXIN must be connected to GND when using the MAX1979.

Chopper-Stabilized Instrumentation Amplifier

The MAX1978 and MAX1979 include a chopped input instrumentation amplifier with a fixed gain of 50. An external thermal sensor, typically a thermistor, is connected to one of the amp's inputs. The other input is connected to a voltage that represents the temperature set point. This set point can be derived from a resistor-divider network or DAC. The included instrumentation amplifier provides low offset drift needed to prevent temperature set-point drift with ambient temperature changes. Temperature stability of 0.001°C can be achieved over a 0°C to +50°C ambient temperarure range by using the amplifier as in Figure 1. DIFOUT is the instrumentation amplifier output and is proportional to 50 times the difference between the set-point temperature and the TEC temperature. This difference is commonly referred to as the "error signal". For best temperature stability, derive the set-point voltage from the same reference that drives the thermistor (usually the MAX1978/MAX1979 REF output). This is called a "ratiometric" or "bridge" connection. The bridge connection optimizes stability by eliminating REF drift as an error source. Errors at REF are nullified because they affect the thermistor and set point equally.

The instrumentation amplifier utilizes a chopped input scheme to minimize input offset voltage and drift. This generates output ripple at DIFOUT that is equal to the chop frequency. The DIFOUT peak-to-peak ripple amplitude is typically 100mV but has no effect on temperature stability. DIFOUT ripple is filtered by the integrator in the following stage. The chopper frequency is derived from, and is synchronized to, the switching frequency of the power stage.

Integrator Amplifier

An on-chip integrator amplifier is provided on the MAX1978/MAX1979. The noninverting terminal of the amplifier is connected internally to REF. Connect an appropriate network of resistors and capacitors between DIFOUT and INT-, and connect INTOUT to CTLI for typical operation. CTLI directly controls the TEC current magnitude and polarity. The thermal-control-loop dynamics are set by the integrator input and feedback components. See the *Applications Information* section for details on thermal-loop compensation.

Current Monitor Output

ITEC provides a voltage output proportional to the TEC current, ITEC (see the *Functional Diagram*):

$$V_{ITEC} = 1.5V + 8 \times (V_{OS1} - V_{CS})$$

Over- and Under-Temperature Alarms

The MAX1978/MAX1979 provide open-drain status outputs that alert a microcontroller when the TEC temperature is over or under the set-point temperature. $\overline{OT}$ and $\overline{UT}$ pull low when $V_{(FB1+ - FB-)}$ is more than 20mV. For a typical thermistor connection, this translates to approximately 1.5°C error.

Reference Output

The MAX1978/MAX1979 include an on-chip 1.5V voltage reference accurate to 1% over temperature. Bypass REF with 1µF to GND. REF can be used to bias an external thermistor for temperature sensing as shown in Figures 1 and 2. Note that the 1% accuracy of REF does not limit the temperature stability achievable with the MAX1978/MAX1979. This is because the thermistor and set-point bridge legs are intended to be driven ratiometrically by the same reference source (REF). Variations in the bridge-drive voltage then cancel out and do not generate errors. Consequently, 0.001°C stable temperature control is achievable with the MAX1978/MAX1979 reference.

An external source can be used to bias the thermistor bridge. For best accuracy, the common-mode voltage applied to FB+ and FB- should be kept between 0.5V and 1V, however the input range can be extended from 0.2V to V_{DD} / 2 if some shift in instrumentation amp offset (approximately -50µV/V) can be tolerated. This shift remains constant with temperature and does not contribute to set-point drift.

Integrated Temperature Controllers for Peltier Modules

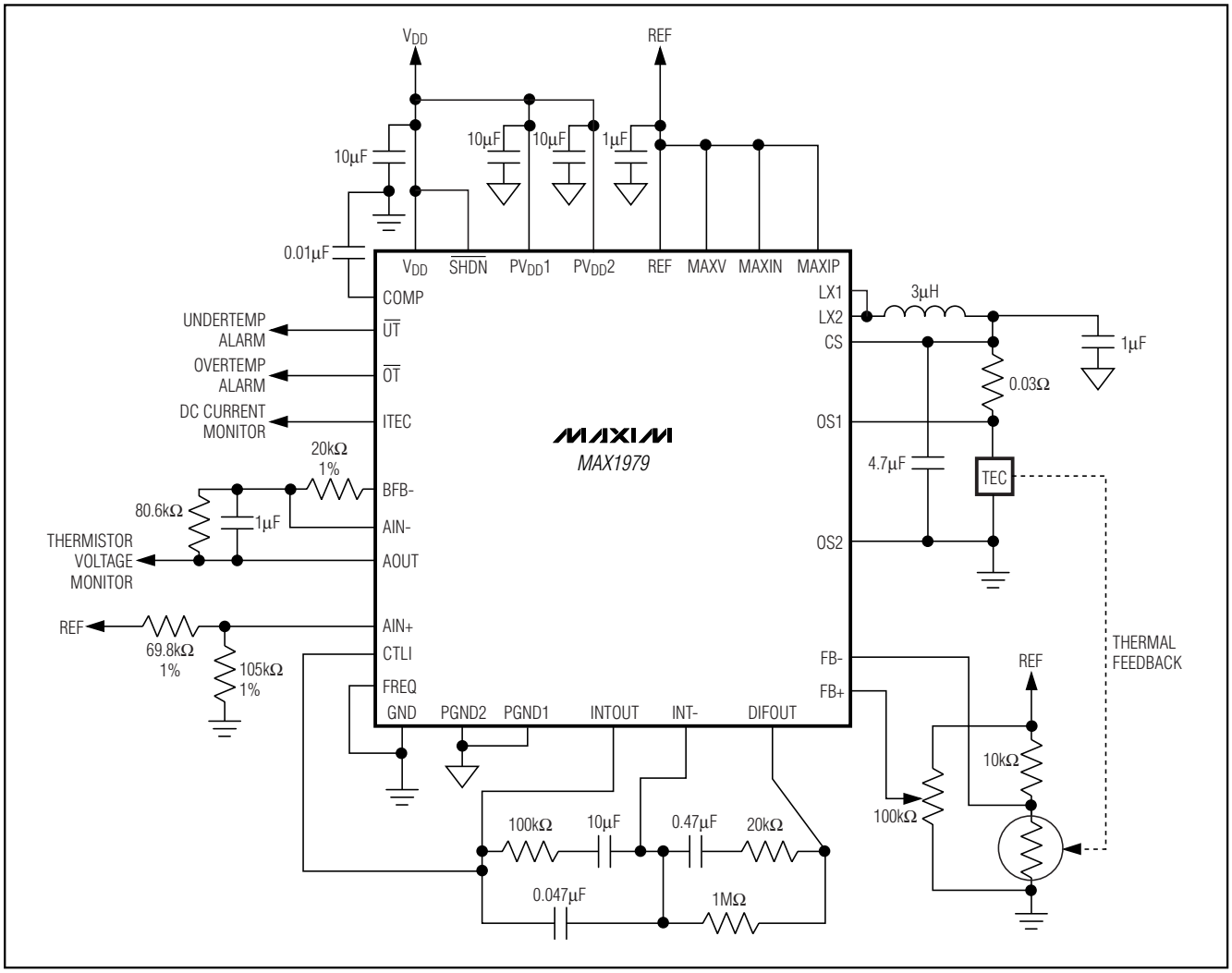


Figure 2. MAX1979 Typical Application Circuit

Buffered Outputs, BFB+ and BFB-

BFB+ and BFB- output a buffered version of the voltage that appears on FB+ and FB-, respectively. The buffers are typically used in conjunction with the undedicated chopper amplifier to create a monitor for the thermistor voltage/TEC temperature (Figures 1 and 2). These buffers are unity-gain chopper amplifiers and exhibit output ripple. Each output can be either integrated or filtered to remove the ripple content if necessary.

Undedicated Chopper-Stabilized Amplifier

In addition to the chopper amplifiers at DIFOUT and BFB_, the MAX1978/MAX1979 include an additional chopper amplifier at AOUT. This amplifier is uncommitted but is intended to provide a temperature-proportional analog output. The thermistor voltage typically is connected to the undedicated chopper amplifier through the included buffers BFB+ and BFB-. Figure 3 shows how to configure the undedicated amplifier as a thermistor voltage monitor. The output voltage at AOUT is not precisely linear, because the thermistor is not linear. AOUT is also chopper stabilized and exhibits output ripple and can be either integrated or filtered to remove the ripple content if necessary.

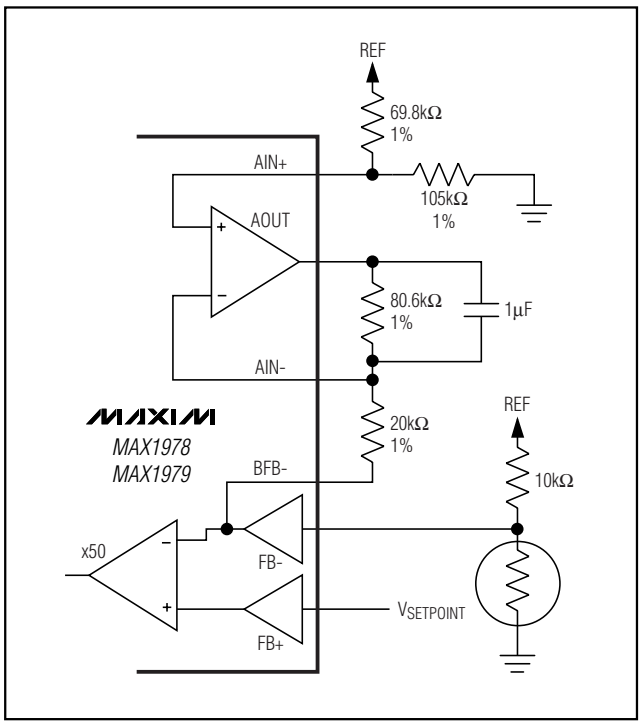


Figure 3. Thermistor Voltage Monitor

Design Procedure

Inductor Selection

Small surface-mount inductors are ideal for use with the MAX1978/MAX1979. Select the output inductors so that the LC resonant frequency of the inductance and the output capacitance is less than 1/5 the selected switching frequency. For example, 3.0µH and 1µF have a resonance at 92kHz, which is adequate for 500kHz operation.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}}$$

where:

f_{LC} = resonant frequency of output filter.

Capacitor Selection

Filter Capacitors

Decouple each power-supply input (V_{DD}, $PV_{DD}1$, and $PV_{DD}2$) with a 10µF ceramic capacitor close to the supply pins. If long supply lines separate the source supply from the MAX1978/MAX1979, or if the source supply has high output impedance, place an additional 22µF to 100µF ceramic capacitor between the V_{DD} power plane and power ground. Insufficient supply bypassing can result in supply bounce and degraded accuracy.

Compensation Capacitor

Include a compensation capacitor to ensure current-power control-loop stability. Select the capacitor so that the unity-gain bandwidth of the current-control loop is less than or equal to 10% the resonant frequency of the output filter:

$$C_{COMP} \geq \left(\frac{g_m}{f_{BW}}\right) \times \left(\frac{24 \times R_{SENSE}}{2\pi \times (R_{SENSE} + R_{TEC})}\right)$$

where:

f_{BW} = unity-gain bandwidth frequency

g_m = loop transconductance, typically 100µA/V

C_{COMP} = value of the compensation capacitor

R_{TEC} = TEC series resistance

R_{SENSE} = sense resistor

Setting Voltage and Current Limits

Consider TEC parameters to guarantee a robust design. These parameters include maximum positive current, maximum negative current, and the maximum voltage allowed across the TEC. These limits should be used to set MAXIP, MAXIN, and MAXV voltages.

Setting Max Positive and Negative TEC Current

MAXIP and MAXIN set the maximum positive and negative TEC currents, respectively. The default current limit is ±150mV / R_{SENSE} when MAXIP and MAXIN are connected to REF. To set maximum limits other than the defaults, connect a resistor-divider from REF to GND to set $V_{MAXI_}$. Use resistors in the 10kΩ to 100kΩ range. $V_{MAXI_}$ is related to ITEC by the following equations:

$$V_{MAXIP} = 10\ (I_{TECP(MAX)} \times R_{SENSE})$$
$$V_{MAXIN} = 10\ (I_{TECN(MAX)} \times R_{SENSE})$$

where $I_{TECP(MAX)}$ is the maximum positive TEC current and $I_{TECN(MAX)}$ is the maximum negative TEC current.

Positive TEC current occurs when CS is less than OS1:

$$I_{TEC} \times R_{SENSE} = CS - OS1 \text{ when } I_{TEC} < 0.$$
$$I_{TEC} \times R_{SENSE} = OS1 - CS \text{ when } I_{TEC} > 0.$$

Integrated Temperature Controllers for Peltier Modules

The MAX1979 controls the TEC current in only one direction (unipolar). Set the maximum unipolar TEC current by applying a voltage to MAXIP. Connect MAXIN to GND when using the MAX1979. The equation for setting MAXIP is the same for the MAX1978 and MAX1979. Do not exceed the positive or negative current-limit specifications on the TEC. Refer to the TEC manufacturer's data sheet for these limits.

Setting Max TEC Voltage

Apply a voltage to MAXV to control the maximum differential TEC voltage. MAXV can vary from 0 to REF. The voltage across the TEC is four times V_{MAXV} and can be positive or negative.

$$|V_{OS1} - V_{OS2}| = 4 \times V_{MAXV}$$

Use resistors from 10kΩ to 100kΩ to form a voltage-divider to set V_{MAXV}.

Thermal-Control Loop

The MAX1978/MAX1979 provide all the necessary amplifiers needed to create a thermal-control loop. Typically, the chopper-stabilized instrumentation amplifier generates an error signal and the integrator amplifier is used to create a PID controller. Figure 4 shows an example of a simple PID implementation. The error signal needed to control the loop is generated from the difference between the set point and the thermistor voltage. The desired set-point voltage can be derived from a potentiometer, DAC, or other voltage source. Figure 5 details the required connections. Connect the output of the PID controller to CTLI. For details, see the *Applications Information* section.

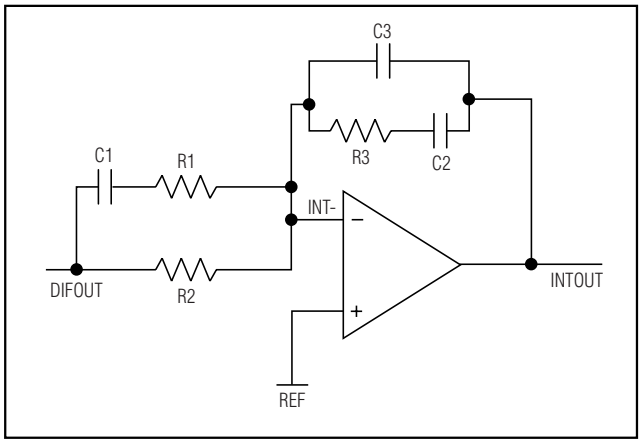


Figure 4. Proportional Integral Derivative Controller

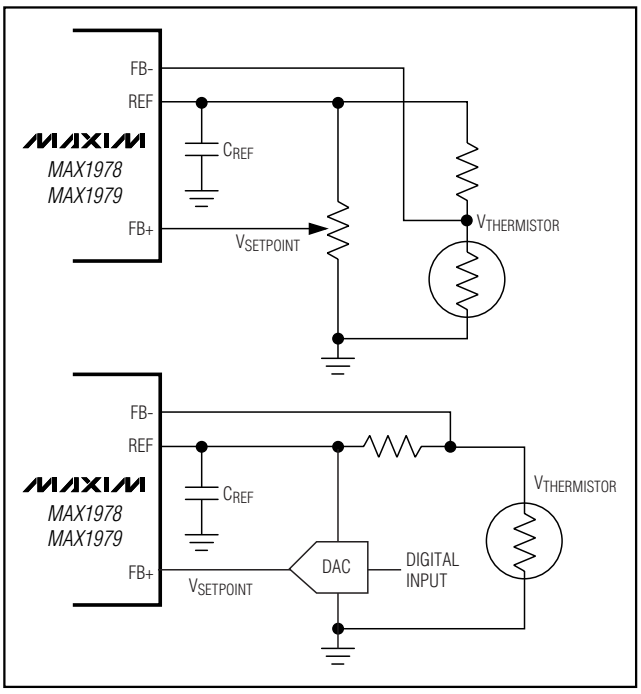


Figure 5. The Set Point can be Derived from a Potentiometer or a DAC

Control Inputs/Outputs

TEC Current Control

The voltage at CTLI directly sets the TEC current. CTLI typically is driven from the output of a temperature-control circuit C_{INTOUT}. For the purposes of the following equations, it is assumed that positive TEC current is heating.

The transfer function relating current through the TEC (I_{TEC}) and V_{CTLI} is given by:

$$I_{TEC} = (V_{CTLI} - V_{REF}) / (10 \times R_{SENSE})$$

where V_{REF} is 1.50V

and $I_{TEC} = (V_{OS1} - V_{CS}) / R_{SENSE}$

V_{CTLI} is centered around REF (1.50V). I_{TEC} is zero when V_{CTLI} = 1.50V. When V_{CTLI} > 1.50V, the MAX1978 is heating. Current flow is from OS2 to OS1. The voltages are:

$$V_{OS2} > V_{OS1} > V_{CS}$$

when V_{CTLI} < 1.50V, current flows from OS1 to OS2:

$$V_{OS2} < V_{OS1} < V_{CS}$$

Shutdown Control

Drive $\overline{SHDN}$ low to place the MAX1978/MAX1979 in a power-saving shutdown mode. When the MAX1978/MAX1979 are in shutdown, the TEC is off (V_{OS1} and V_{OS2} decay to GND) and input supply current lowers to 2mA (typ).

ITEC Output

ITEC is a status output that provides a voltage proportional to the actual TEC current. ITEC = REF when TEC current is zero. The transfer function for the ITEC output:

$$V_{ITEC} = 1.50 + 8 \times (V_{OS1} - V_{CS})$$

Use ITEC to monitor the cooling or heating current through the TEC. The maximum capacitance that ITEC can drive is 100pF.

Applications Information

The MAX1978/MAX1979 drive a thermoelectric cooler inside a thermal-control loop. TEC drive polarity and power are regulated to maintain a stable control temperature based on temperature information read from a thermistor, or from other temperature-measuring devices. Carefully selected external components can achieve 0.001°C temperature stability. The MAX1978/MAX1979 provide precision amplifiers and an integrator amplifier to implement the thermal-control loop (Figures 1 and 2).

Connecting and Compensating the Thermal-Control Loop

Typically, the thermal loop consists of an error amplifier and proportional integral derivative controller (PID) (Figure 4). The thermal response of the TEC module must be understood before compensating the thermal loop. In particular, TECs generally have stronger heating capacity than cooling capacity because of the effects of waste heat. Consider this point when analyzing the TEC response.

Analysis of the TEC using a signal analyzer can ease compensation calculations. Most TECs can be crudely modeled as a two-pole system. The second pole potentially creates an oscillatory condition because of the associated 180° phase shift. A dominant pole compensation scheme is not practical because the crossover frequency (the point of the Bode plot where the gain is zero dB) must be below the TEC's first pole, often as low as 0.02Hz. This requires an excessively large integrator capacitor and results in slow loop-transient response. A better approach is to use a PID controller, where two additional zeros are used to cancel the TEC and integrator poles. Adequate phase margin can be achieved near the frequency of the TEC's second pole when using a PID controller. The following is an example of the compensation procedure using a PID controller.

Figure 6 details a two-pole transfer function of a typical TEC module. This Bode plot can be generated with a signal analyzer driving the CTLI input of the MAX1978/MAX1979, while plotting the thermistor voltage from the module. For the example module, the two poles are at 0.02Hz and 1Hz.

The first step in compensating the control loop involves selecting components R3 and C2 for highest DC gain. Film capacitors provide the lowest leakage but can be large. Ceramic capacitors are a good compromise between low leakage and small size. Tantalum and electrolytic capacitors have the highest leakage and generally are not suitable for this application. The integrating capacitor, C2, and R3 (Figure 4) set the first zero (fz1). The specific application dictates where the first zero should be set. Choosing a very low frequency results in a very large value capacitor. Set the first zero frequency to no more than 8 times the frequency of the lowest TEC pole. Setting the frequency more than 8 times the lowest pole results in the phase falling below -135° and may cause instability in the system. For this example, C2 = 10µF. Resistor R3 then sets the zero at 0.16Hz using the following equation:

$$fz1 = \frac{1}{2\pi \times C2 \times R3}$$

This yields a value of R3 = 99.47kΩ. For our example, use 100kΩ.

Next, adjust the gain for a crossover frequency for maximum phase margin near the TEC's second pole. From Figure 6, the TEC bode plot, approximately 30dB of gain is needed to move the 0dB crossover point up to 1.5Hz. The error amplifier provides a fixed gain of 50, or approximately 34dB. Therefore, the integrator needs to provide -4dB of gain at 1.5Hz. C1 and R3 set the gain at the crossover frequency.

$$C1 = \frac{A}{\frac{1}{C2} + 2\pi \times R3 \times f_C}$$

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where:

A = The gain needed to move the 0dB crossover point up to the desired frequency. In this case, A = -4dB = 0.6.

f_C = The desired crossover frequency, 1.5Hz in this example.

C1 is found to be 0.58µF; use 0.47µF.

Next, the second TEC pole must be cancelled by adding a zero. Canceling the second TEC pole provides maximum phase margin by adding positive phase to the circuit. Setting a second zero (fz2) to at least 1/5 the crossover frequency (1.5Hz/5 = 0.3Hz), and a pole (fp1) to 5 times the crossover frequency or higher (5 × 1.5Hz = 7.5Hz) ensures good phase margin, while allowing for variation in the location of the TEC's second pole. Set the zero fz2 to 0.3Hz and calculate R2:

$$fz2 = \frac{1}{2\pi \times C1 \times R2}$$

where fz2 is the second zero.

R2 is calculated to be 1.1MΩ; use 1MΩ.

Now pole fp1 is added at least 5 times the crossover frequency to terminate zero fz2.

Choose fp1 = 15Hz, find R1 using the following equation:

$$fp1 = \frac{1}{2\pi \times C1 \times R1}$$

Resistor R1 is found to be 22kΩ, use 20kΩ

The final step is to terminate the first zero by setting the rolloff frequency with a second pole, fp2. A good choice is 2 times fp1.

Choose fp2 = 30Hz, find C3 using the following equation:

$$fp2 = \frac{1}{2\pi \times C3 \times R3}$$

where C3 is found to be 0.05µF, use 0.047µF.

Figure 7 displays the compensated gain and phase plots for the above example.

The example given is a good place to start when compensating the thermal loop. Different TEC modules require individual testing to find their optimal compensation scheme. Other compensation schemes can be used. The above procedure should provide good results for the majority of optical modules.

Chip Information

TRANSISTOR COUNT: 6023

PROCESS: BiCMOS

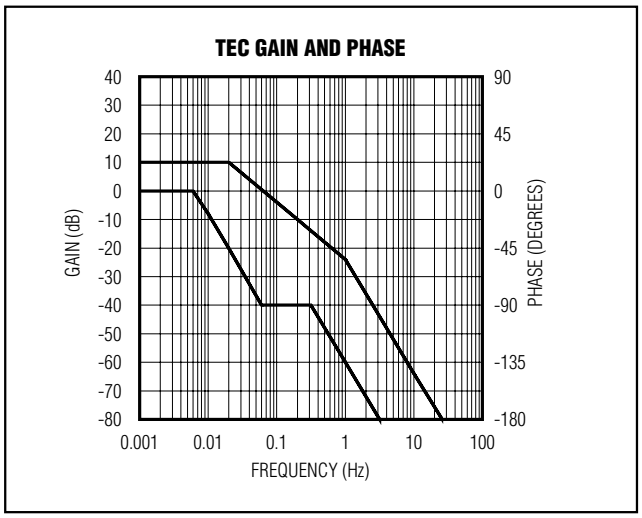


Figure 6. Bode Plot of a Generic TEC Module

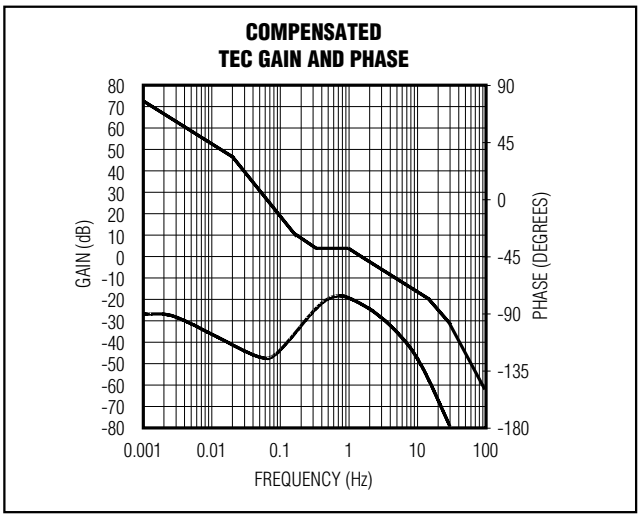
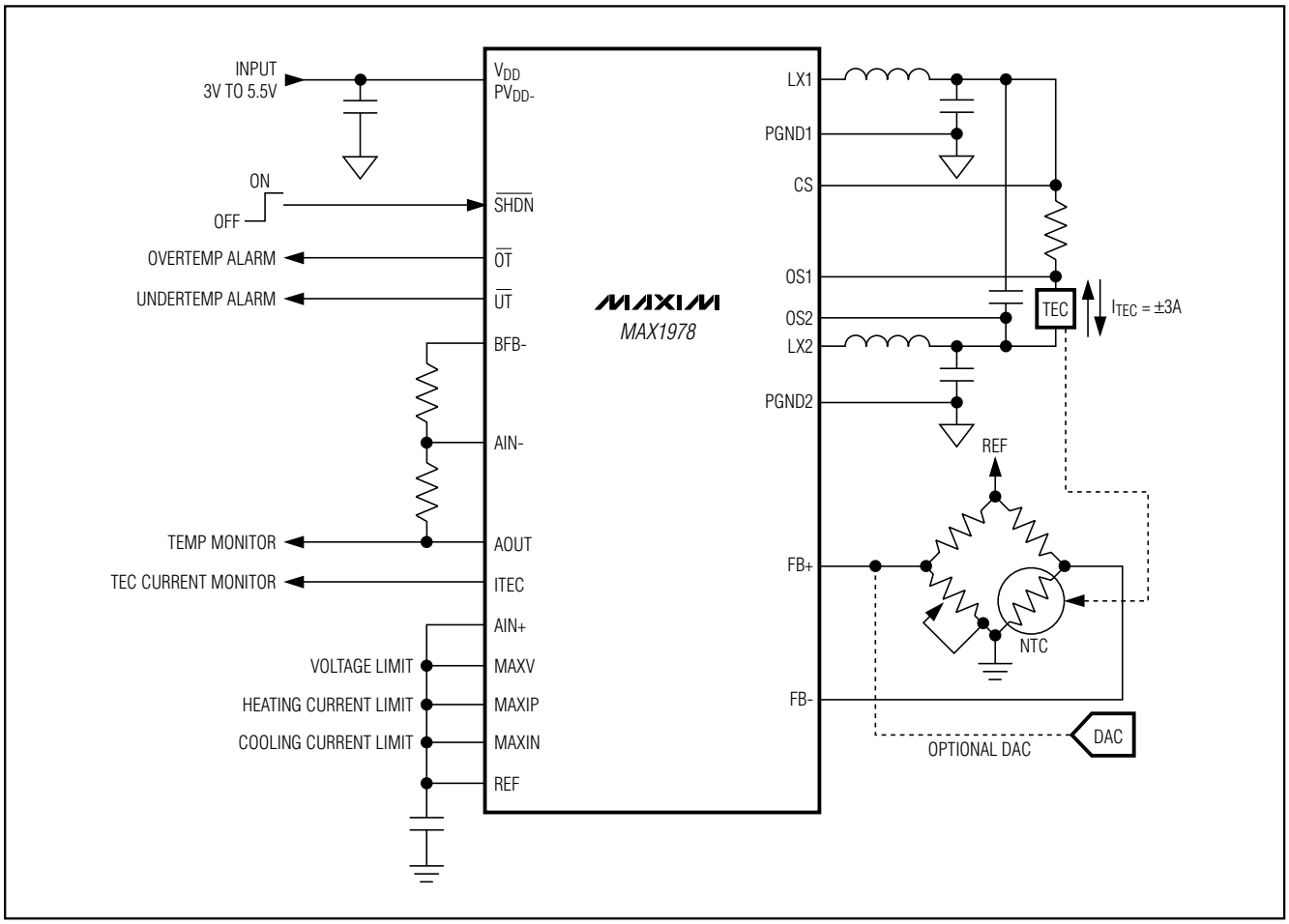


Figure 7. Compensated Thermal-Control Loop Using the TEC Module in Figure 6

Typical Operating Circuit

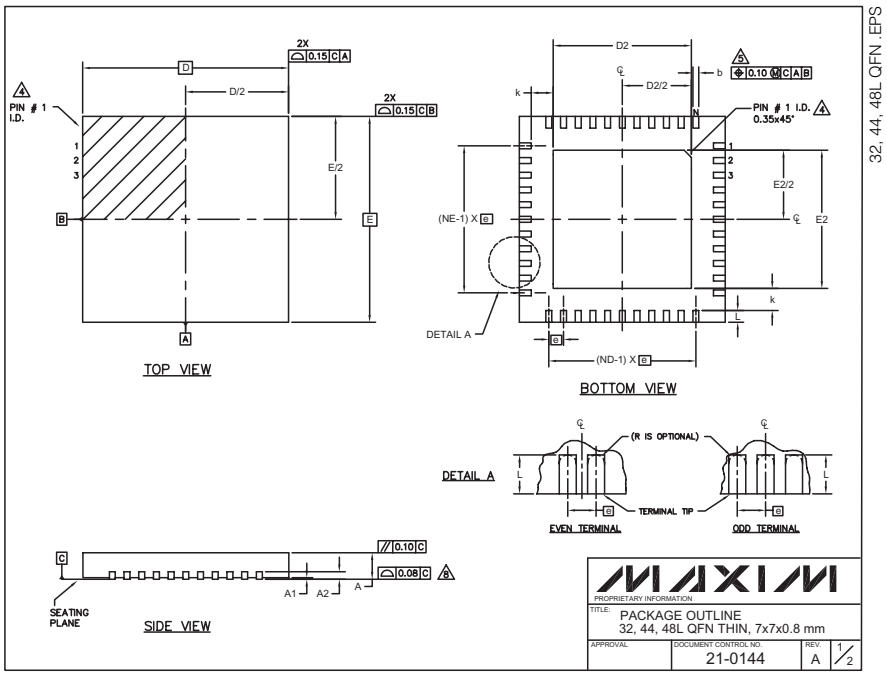


Integrated Temperature Controllers for Peltier Modules

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN .EPS



COMMON DIMENSIONS												
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.75	5.45	5.60	5.75	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0144
REV. A
2/2

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- *Подбор аналогов.*
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- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
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- *Техническую поддержку проекта.*
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