1 MHz to 8 GHz, 70 dB Logarithmic Detector/Controller

AD8318

FEATURES

Wide bandwidth: 1 MHz to 8 GHz
High accuracy: ±1.0 dB over 55 dB range (f < 5.8 GHz)
Stability over temperature: ±0.5 dB
Low noise measurement/controller output (VOUT)
Pulse response time: 10 ns/12 ns (fall/rise)
Integrated temperature sensor
Small footprint LFCSP
Power-down feature: <1.5 mW at 5 V
Single-supply operation: 5 V @ 68 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
RSSI measurement in base stations, WLAN, WiMAX, and radars

GENERAL DESCRIPTION

The AD8318 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output voltage. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device is used in measurement or controller mode. The AD8318 maintains accurate log conformance for signals of 1 MHz to 6 GHz and provides useful operation to 8 GHz. The input range is typically 60 dB (re: 50 Ω) with error less than ±1 dB. The AD8318 has a 10 ns response time that enables RF burst detection to beyond 45 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A 2 mV/°C slope temperature sensor output is also provided for additional system monitoring. A single supply of 5 V is required. Current consumption is typically 68 mA. Power consumption decreases to <1.5 mW when the device is disabled.

The AD8318 can be configured to provide a control voltage to a VGA, such as a power amplifier or a measurement output, from Pin VOUT. Because the output can be used for controller applications, wideband noise is minimal.

FUNCTIONAL BLOCK DIAGRAM

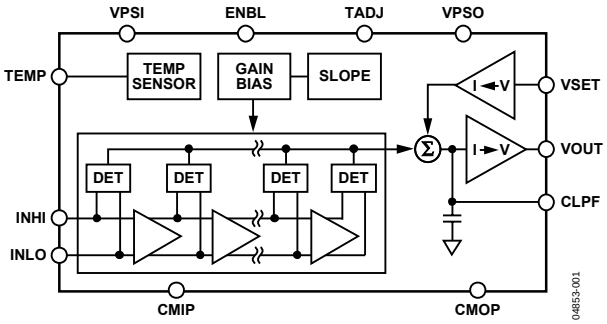


Figure 1.

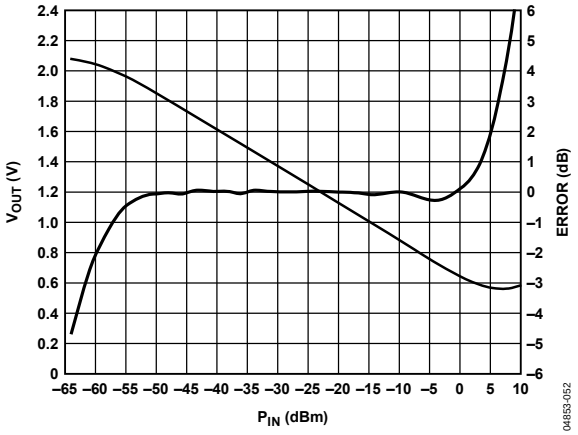


Figure 2. Typical Logarithmic Response and Error vs. Input Amplitude at 5.8 GHz

In this mode, the setpoint control voltage is applied to VSET. The feedback loop through an RF amplifier is closed via VOUT, the output of which regulates the amplifier output to a magnitude corresponding to VSET. The AD8318 provides 0 V to 4.9 V output capability at the VOUT pin, suitable for controller applications. As a measurement device, Pin VOUT is externally connected to VSET to produce an output voltage, V_{OUT}, which is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is nominally −25 mV/dB but can be adjusted by scaling the feedback voltage from VOUT to the VSET interface. The intercept is 20 dBm (re: 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8318 is fabricated on a SiGe bipolar IC process and is available in a 4 mm × 4 mm, 16-lead LFCSP for the operating temperature range of −40°C to +85°C.

Rev. B
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7/04—Rev. 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, C_{LPF} = 220 pF, T_A = 25°C, 52.3 Ω termination resistor at INHI, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHI (Pin 14) and INLO (Pin 15)				
Specified Frequency Range		0.001		8	GHz
DC Common-Mode Voltage			V_{POS} − 1.8		V
MEASUREMENT MODE	VOUT (Pin 6) shorted to VSET (Pin 7), sinusoidal input signal				
f = 900 MHz	R_{TADJ} = 500 Ω				
Input Impedance			957||0.71		Ω||pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB error		−1		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope		−26	−24.5	−23	mV/dB
Intercept		19.5	22	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.7	0.78	0.86	V
Output Voltage—Low Power In	P_{IN} = −40 dBm	1.42	1.52	1.62	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤85°C		0.0011		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.003		dB/°C
f = 1.9 GHz	R_{TADJ} = 500 Ω				
Input Impedance			523||0.68		Ω||pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
	−40°C < T_A < +85°C		50		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−59		dBm
Slope		−27	−24.4	−22	mV/dB
Intercept		17	20.4	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.83	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.35	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.0011		dB/°C
	−40°C ≤ T_A ≤ +5°C		0.0072		dB/°C
f = 2.2 GHz	R_{TADJ} = 500 Ω				
Input Impedance			391||0.66		Ω||pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
±1 dB Dynamic Range	T_A = 25°C		58		dB
	−40°C < T_A < +85°C		50		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−60		dBm
Slope		−28	−24.4	−21.5	mV/dB
Intercept		15	19.6	25	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.84	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.34	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		−0.0005		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0062		dB/°C

Parameter	Conditions	Min	Typ	Max	Unit
f = 3.6 GHz	R_{TADJ} = 51 Ω				
Input Impedance			119||0.7		Ω||pF
±3 dB Dynamic Range	T_A = 25°C		70		dB
±1 dB Dynamic Range	T_A = 25°C		58		dB
	−40°C < T_A < +85°C		42		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−60		dBm
Slope			−24.3		mV/dB
Intercept			19.8		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.717		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.46		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.0022		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.004		dB/°C
f = 5.8 GHz	R_{TADJ} = 1000 Ω				
Input Impedance			33||0.59		Ω||pF
±3 dB Dynamic Range	T_A = 25°C		70		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB error		−1		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			−24.3		mV/dB
Intercept			25		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.86		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.59		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.0033		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0069		dB/°C
f = 8.0 GHz	R_{TADJ} = 500 Ω				
±3 dB Dynamic Range	T_A = 25°C		60		dB
	−40°C < T_A < +85°C		58		dB
Maximum Input Level	±3 dB error		3		dBm
Minimum Input Level	±3 dB error		−55		dBm
Slope			−23		mV/dB
Intercept			37		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		1.06		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.78		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.028		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0085		dB/°C
OUTPUT INTERFACE	VOUT (Pin 6)				
Voltage Swing	V_{SET} = 0 V; P_{IN} = −10 dBm, no load[1]		4.9		V
	V_{SET} = 2.1 V; P_{IN} = −10 dBm, no load[1]		25		mV
Output Current Drive	V_{SET} = 1.5 V; P_{IN} = −50 dBm		60		mA
Small Signal Bandwidth	P_{IN} = −10 dBm; from CLPF to VOUT		60		MHz
Video Bandwidth (or Envelope Bandwidth)			45		MHz
Output Noise	P_{IN} = 2.2 GHz; −10 dBm, f_{NOISE} = 100 kHz, C_{LPF} = 220 pF		90		nV/√Hz
Fall Time	P_{IN} = Off to −10 dBm, 90% to 10%		10		ns
Rise Time	P_{IN} = −10 dBm to off, 10% to 90%		12		ns

Parameter	Conditions	Min	Typ	Max	Unit
VSET INTERFACE	VSET (Pin 7)				
Nominal Input Range	P_{IN} = 0 dBm; measurement mode[2]		0.5		
	P_{IN} = −65 dBm; measurement mode[2]		2.1		V
Logarithmic Scale Factor			−0.04		dB/mV
Bias Current Source	P_{IN} = −10 dBm; V_{SET} = 2.1 V		2.5		µA
TEMPERATURE REFERENCE	TEMP (Pin 13)				
Output Voltage	T_A = 25°C, R_{LOAD} = 10 kΩ	0.57	0.6	0.63	V
Temperature Slope	−40°C ≤ T_A ≤ +85°C, R_{LOAD} = 10 kΩ		2		mV/°C
Current Source/Sink	T_A = 25°C		10/0.1		mA
POWER-DOWN INTERFACE	ENBL (Pin 16)				
Logic Level to Enable Device			1.7		V
ENBL Current When Enabled	ENBL = 5 V		<1		µA
ENBL Current When Disabled	ENBL = 0 V; sourcing		15		µA
POWER INTERFACE	VPSI (Pin 3 and Pin 4), VPSO (Pin 9)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	ENBL = 5 V	50	68	82	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		150		µA/°C
Supply Current when Disabled	ENBL = 0 V, total currents for VPSI and VPSO		260		µA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		350		µA

[1] Controller mode.
[2] Gain = 1. For other gains, see the Measurement Mode section.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: Pin VPSO, Pin VPSI	5.7 V
ENBL, V_{SET} Voltage	0 to V_{POS}
Input Power (Single-Ended, re: 50 Ω)	12 dBm
Internal Power Dissipation	0.73 W
θ_{JA}[1]	55°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	260°C

[1] With package die paddle soldered to thermal pads with vias connecting to inner and bottom layers.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

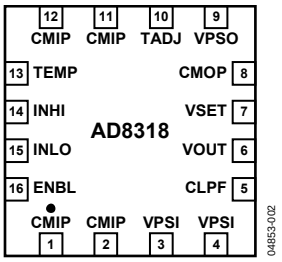


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 11, 12	CMIP	Device Common (Input System Ground).
3, 4	VPSI	Positive Supply Voltage (Input System): 4.5 V to 5.5 V. Voltage on Pin 3, Pin 4, and Pin 9 should be equal.
5	CLPF	Loop Filter Capacitor.
6	VOUT	Measurement and Controller Output.
7	VSET	Setpoint Input for Controller Mode or Feedback Input for Measurement Mode.
8	CMOP	Device Common (Output System Ground).
9	VPSO	Positive Supply Voltage (Output System): 4.5 V to 5.5 V. Voltage on Pin 3, Pin 4, and Pin 9 should be equal.
10	TADJ	Temperature Compensation Adjustment.
13	TEMP	Temperature Sensor Output.
14	INHI	RF Input. Nominal input range: −60 dBm to 0 dBm (re: 50 Ω), ac-coupled.
15	INLO	RF Common for INHI. AC-coupled RF common.
16	ENBL	Device Enable. Connect to VPSI for normal operation. Connect pin to ground for disable mode.
	Paddle	Internally Connected to CMIP (Solder to Ground).

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V; T_A = +25°C, −40°C, +85°C; C_{LPF} = 220 pF; R_{TADJ} = 500 Ω; unless otherwise noted. Colors: +25°C → Black; −40°C → Blue; +85°C → Red.

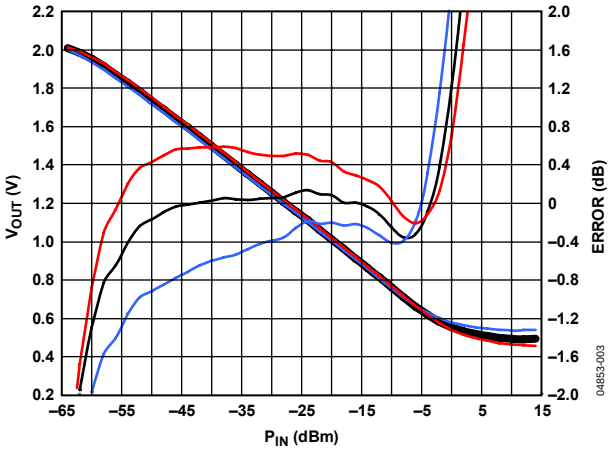


Figure 4. VOUT and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device

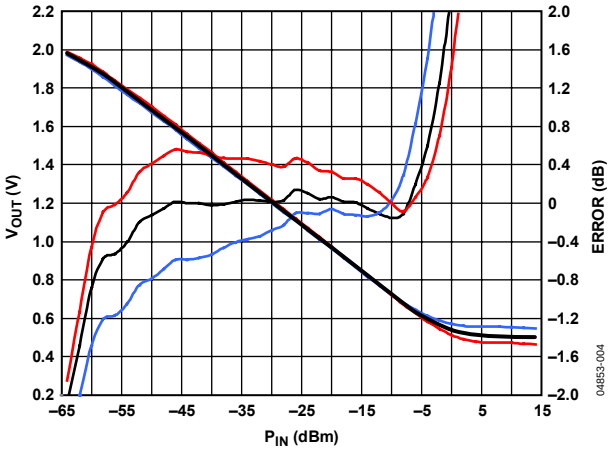


Figure 5. VOUT and Log Conformance vs. Input Amplitude at 1.9 GHz, Typical Device

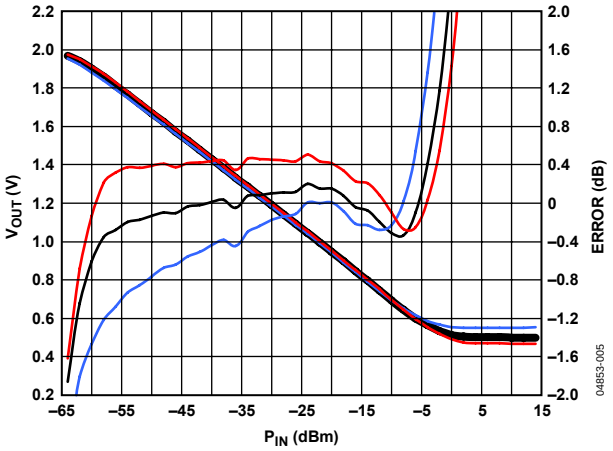


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, Typical Device

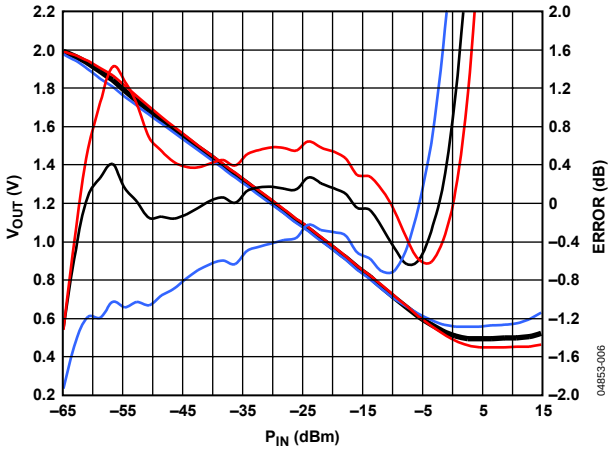


Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, Typical Device, R_{TADJ} = 51 Ω

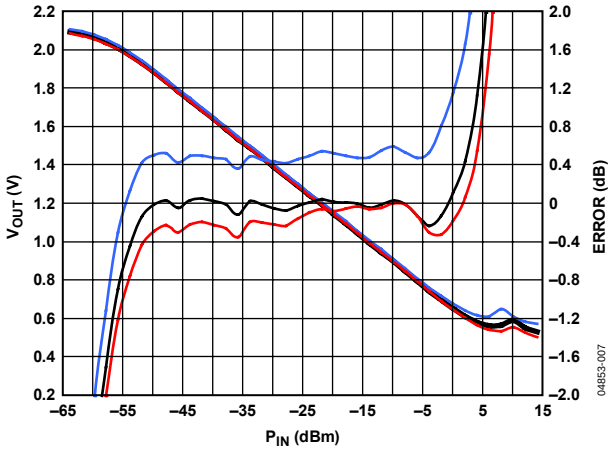


Figure 8. VOUT and Log Conformance vs. Input Amplitude at 5.8 GHz, Typical Device, R_{TADJ} = 1000 Ω

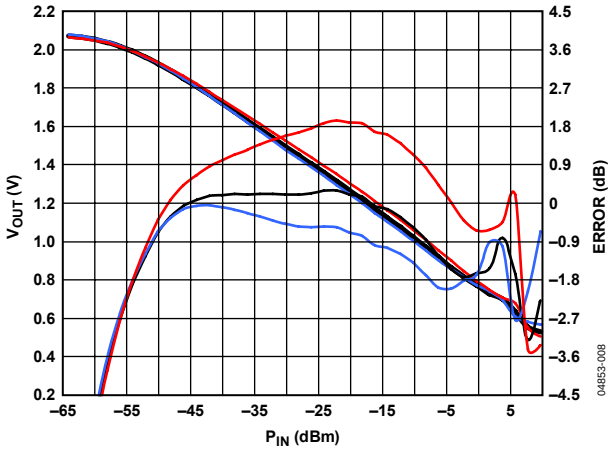


Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 8 GHz, Typical Device

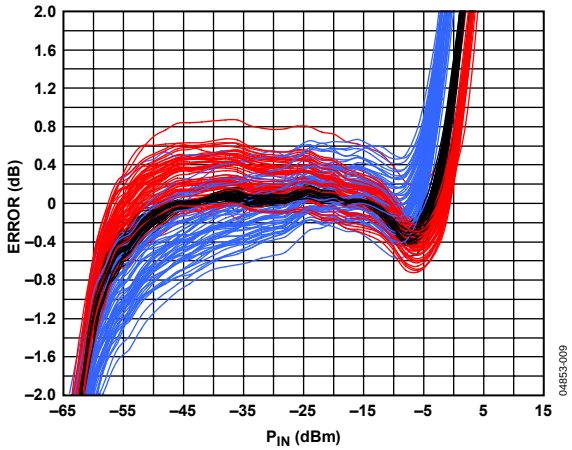


Figure 10. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude at 900 MHz for at Least 70 Devices

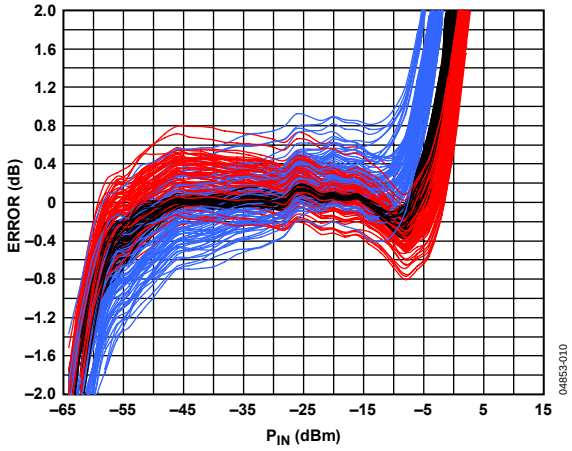


Figure 11. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 1900 MHz for at Least 70 Devices

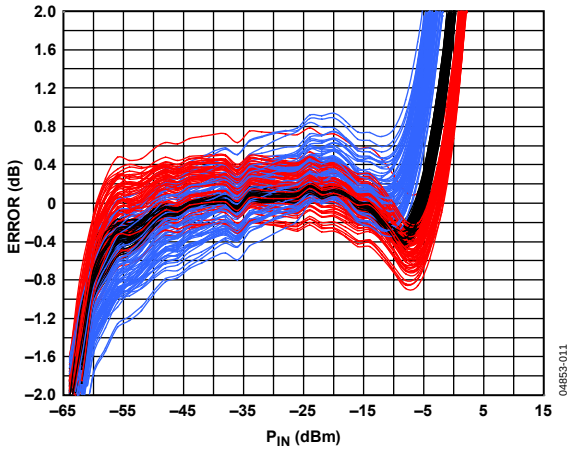


Figure 12. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 2.2 GHz for at Least 70 Devices

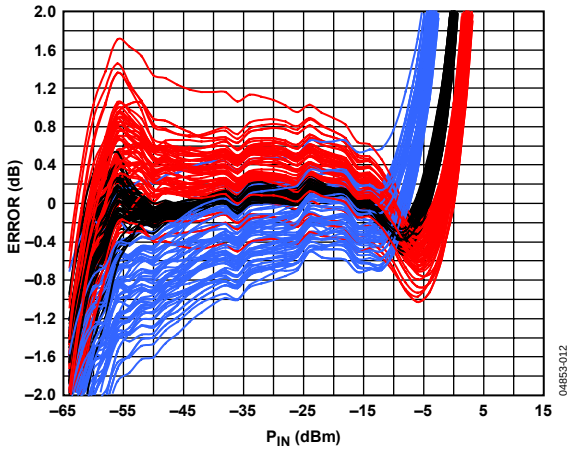


Figure 13. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 3.6 GHz for at Least 70 Devices, R_{TADJ} = 51 Ω

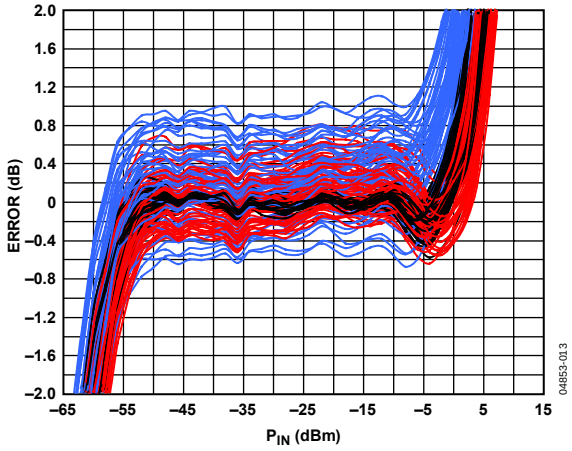


Figure 14. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 5.8 GHz for at Least 70 Devices, R_{TADJ} = 1000 Ω

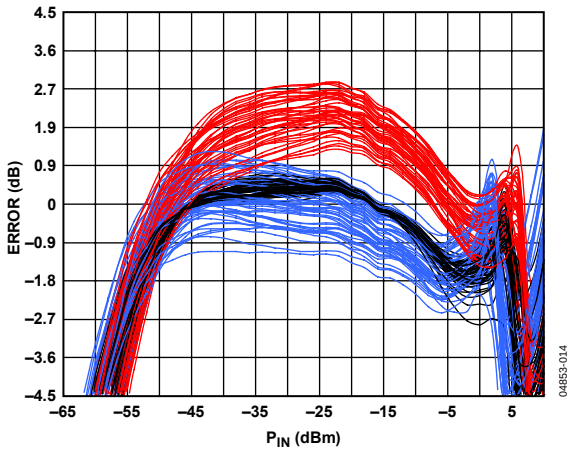


Figure 15. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 8 GHz for at Least 70 Devices

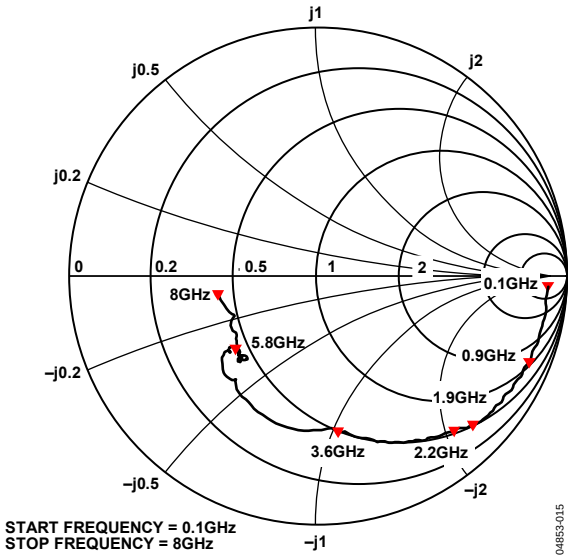


Figure 16. Input Impedance vs. Frequency; No Termination Resistor on INHI, Z_O = 50 Ω

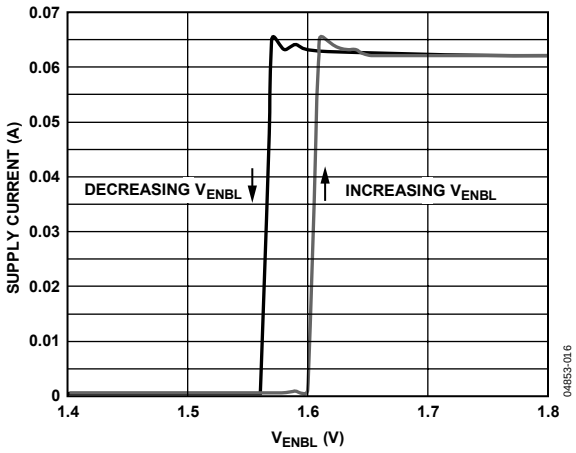


Figure 17. Supply Current vs. Enable Voltage

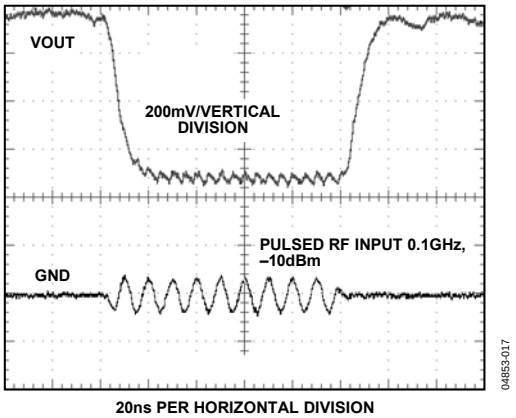


Figure 18. VOUT Pulse Response Time; Pulsed RF Input 0.1 GHz, –10 dBm; CLPF = Open

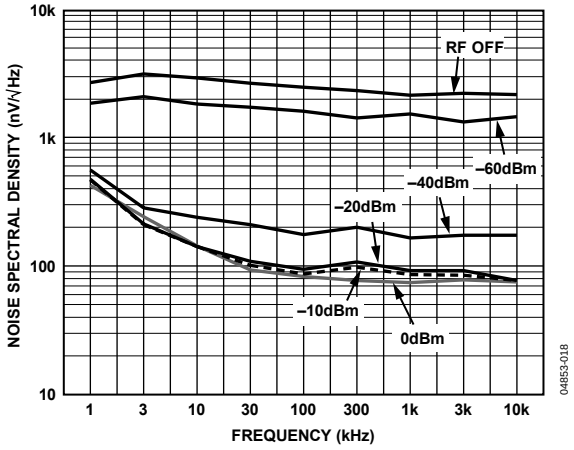


Figure 19. Noise Spectral Density of Output; CLPF = Open

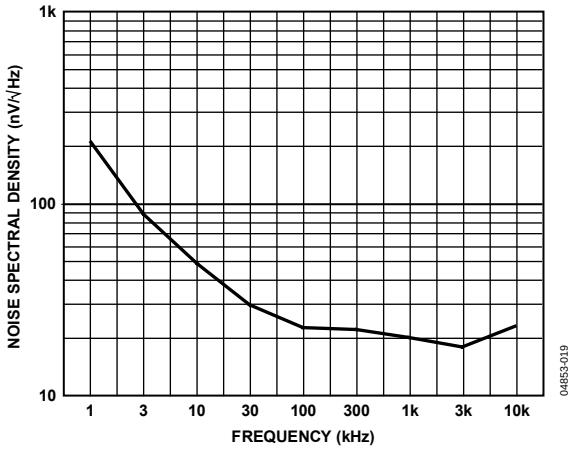


Figure 20. Noise Spectral Density of Output Buffer (from CLPF to VOUT); CLPF = 0.1 µF

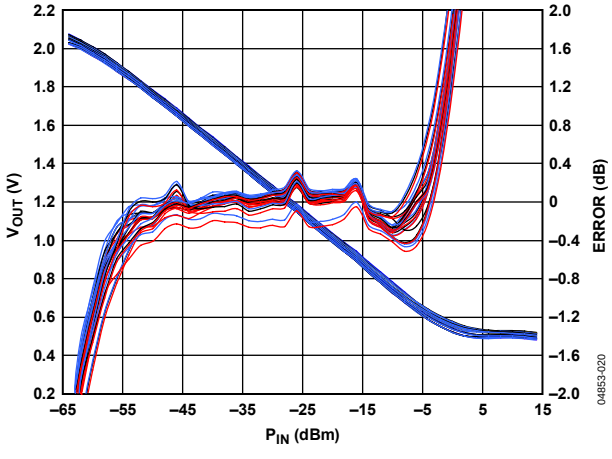


Figure 21. Output Voltage Stability vs. Supply Voltage at 1.9 GHz When VP Varies by 10%, Multiple Devices

THEORY OF OPERATION

The AD8318 is a 9-stage demodulating logarithmic amplifier that provides RF measurement and power amplifier control functions. The design of the AD8318 is similar to the AD8313 logarithmic detector/controller. However, the AD8318 input frequency range extends to 8 GHz with a 60 dB dynamic range. Other improvements include: reduced intercept variability vs. temperature, increased dynamic range at higher frequencies, low noise measurement and controller output (VOUT), adjustable low-pass corner frequency (CLPF), temperature sensor output (TEMP), negative transfer function slope for higher accuracy, and 10 ns response time for RF burst detection capability. A block diagram is shown in Figure 22.

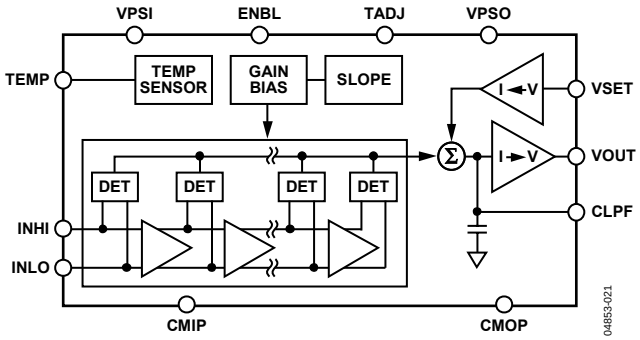


Figure 22. Block Diagram

A fully differential design, using a proprietary high speed SiGe process, extends high frequency performance. Input INHI receives the signal with a low frequency impedance of nominally 1200 Ω in parallel with 0.7 pF. The maximum input with ±1 dB log conformance error is typically 0 dBm (re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 μV rms in a 10.5 GHz bandwidth, or a noise power of −66 dBm (re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low end accuracy of the AD8318 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise.

CMIP, the input system common pin, provides a quality low impedance connection to the printed circuit board (PCB) ground via four package pins. Ground the package paddle, which is internally connected to the CMIP pin, to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by nine cascaded gain stages. For a more complete explanation of the logarithm approximation, refer to the AD8307 data sheet. The cells have a nominal voltage gain of 8.7 dB each and a 3 dB bandwidth of 10.5 GHz.

Using precision biasing, the gain is stabilized over temperature and supply variations. Because the cascaded gain stages are dc-coupled, the overall dc gain is high. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell rectifies the signal. The RF signal voltages are converted to a fluctuating differential current with an average value that increases with signal level. Along with the nine gain stages and detector cells, an additional detector is included at the input of the AD8318, altogether providing a 60 dB dynamic range. After the detector currents are summed and filtered, the function

$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (1)$$

is formed at the summing node,

where:
I_D is the internally set detector current.
V_{IN} is the input signal voltage.
$V_{INTERCEPT}$ is the intercept voltage (that is, when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V if capable of going to 0 V).

USING THE AD8318

BASIC CONNECTIONS

The AD8318 is specified for operation up to 8 GHz. As a result, low impedance supply pins with adequate isolation between functions are essential. In the AD8318, VPSI and VPSO, the two positive supply pins, must be connected to the same positive potential. The VPSI pin biases the input circuitry, while the VPSO pin biases the low noise output driver for VOUT. Separate commons are also included in the device. CMOP is used as the common for the output drivers. Pin CMIP and Pin CMOP should be connected to a low impedance ground plane.

A power supply voltage of between 4.5 V and 5.5 V should be applied to VPSO and VPSI. In addition, 100 pF and 0.1 µF power supply decoupling capacitors connect close to each power supply pin. The two adjacent VPSI pins can share a pair of decoupling capacitors due to their proximity.

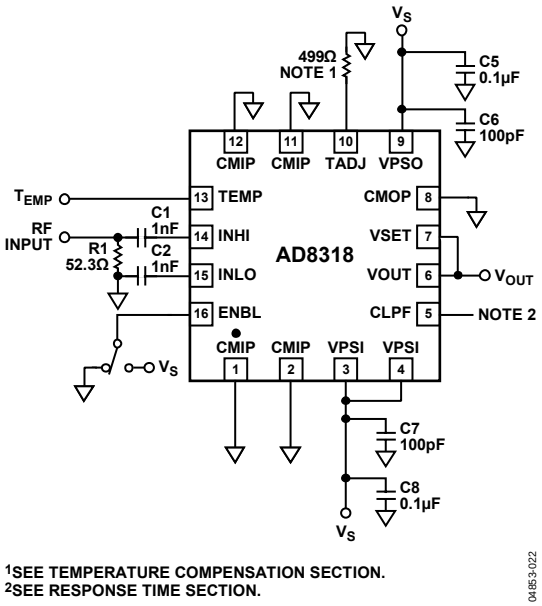


Figure 23. Basic Connections

The paddle of the AD8318 LFCSP is internally connected to CMIP. For optimum thermal and electrical performance, solder the paddle to a low impedance ground plane.

ENABLE INTERFACE

To enable the AD8318, the ENBL pin must be pulled high. Taking ENBL low puts the AD8318 in sleep mode, reducing current consumption to 260 µA at ambient. The voltage on ENBL must be greater than 2 V_{BE} (~1.7 V) to enable the device. When enabled, the ENBL pin draws less than 1 µA. When ENBL is pulled low, the pin sources 15 µA.

The enable interface has high input impedance. An internal 200 Ω resistor is placed in series with the ENBL input for added protection. Figure 24 depicts a simplified schematic of the enable interface. The response time of the AD8318 ENBL interface is shown in Figure 25.

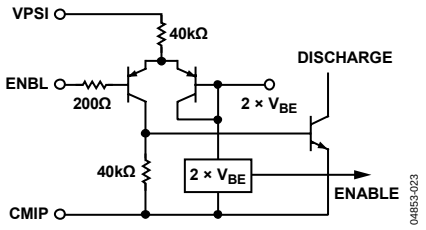


Figure 24. ENBL Interface

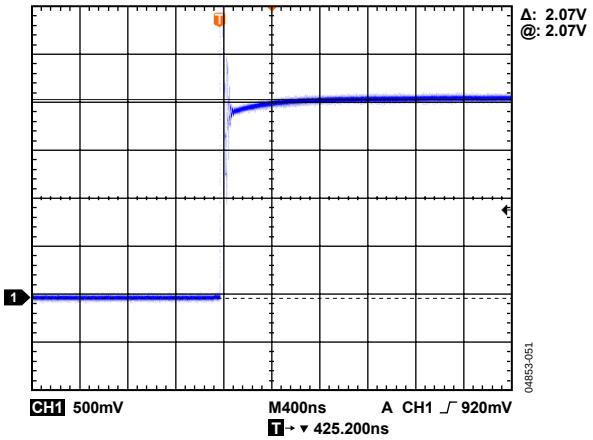


Figure 25. ENBL Response Time; VPOS = 5.0 V; Input AC-Coupling Caps = 18 pF; CLPF = Open

INPUT SIGNAL COUPLING

The RF input to the AD8318 (INHI) is single ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground (see Figure 23). Suggested coupling capacitors are 1 nF ceramic, 0402-style capacitors for input frequencies of 1 MHz to 8 GHz. The coupling capacitors should be mounted close to the INHI pin and the INLO pin. These capacitor values can be increased to lower the input stage high-pass cutoff frequency. The high-pass corner is set by the input coupling capacitors and the internal 10 pF capacitor. The dc voltage on INHI and INLO is approximately one diode voltage drop below the voltage applied to the VPSI pin.

The Smith Chart in Figure 16 shows the AD8318 input impedance vs. frequency. Table 4 lists the reflection coefficient and impedance at select frequencies. For Figure 16 and Table 4, the 52.3 Ω input termination resistor is removed. At dc, the resistance is typically 2 kΩ. At frequencies up to 1 GHz, the impedance is approximated as 1000 Ω||0.7 pF. The RF input pins are coupled to a network as shown in the simplified schematic in Figure 26.

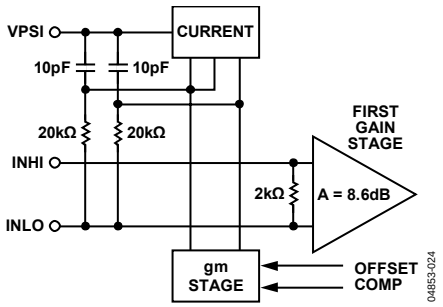


Figure 26. Input Interface

While the input can be reactively matched, this is typically not necessary. An external 52.3 Ω shunt resistor (connected on the signal side of the input coupling capacitors, see Figure 23) combines with the relatively high input impedance to provide an adequate broadband 50 Ω match.

Table 4. Input Impedance for Select Frequency

Frequency	S11		Impedance Ω
(MHz)	Real	Imaginary	(Series)
100	+0.918	−0.041	927-j491
450	+0.905	−0.183	173-j430
900	+0.834	−0.350	61-j233
1900	+0.605	−0.595	28-j117
2200	+0.524	−0.616	28-j102
3600	+0.070	−0.601	26-j49
5300	−0.369	−0.305	20-j16
5800	−0.326	−0.286	22-j16
8000	−0.390	−0.062	22-j3

The coupling time constant, $50 \times C_C/2$, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(2\pi \times 50 \times C_C)$, where $C1 = C2 = C_C$. Using the typical value of 1 nF, this high-pass corner is ~3.2 MHz. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. Likewise, in low frequency applications, a simple RC network forming a low-pass filter should be added, generally placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

OUTPUT INTERFACE

The logarithmic output interface is shown in Figure 27. The VOUT pin is driven by a PNP output stage. An internal 10 Ω resistor is placed in series with the emitter follower output and the VOUT pin. The rise time of the output is limited mainly by the slew on CLPF. The fall time is an RC limited slew provided by the load capacitance and the pull-down resistance at VOUT. There is an internal pull-down resistor of 350 Ω. Any resistive load at VOUT is placed in parallel with the internal pull-down resistor and provides additional discharge current.

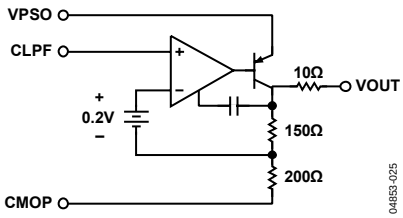


Figure 27. Output Interface

SETPOINT INTERFACE

The setpoint interface is shown in Figure 28. The VSET input drives the high impedance (250 kΩ) input of an internal operational amplifier. The VSET voltage appears across the internal 3.13 kΩ resistor to generate I_{SET}. When a portion of VOUT is applied to VSET, the feedback loop forces

$$-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET} \quad (2)$$

If $V_{SET} = V_{OUT}/X$, $I_{SET} = V_{OUT}/(X \times 3.13\ k\Omega)$. The result is $V_{OUT} = (-I_D \times 3.13\ k\Omega \times X) \times \log_{10}(V_{IN}/V_{INTERCEPT})$.

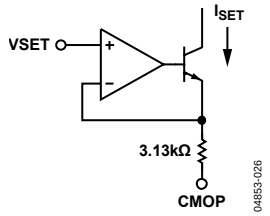


Figure 28. VSET Interface

The slope is given by $-I_D \times X \times 3.13\ k\Omega = -500\ mV \times X$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, X = 2. The slope is set to −1 V/decade or −50 mV/dB.

TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE

The AD8318 functionality includes the capability to externally trim the temperature drift. Attaching a ground-referenced resistor to the TADJ pin alters an internal current, minimizing intercept drift vs. temperature. As a result, the R_{TADJ} can be optimized for operation at different frequencies.

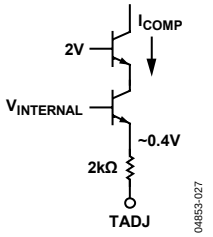


Figure 29. TADJ Interface

R_{TADJ}, nominally 499 Ω for optimal temperature compensation at 2.2 GHz input frequency, is connected between the TADJ pin and ground (see Figure 23). The value of this resistor partially determines the magnitude of an analog correction coefficient that is employed to reduce intercept drift.

Table 5 lists recommended resistors for various frequencies. These resistors provide the best overall temperature drift based on measurements of a diverse population of devices.

The relationship between output temperature drift and frequency is nonlinear and is not easily modeled. Experimentation is required to choose the correct R_{TADJ} resistor at frequencies not listed in Table 5.

Table 5. Recommended R_{TADJ} Resistors

Frequency	Recommended R_{TADJ}
900 MHz	500 Ω
1.9 MHz	500 Ω
2.2 GHz	500 Ω
3.6 GHz	51 Ω
5.8 GHz	1 kΩ
8 GHz	500 Ω

TEMPERATURE SENSOR

The AD8318 internally generates a voltage that is proportional to absolute-temperature (V_{PTAT}). The V_{PTAT} voltage is multiplied by a factor of 5, resulting in a 2 mV/°C output at the TEMP pin. The output voltage at 27°C is typically 600 mV. An emitter follower drives the TEMP pin, as shown in Figure 30.

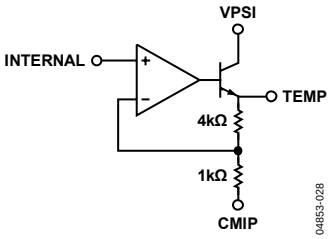


Figure 30. Temp Sensor Interface

The internal pull-down resistance is 5 kΩ. The temperature sensor has a slope of 2 mV/°C.

The temperature sensor output varies with output current due to increased die temperature. Output loads less than 1 kΩ draw enough current from the output stage causing this increase to occur. An output current of 10 mA results in the voltage on the temperature sensor to increase by 1.5°C, or ~3 mV.

Best precision from the temperature sensor is obtained when the supply current to AD8318 remains fairly constant, that is, no heavy load drive.

MEASUREMENT MODE

When the VOUT voltage, or a portion of the VOUT voltage, is fed back to VSET, the device operates in measurement mode. As shown in Figure 31, the AD8318 has an offset voltage, a negative slope, and a VOUT measurement intercept greater than its input signal range.

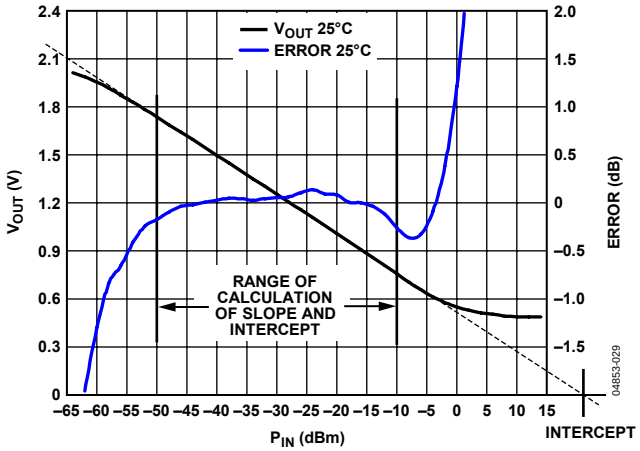


Figure 31. Typical Output Voltage vs. Input Signal

The output voltage vs. input signal voltage of the AD8318 is linear-in-dB over a multidecade range. The equation for this function is

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (3)$$

$$= X \times V_{SLOPE/dB} \times 20 \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (4)$$

where:
X is the feedback factor in $V_{SET} = V_{OUT}/X$.
$V_{INTERCEPT}$ is expressed in V_{rms}.
$V_{SLOPE/DEC}$ is nominally −500 mV/decade and $V_{SLOPE/dB}$ is nominally −25 mV/dB.
$V_{INTERCEPT}$, expressed in dBV, is the x-axis intercept of the linear-in-dB transfer function shown in Figure 31.
$V_{INTERCEPT}$ is 7 dBV (20 dBm, re: 50 Ω or 2.239 V_{rms}) for a sinusoidal input signal.

The slope of the transfer function can be increased to accommodate various converter mV per dB (LSB per dB) requirements. However, increasing the slope can reduce the dynamic range. This is due to the limitation of the minimum and maximum output voltages, determined by the chosen scaling factor X.

The minimum value for V_{OUT} is $X \times V_{OFFSET}$. The offset voltage, V_{OFFSET}, is equal to 0.5 V and is internally added to the detector output signal.

$$V_{OUT(MIN)} = (X \times V_{OFFSET}) \quad (5)$$

The maximum output voltage is 2.1 V × X, and cannot exceed 400 mV below the positive supply.

$$V_{OUT(MAX)} = (2.1\ V \times X) \text{ when } X < (V_{POS} - 400\ mV)/(2.1\ V) \quad (6)$$

$$V_{OUT(MAX)} = (V_{POS} - 400\ mV) \text{ when } X \geq (V_{POS} - 400\ mV)/(2.1\ V) \quad (7)$$

When X = 1, the typical output voltage swing is 0.5 V to 2.1 V. The output voltage swing is modeled using Equation 5 to Equation 7 and restricted by Equation 8:

$$V_{OUT(MIN)} < V_{OUT} < V_{OUT(MAX)} \quad (8)$$

When X = 4 and V_{POS} = 5 V,

$$(X \times V_{OFFSET}) < V_{OUT} < (V_{POS} - 400\ mV)$$

$$(4 \times 0.5\ V) < V_{OUT} < (2.1\ V \times 4)$$

$$2\ V < V_{OUT} < 4.6\ V$$

For X = 4, slope = −100 mV/dB; V_{OUT} can swing 2.6 V, and the usable dynamic range is reduced to 26 dB from 0 dBm to −26 dBm.

The slope is very stable vs. process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the output voltage per decade of input power. One decade is equal to 20 dB; $V_{SLOPE/DEC}/20 = V_{SLOPE/dB}$ represents the output voltage slope in V/dB.

As noted in Equation 3, the V_{OUT} voltage has a negative slope. This is the correct slope polarity to control the gain of many power amplifiers and other VGAs in a negative feedback configuration. Because both the slope and intercept vary slightly with frequency, refer to Table 1 for application-specific values for the slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_0, must be known to convert voltages to corresponding power levels. Beginning with the definitions of dBm and dBV,

$$P\ (dBm) = 10 \times \log_{10}(V_{rms}^2/(Z_0 \times 1\ mW)) \quad (9)$$

$$V\ (dBV) = 20 \times \log_{10}(V_{rms}/1\ V_{rms}) \quad (10)$$

When Equation 9 is expanded

$$P\ (dBm) = 20 \times \log_{10}(V_{rms}) - 10 \times \log_{10}(Z_0 \times 1\ mW) \quad (11)$$

and given Equation 10, Equation 11 can be rewritten as

$$P\ (dBm) = V\ (dBV) - 10 \times \log_{10}(Z_0 \times 1\ mW) \quad (12)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal, expressed in terms of dBm (decibels referred to 1 mW), in a 50 Ω system is

$$P_{INTERCEPT}\ (dBm) = V_{INTERCEPT}\ (dBV) - 10 \times \log_{10}(Z_0 \times 1\ mW) = 7\ dBV - 10 \times \log_{10}(50 \times 10^{-3}) = 20\ dBm \quad (13)$$

For further information on the intercept variation dependence upon waveform, refer to the AD8313 and AD8307 data sheets.

DEVICE CALIBRATION AND ERROR CALCULATION

The measured transfer function of the AD8318 at 2.2 GHz is shown in Figure 32. The figure shows plots of both output voltage vs. input power and calculated log conformance error vs. input power.

As the input power varies from −65 dBm to 0 dBm, the output voltage varies from 2 V to about 0.5 V.

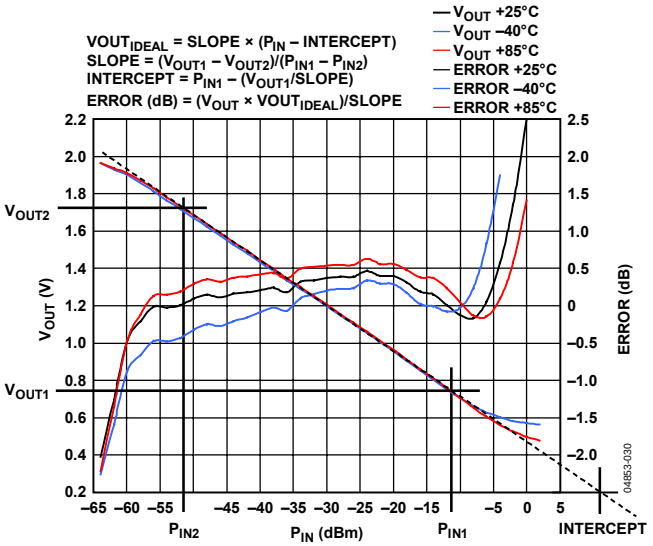


Figure 32. Transfer Function at 2.2 GHz

Because the slope and intercept vary from device to device, board-level calibration is performed to achieve high accuracy.

The equation can be rewritten for output voltage, from the Measurement Mode section, using an intercept expressed in dBm.

$$V_{OUT} = Slope \times (P_{IN} - Intercept) \quad (14)$$

In general, the calibration is performed by applying two known signal levels to the AD8318 input and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear-in-dB operating range of the device (see Figure 32). Calculation of the slope and intercept is done by:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2}) \quad (15)$$

$$Intercept = P_{IN1} - V_{OUT1}/Slope \quad (16)$$

Once the slope and intercept are calculated, an equation can be written to allow calculation of an (unknown) input power based on the output voltage of the detector.

$$P_{IN}(unknown) = V_{OUT}(measured)/Slope + Intercept \quad (17)$$

Using the equation for the ideal output voltage (see Equation 13) as a reference, the log conformance error of the measured data can be calculated as

$$Error\ (\text{dB}) = (V_{OUT(MEASURED)} - V_{OUT(IDEAL)})/Slope \quad (18)$$

Figure 32 includes a plot of the error at 25°C, the temperature at which the log amp is calibrated. Note that the error is not zero. This is because the log amp does not perfectly follow the ideal V_{OUT} vs. P_{IN} equation, even within its operating region. The error at the calibration points (−12 dBm and −52 dBm, in this case) is, however, equal to 0 by definition.

Figure 32 includes error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the slope and intercept at 25°C. This method is consistent with a mass-production environment where calibration at temperature is not practical.

SELECTING CALIBRATION POINTS TO IMPROVE ACCURACY OVER A REDUCED RANGE

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at, or close to, full power.

Figure 33 shows the same measured data as Figure 32. Note that accuracy is very high from −10 dBm to −30 dBm. Below −30 dBm, the error increases to about −1 dB. This is because the calibration points have changed to −14 dBm and −26 dBm.

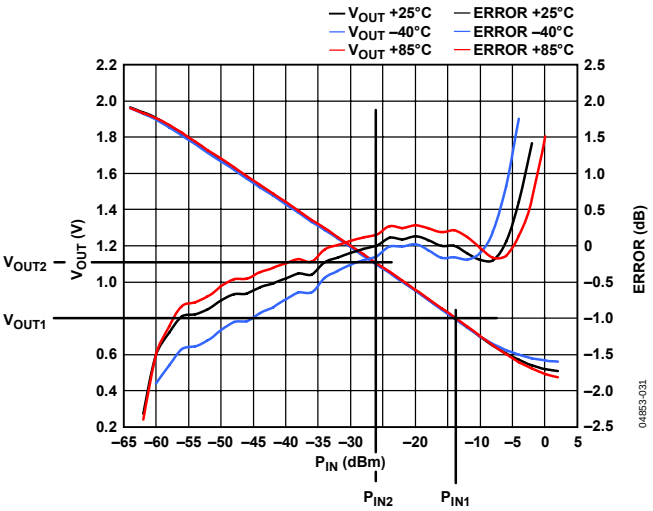


Figure 33. Output Voltage and Error vs. P_{IN} with 2-Point Calibration at −10 dBm and −30 dBm

Calibration points are chosen to suit the application at hand. In general, the calibration points are never chosen in the nonlinear portion of the transfer function of the log amp (above −5 dBm or below −60 dBm, in this case).

Figure 34 shows how calibration points can be adjusted to increase dynamic range but at the expense of linearity. In this case, the calibration points for slope and intercept are set at −4 dBm and −60 dBm. These points are at the end of the linear range of the device.

Once again, at 25°C, an error of 0 dB is seen at the calibration points. Note also that the range over which the AD8318 maintains an error of < ±1 dB is extended to 60 dB at 25°C and 58 dB over temperature. The disadvantage of this approach is that linearity suffers, especially at the top end of the input range.

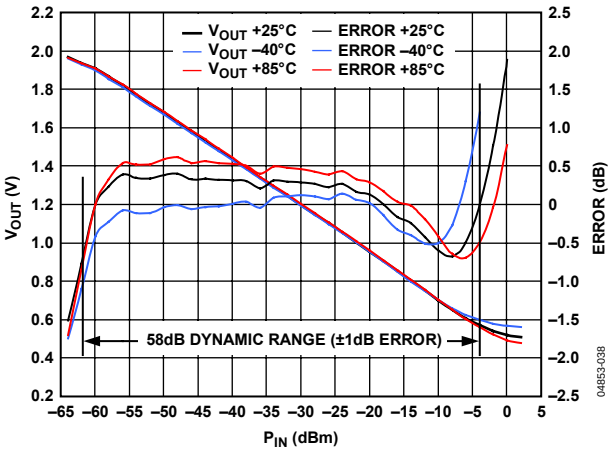


Figure 34. Dynamic Range Extension by Choosing Calibration Points Close to the End of the Linear Range

Another way of presenting the error function of a log amp detector is shown in Figure 35. In this case, the dB error at hot and cold temperatures is calculated with respect to the output voltage at ambient. This is a key difference in comparison to the plots in Figure 33 and Figure 34. Previously, all errors were calculated with respect to the ideal transfer function at ambient.

When this alternative technique is used, the error at ambient becomes, by definition, equal to 0 (see Figure 35). This is valid if the device transfer function perfectly follows the ideal $V_{OUT} = Slope \times (P_{IN} - Intercept)$ equation. However, because a log amp in practice never perfectly follows this equation (especially outside of its linear operating range), this plot tends to artificially improve linearity and extend the dynamic range. This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) output voltage at ambient. However, to achieve this level of accuracy in an end application requires calibration at multiple points in the operating range of the device.

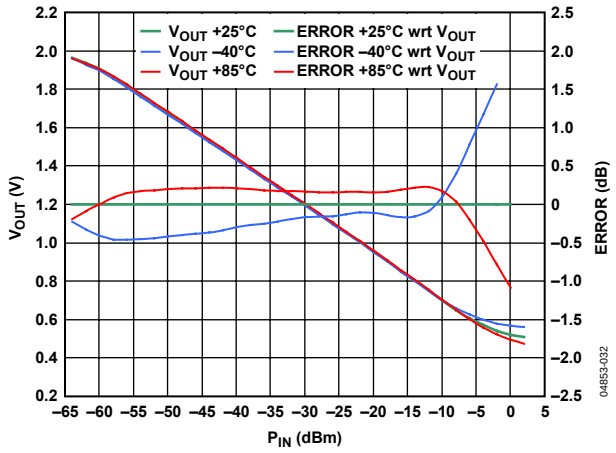


Figure 35. Error vs. Temperature with Respect to Output Voltage at 25°C (Does Not Take Transfer Function Nonlinearities at 25°C into Account)

VARIATION IN TEMPERATURE DRIFT FROM DEVICE TO DEVICE

Figure 36 shows a plot of output voltage and error for multiple AD8318 devices measured at 5.8 GHz. The concentration of black error plots represents the performance of the population at 25°C (slope and intercept are calculated for each device). The red and blue curves indicate the measured behavior of a population of devices over temperature. This suggests a range on the drift (from device to device) of 1.2 dB.

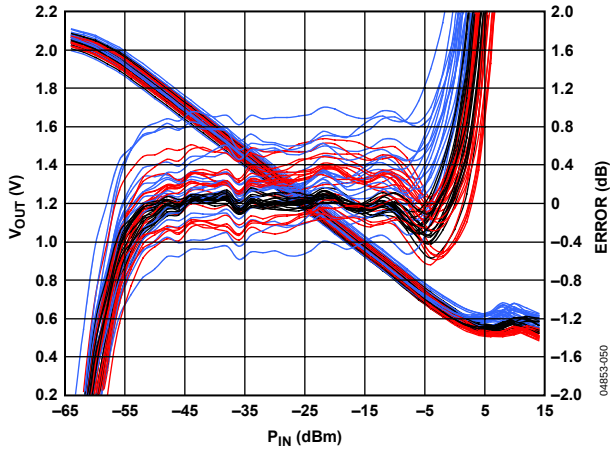


Figure 36. Output Voltage and Error vs. Temperature (+25°C, –40°C, and +85°C) of a Population of Devices Measured at 5.8 GHz

TEMPERATURE DRIFT AT DIFFERENT TEMPERATURES

Figure 37 shows the log slope and error over temperature for a 5.8 GHz input signal. Error due to drift over temperature consistently remains within ±0.5 dB, and only begins to exceed this limit when the ambient temperature drops below –20°C. When using a reduced temperature range, higher measurement accuracy is achievable for all frequencies.

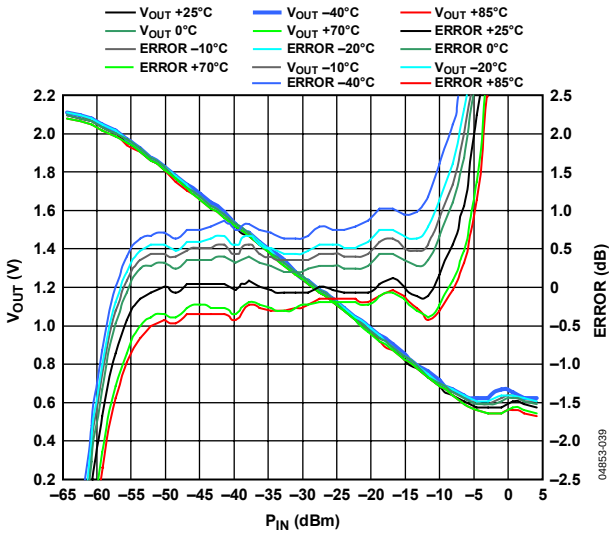


Figure 37. Typical Drift at 5.8 GHz for Various Temperatures

SETTING THE OUTPUT SLOPE IN MEASUREMENT MODE

To operate in measurement mode, VOUT is connected to VSET. This yields the typical logarithmic slope of –25 mV/dB. The output swing corresponding to the specified input range is then approximately 0.5 V to 2.1 V. The slope and output swing can be increased by placing a resistor divider between VOUT and VSET (that is, one resistor from VOUT to VSET and one resistor from VSET to common).

As an example, if two equal resistors, such as 10 kΩ/10 kΩ, are used, the slope doubles to approximately –50 mV/dB. The input impedance of VSET is approximately 500 kΩ. Slope setting resistors should be kept below ~50 kΩ to prevent this input impedance from affecting the resulting slope. When increasing the slope, the new output voltage range cannot exceed the output voltage swing capability of the output stage. Refer to the Measurement Mode section for further details.

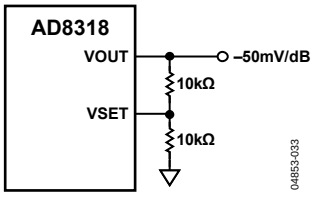


Figure 38. Increasing the Slope

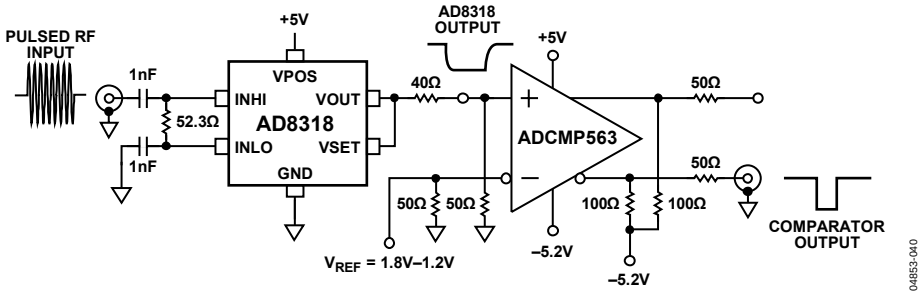


Figure 39. AD8318 Operating with the High Speed ADCMP563 Comparator

RESPONSE TIME CAPABILITY

The AD8318 has a 10 ns rise/fall time capability (10% to 90%) for input power switching between the noise floor and 0 dBm. This capability enables RF burst measurements at repetition rates beyond 45 MHz. In most measurement applications, the AD8318 has an external capacitor connected to CLPF to provide additional filtering for VOUT. However, using the CLPF capacitor slows the response time as does stray capacitance on VOUT. For an application requiring maximum RF burst detection capability, the CLPF pin is left unconnected. In this case, the integration function is provided by the 1.5 pF on-chip capacitor.

There is a 10 Ω internal resistor in series with the output driver. Because of this resistor, it is necessary to add an external 40 Ω back-terminating resistor in series with the output when driving a 50 Ω load. Place the back-terminating resistor close to the VOUT pin. The AD8318 has the drive capability to drive a 50 Ω load at the end of a coaxial cable or transmission line when back terminated (see Figure 39).

The circuit diagram in Figure 39 shows the AD8318 used with a high speed comparator circuit. The 40 Ω series resistor at the output of the AD8318 combines with an internal 10 Ω to properly match to the 50 Ω input of the comparator.

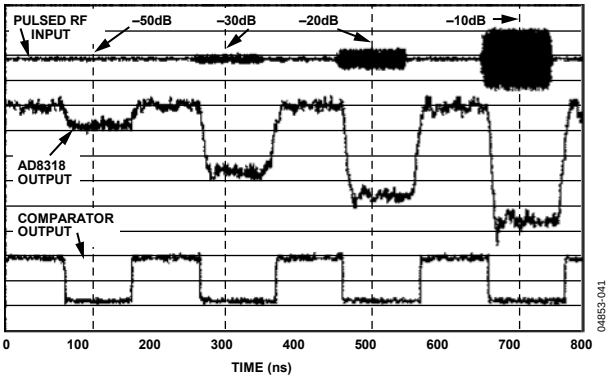


Figure 40. Pulse Response of AD8318 and Comparator for RF Pulses of Varying Amplitudes

Figure 40 shows the response of the AD8318 and the comparator for a 500 MHz pulsed sine wave of varying amplitudes. The output level of the AD8318 is the signal strength of the input signal. For applications where these RF bursts are very small, the output level does not change by a large amount. Using a comparator is beneficial in this case because it turns the output of the log amp into a limiter-like signal. While this configuration does result in the loss of received signal power level, it does allow for presence-only detection of low power RF bursts.

OUTPUT FILTERING

For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the CLPF pin be left unconnected and free of any stray capacitance.

To reduce the nominal output video bandwidth of 45 MHz, connect a ground-referenced capacitor (C_{FLT}) to the CLPF pin, as shown in Figure 41. Generally, this is done to reduce output ripple (at twice the input frequency for a symmetric input waveform, such as sinusoidal signals).

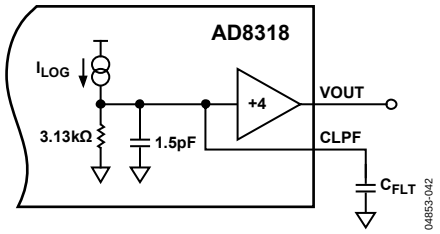


Figure 41. Lowering the Postdemodulation Bandwidth

C_{FLT} is selected by

$$C_{FLT} = \frac{1}{\left(\pi \times 3.13\ \text{k}\Omega \times VideoBandwidth\right)} - 1.5\ \text{pF} \qquad (19)$$

Set the video bandwidth to a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered.

In many log amp applications, it may be necessary to lower the corner frequency of the postdemodulation filtering to achieve low output ripple while maintaining a rapid response time to changes in signal level. For an example of a 4-pole active filter, see the AD8307 data sheet.

CONTROLLER MODE

The AD8318 provides a controller mode feature at the VOUT pin. Using V_{SET} for the setpoint voltage, it is possible for the AD8318 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs) that have output power that increases monotonically with respect to their gain control signal.

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input; VOUT is connected to the gain control terminal of the VGA, and the detector RF input is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the AD8318 adjusts the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}.

When the AD8318 operates in controller mode, there is no defined relationship between V_{SET} and V_{OUT} voltage; V_{OUT} settles to a value that results in the correct input signal level appearing at INHI/INLO.

In order for this output power control loop to be stable, a ground-referenced capacitor is connected to the CLPF pin. This capacitor, C_{FLT}, integrates the error signal (in the form of a current) to set the loop bandwidth and ensure loop stability. For further details on control loop dynamics, refer to the AD8315 data sheet.

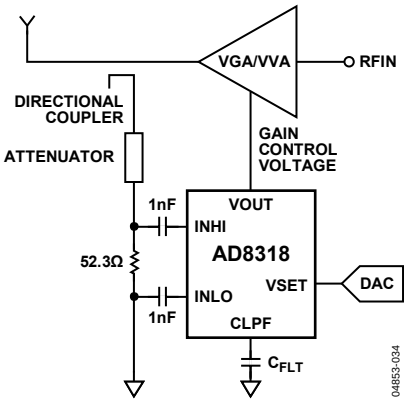


Figure 42. AD8318 Controller Mode

Decreasing V_{SET}, which corresponds to demanding a higher signal from the VGA, tends to increase V_{OUT}. The gain control voltage of the VGA must have a positive sense. A positive control voltage to the VGA increases the gain of the device.

The basic connections for operating the AD8318 as an analog controller with the AD8367 are shown in Figure 43. The AD8367 is a low frequency to 500 MHz VGA with 45 dB of dynamic range. This configuration is very similar to the one shown in Figure 42. For applications working at high input frequencies, such as cellular bands or WLAN, or those requiring large gain control ranges, the AD8318 can control the 10 MHz to 3 GHz ADL5330 RF VGA. For further details and an application schematic, refer to the ADL5330 data sheet.

The voltage applied to the GAIN pin controls the gain of the AD8367. This voltage, V_{GAIN}, is scaled linear-in-dB with a slope of 20 mV/dB and runs from 50 mV at −2.5 dB of gain up to 1.0 V at +42.5 dB.

The incoming RF signal to the AD8367 has a varying amplitude level. Receiving and demodulating it with the lowest possible error requires that the signal levels be optimized for the highest signal-to-noise ratio (SNR) feeding into the analog-to-digital converters (ADC). This is done by using an automatic gain control (AGC) loop. In Figure 43, the voltage output of the AD8318 modifies the gain of the AD8367 until the incoming RF signal produces an output voltage that is equal to the setpoint voltage V_{SET}.

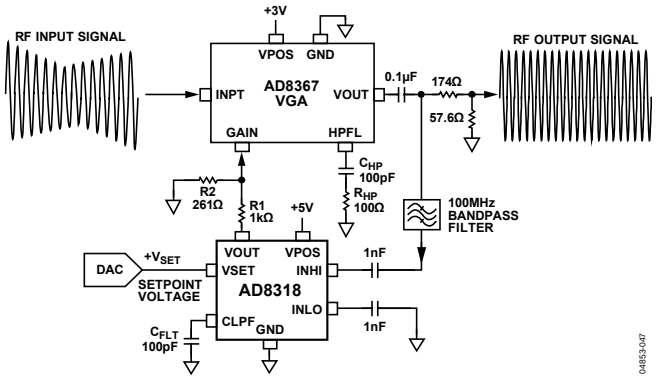


Figure 43. AD8318 Operating in Controller Mode to Provide Automatic Gain Control Functionality in Combination with the AD8367

The AGC loop is capable of controlling signals over ~45 dB dynamic range. The output of the AD8367 is designed to drive loads ≥ 200 Ω. As a result, it is not necessary to use the 53.6 Ω resistor at the input of the AD8318; the nominal input impedance of 2 kΩ is sufficient.

If the AD8367 output drives a 50 Ω load, such as an oscilloscope or spectrum analyzer, use a simple resistive divider network. The divider used in Figure 43 has an insertion loss of 11.5 dB. Figure 44 shows the transfer function of output power vs. V_{SET} voltage for a 100 MHz sine wave at −40 dBm into the AD8367.

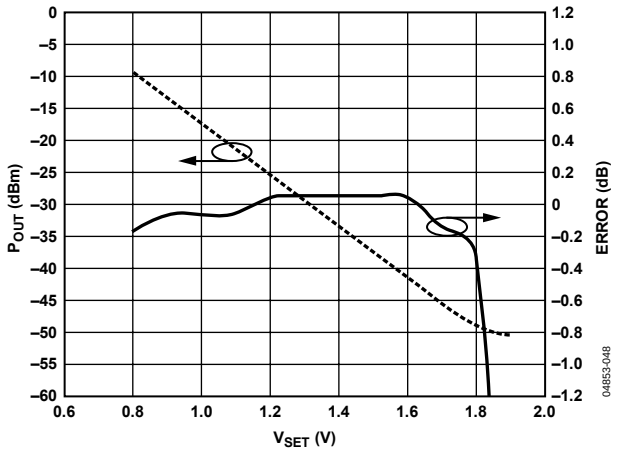


Figure 44. AD8367 Output Power vs. AD8318 Setpoint Voltage

For the AGC loop to remain locked, the AD8318 must track the envelope of the VGA output signal and provide the necessary voltage levels to the AD8367 gain control input. Figure 45 shows an oscilloscope screen image of the AGC loop depicted in Figure 43. A 50 MHz sine wave with 50% AM modulation is applied to the AD8367. The output signal from the VGA is a constant envelope sine wave with an amplitude corresponding to a setpoint voltage at the AD8318 of 1.0 V.

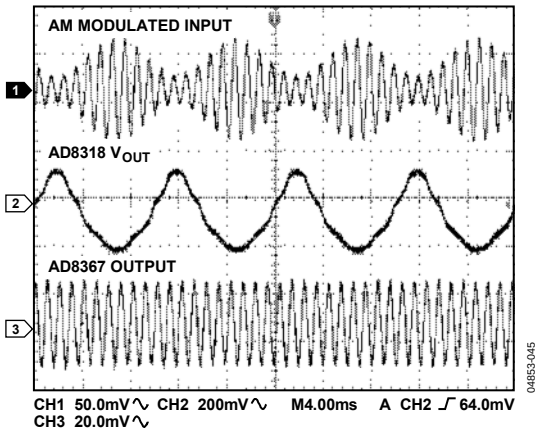


Figure 45. Oscilloscope Screen Image Showing an AM Modulated Input Signal to the AD8367. The AD8318 tracks the envelope of this input signal and applies the appropriate voltage to ensure a constant output from the AD8367.

The 45 dB control range is constant for the range of V_{SET} voltages. The input power levels to the AD8367 must be optimized to achieve this range. In Figure 46, the minimum and maximum input power levels are shown vs. setpoint voltage.

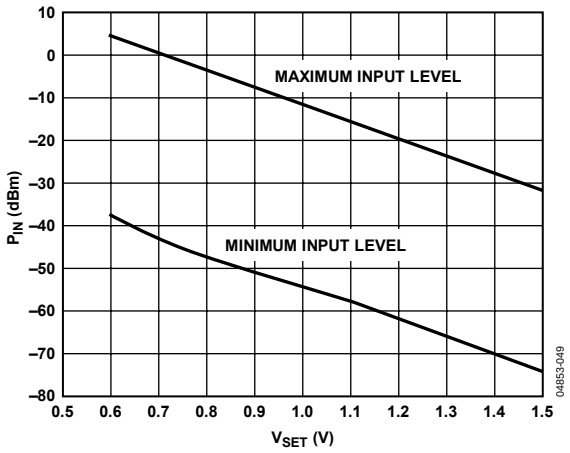


Figure 46. Setpoint Voltage vs. Input Power. Optimal signal levels must be used to achieve the full 45 dB dynamic range capabilities of the AD8367.

In some cases, if V_{GAIN} is >1.0 V it can take an unusually long time for the AGC loop to recover; that is, the output of the AD8318 remains at an abnormally high value and the gain is set to its maximum level. A voltage divider is placed between the output of the AD8318 and the AD8367 GAIN pin to ensure that V_{GAIN} does not exceed 1.0 V.

In Figure 43, C_{HP} and R_{HP} are configured to reduce oscillation and distortion due to harmonics at higher gain settings. Some additional filtering is recommended between the output of the AD8367 and the input of the AD8318. This helps to decrease the output noise of the AD8367, which can reduce the dynamic range of the loop at higher gain settings (smaller V_{SET}).

Response time and the amount of signal integration are controlled by C_{FLT}. This functionality is analogous to the feedback capacitor around an integrating amplifier. Though it is possible to use large capacitors for C_{FLT}, in most applications, values under 1 nF provide sufficient filtering.

Calibration in controller mode is similar to the method used in measurement mode. Do a simple 2-point calibration by applying two known V_{SET} voltages or DAC codes and measuring the output power from the VGA. Slope and intercept are calculated using Equation 20 to Equation 22:

$$Slope = (V_{SET1} - V_{SET2})/(P_{OUT1} - P_{OUT2}) \quad (20)$$

$$Intercept = P_{OUT1} - V_{SET1}/Slope \quad (21)$$

$$V_{SET} = Slope \times (Px - Intercept) \quad (22)$$

For more information on AGC applications, refer to the AD8367 data sheet or ADL5330 data sheet.

CHARACTERIZATION SETUP AND METHODS

The general hardware configuration used for the AD8318 characterization is shown in Figure 47. The primary setup used for characterization is measurement mode. The characterization board is similar to the customer evaluation board with the exception that the RF input has a Rosenberger SMA connector and R10 has changed to a 1 kΩ resistor to remove cable capacitance from the bench characterization setup. Slope and intercept are calculated in this data sheet and in the production environment using linear regression from −50 dBm to −10 dBm. The slope and intercept generate an ideal line. Log conformance error is the difference from the ideal line and the measured output voltage for a given temperature in dB. For additional information on the error calculation, refer to the Device Calibration and Error Calculation section.

The hardware configuration for pulse response measurement replaces the 0 Ω series resistor at the VOUT pin with a 40 Ω resistor; the CLPF pin remains open. Pulse response time is measured using a Tektronix TDS5104 digital phosphor oscilloscope. Both channels on the scope are configured for 50 Ω termination. The 10 Ω internal series resistance at VOUT, combined with the 40 Ω resistor, attenuates the output voltage level by two. RF input frequency is set to 100 MHz with −10 dBm at the input of the device. The RF burst is generated using a Rohde & Schwarz SMT06 with the pulse option with a period of 1.5 µs, a width of 0.1 µs, and a pulse delay of 0.04 µs. The output response is triggered using the video output from the SMT06. Refer to Figure 47 for an overview of the test setup.

To measure noise spectral density, the 0 Ω resistor in series with the VOUT pin is replaced with a 1 µF dc blocking capacitor. The capacitor is used because the Rohde & Schwarz FSEA spectrum analyzer cannot handle dc voltages at its RF input. The CLPF pin is left open for data collected for Figure 19. For Figure 20, a 1 µF capacitor is placed between CLPF and ground. The large capacitor filters the noise from the detector stages of the log amp. Noise spectral density measurements are taken using the FSEA spectrum analyzer and the SMT06 signal generator. The signal generator frequency is set to 2.2 GHz. The spectrum analyzer has a span of 10 Hz, resolution bandwidth of 50 Hz, video bandwidth of 50 Hz, and averages the signal 100×. Data is adjusted to account for the dc blocking capacitor impedance on the output at lower frequencies.

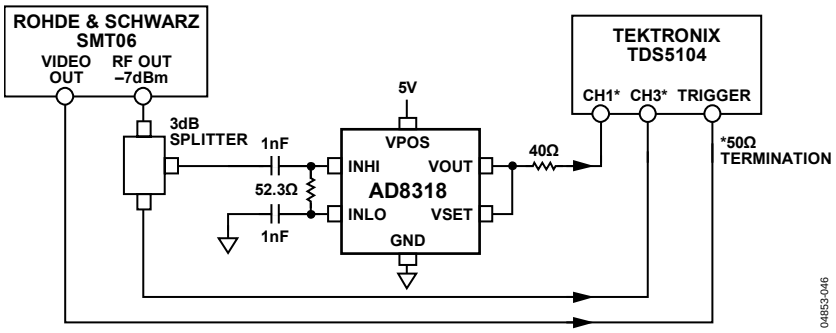


Figure 47. Pulse Response Measurement Test Setup

EVALUATION BOARD

Table 6. Evaluation Board (Rev. A) Bill of Materials

Component	Function	Default Conditions
VP, GND	Supply and Ground Connections	Not Applicable
SW1, R3	Device Enable. When in Position A, the ENBL pin is connected to VP and the AD8318 is in operating mode. In Position B, the ENBL pin is grounded through R3, putting the device in power-down mode. The ENBL pin may be exercised by a pulse generator connected to ENBL SMA and SW1 in Position B.	SW1 = A R3 = 10 kΩ (Size 0603)
R1, C1, C2	Input Interface. The 52.3 Ω resistor (R1) combines with the AD8318 internal input impedance to give a broadband input impedance of 50 Ω. C1 and C2 are dc-blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately valued capacitors.	R1 = 52.3 Ω (Size 0402) C1 = 1 nF (Size 0402) C2 = 1 nF (Size 0402)
R2	Temperature Sensor Interface. The temperature sensor output voltage is available at the SMA labeled TEMP via the current limiting resistor, R2.	R2 = 1 kΩ (Size 0402)
R4	Temperature Compensation Interface. The internal temperature compensation resistor is optimized for an input signal of 2.2 GHz when R4 is 500 Ω. This circuit can be adjusted to optimize performance for other input frequencies by changing the value of Resistor R4. See the Temperature Compensation of Output Voltage section.	R4 = 499 Ω (Size 0603)
R7, R8, R9, R10	Output Interface—Measurement Mode. In measurement mode, a portion of the output voltage is fed back to the VSET pin via R7. The magnitude of the slope at VOUT can be increased by reducing the portion of V_{OUT} that is fed back to VSET. R10 can be used as a back-terminating resistor or as part of a single-pole, low-pass filter.	R7 = 0 Ω = (Size 0402) R8 = open (Size 0402) R9 = open (Size 0402 R10 = 0 Ω (Size 0402)
R7, R8, R9, R10	Output Interface—Controller Mode. In this mode, R7 must be open. In controller mode, the AD8318 can control the gain of an external component. A setpoint voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the AD8318 RF input. The magnitude of the control voltage is optionally attenuated via the voltage divider comprised of R8 and R9, or a capacitor can be installed in R8 to form a low-pass filter along with R9. See the Controller Mode section for more details.	R7 = open (Size 0402) R8 = open (Size 0402) R9 = 0 Ω (Size 0402) R10 = 0 Ω (Size 0402)
C5, C6, C7, C8, R5, R6	Power Supply Decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8318, a 0 Ω series resistor, and a 0.1 µF capacitor placed closer to the power supply input pin.	C5 = 0.1 µF (Size 0603) C6 = 100 pF (Size 0402) C7 = 100 pF (Size 0402) C8 = 0.1 µF (Size 0603) R5 = 0 Ω (Size 0603) R6 = 0 Ω (Size 0603)
C9	Loop Filter Capacitor. The low-pass corner frequency of the circuit that drives the VOUT pin can be lowered by placing a capacitor between CLPF and ground. Increasing this capacitor increases the overall rise/fall time of the AD8318 for pulsed input signals. See the Output Filtering section for more details.	C9 = open (Size 0603)

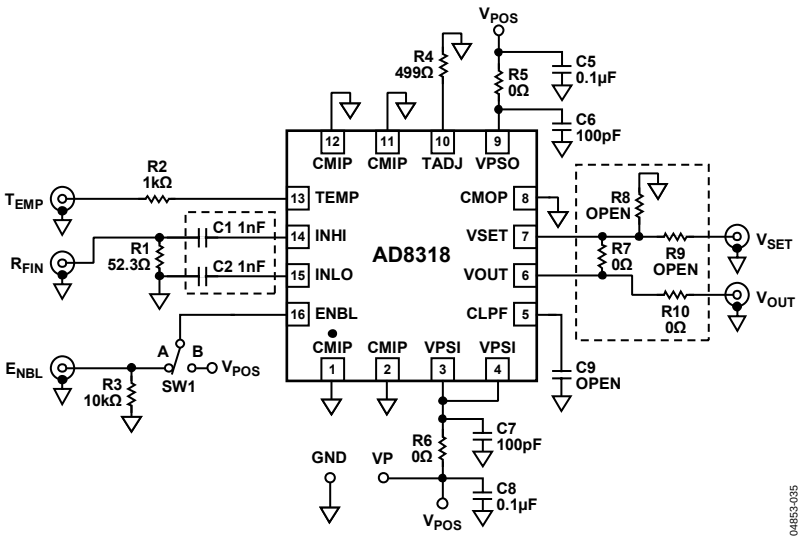


Figure 48. Evaluation Board Schematic

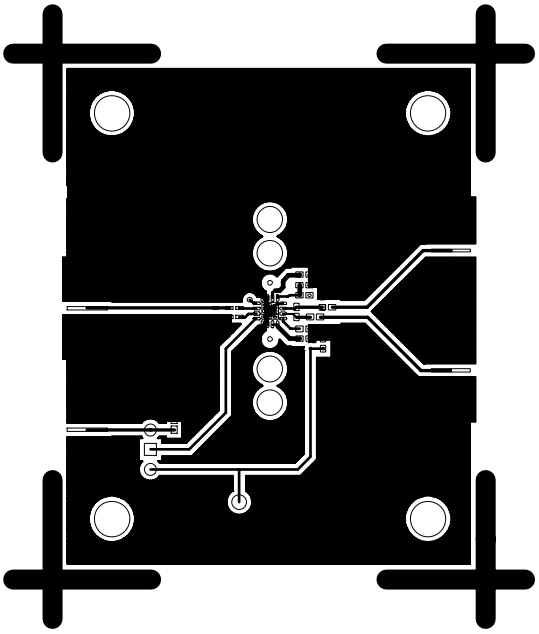


Figure 49. Component Side Layout

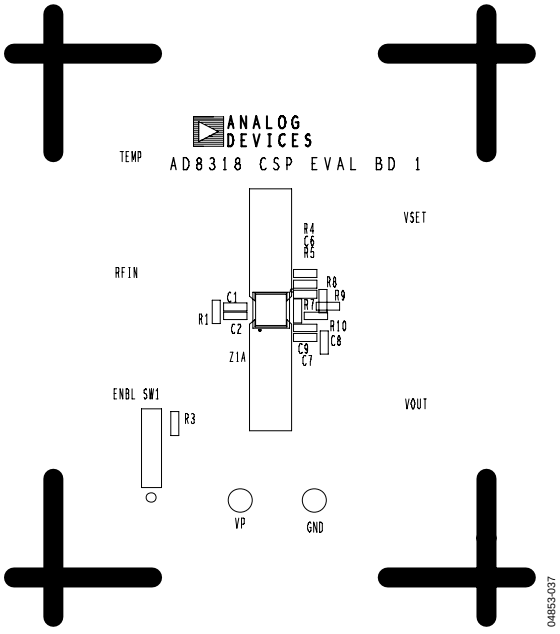


Figure 50. Component Side Silkscreen

OUTLINE DIMENSIONS

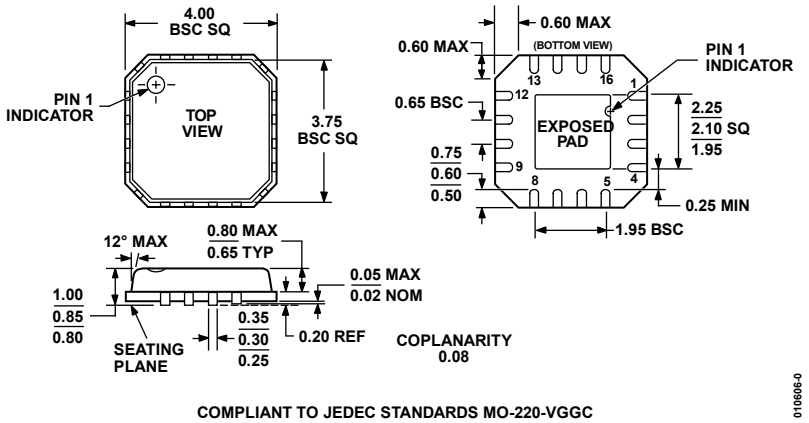


Figure 51. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8318ACPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	1,500
AD8318ACPZ-R2[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	250
AD8318ACPZ-WP[1, 2]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	64
AD8318-EVALZ[1]		Evaluation Board		

[1] Z = RoHS compliant part.
[2] WP = waffle pack.

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