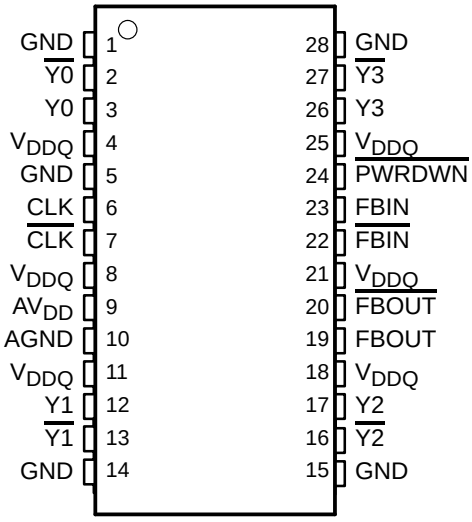
- **Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 180 MHz**
- **Low Jitter (cyc–cyc): ±50 ps**
- **Distributes One Differential Clock Input to Four Differential Clock Outputs**
- **Enters Low Power Mode and Three-State Outputs When Input CLK Signal Is Less Than 20 MHz or PWRDWN Is Low**
- **Operates From Dual 2.5-V Supplies**
- **28-Pin TSSOP Package**
- **Consumes < 200-μA Quiescent Current**
- **External Feedback PIN (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**

PW PACKAGE
(TOP VIEW)



description

The CDCV855 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to four differential pairs of clock outputs (Y[0:3], $\overline{\text{Y[0:3]}}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state), and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low-frequency condition and after applying a >20-MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When AV_{DD} is tied to GND, the PLL is turned off and bypassed for test purposes. The CDCV855 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV855 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PW)
0°C to 70°C	CDCV855PW
–40°C to 85°C	CDCV855IPW

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

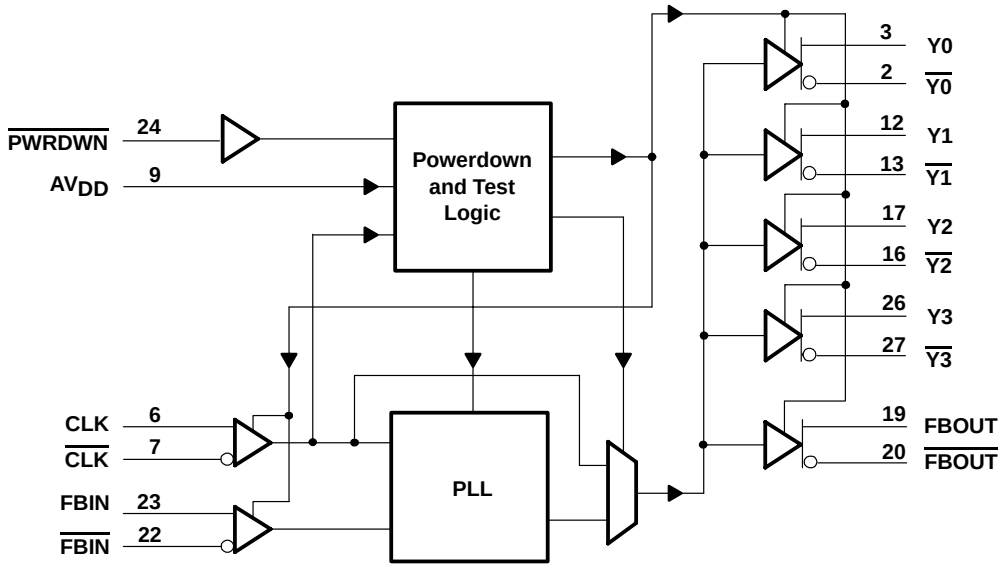
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FUNCTION TABLE
(Select Functions)

INPUTS				OUTPUTS				PLL
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y[0:3]	$\overline{Y[0:3]}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz†	<20 MHz†	Z	Z	Z	Z	Off

† Typically 10 MHz

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	10		Ground for 2.5-V analog supply
AV_{DD}	9		2.5-V analog supply
CLK, $\overline{CLK}$	6, 7	I	Differential clock input
FBIN, $\overline{FBIN}$	23, 22	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	19, 20	O	Feedback differential clock output
GND	1, 5, 14, 15, 28		Ground
$\overline{PWRDWN}$	24	I	Control input to turn device in the power-down mode
V_{DDQ}	4, 8, 11, 18, 21, 25		2.5-V supply
Y[0:3]	3, 12, 17, 26	O	Buffered output copies of input clock, CLK
$\overline{Y[0:3]}$	2, 13, 16, 27	O	Buffered output copies of input clock, $\overline{CLK}$

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DDQ}, AV_{DD} . . . . . –0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current to GND or V_{DDQ} . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package . . . . . 105.8°C/W
Storage temperature range T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DDQ}, AV_{DD}		2.3		2.7	V
Low-level input voltage, V_{IL}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$			$V_{DDQ}/2 - 0.18$	V
	$\overline{PWRDWN}$	–0.3		0.7	
High-level input voltage, V_{IH}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$	$V_{DDQ}/2 + 0.18$			V
	$\overline{PWRDWN}$	1.7		V_{DDQ} + 0.3	
DC input signal voltage (see Note 5)		–0.3		V_{DDQ}	V
Differential input signal voltage, V_{ID} (see Note 6)	CLK, FBIN	0.36		V_{DDQ} + 0.6	V
Output differential cross-voltage, $V_{O(X)}$ (see Note 7)		$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Input differential pair cross-voltage, $V_{I(X)}$ (see Note 7)		$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, I_{OH}				–12	mA
Low-level output current, I_{OL}				12	mA
Input slew rate, SR (see Figure 7)		1		4	V/ns
Operating free-air temperature, T_A	Commercial	0		85	°C
	Industrial	–40		85	

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. DC input signal voltage specifies the allowable dc execution of differential input.
6. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
7. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	All inputs	V_{DDQ} = 2.3 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		V_{DDQ} = min to max,	I_{OH} = –1 mA	V_{DDQ} – 0.1			V
			V_{DDQ} = 2.3 V,	I_{OH} = –12 mA	1.7			
V_{OL}	Low-level output voltage		V_{DDQ} = min to max,	I_{OL} = 1 mA			0.1	V
			V_{DDQ} = 2.3 V,	I_{OL} = 12 mA			0.6	
I_{OH}	High-level output current		V_{DDQ} = 2.3 V,	V_O = 1 V	–18	–32		mA
I_{OL}	Low-level output current		V_{DDQ} = 2.3 V,	V_O = 1.2 V	26	35		mA
V_{OD}	Output voltage swing		Differential outputs are terminated with 120 Ω		1.1		V_{DDQ} – 0.4	V
V_{OX}	Output differential cross-voltage‡				$V_{DDQ}/2$ – 0.2	$V_{DDQ}/2$	$V_{DDQ}/2$ + 0.2	
I_I	Input current		V_{DDQ} = 2.7 V,	V_I = 0 V to 2.7 V			±10	µA
I_{OZ}	High-impedance-state output current		V_{DDQ} = 2.7 V,	V_O = V_{DDQ} or GND			±10	µA
$I_{DD(PD)}$	Power-down current on V_{DDQ} + AV_{DD}		CLK and $\overline{CLK}$ = 0 MHz; $\overline{PWRDWN}$ = Low; Σ of I_{DD} and AI_{DD}			100	200	µA
I_{DD}	Dynamic current on V_{DDQ}		Differential outputs are terminated with 120 Ω / CL = 14 pF	f_O = 167 MHz		150	180	mA
			Differential outputs are terminated with 120 Ω / CL = 0 pF			130	160	
AI_{DD}	Supply current on AV_{DD}		f_O = 167 MHz			8	10	mA
C_I	Input capacitance		V_{DDQ} = 2.5 V	V_I = V_{DDQ} or GND	2	2.5	3	pF
C_O	Output capacitance		V_{DDQ} = 2.5 V	V_O = V_{DDQ} or GND	2.5	3	3.5	pF

† All typical values are at respective nominal V_{DDQ}.
‡ Differential cross-point voltage is expected to track variation of V_{DDQ} and is the voltage at which the differential signals must be crossing.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		MIN	MAX	UNIT
f_{CLK}	Operating clock frequency	60	180	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time (PLL mode)¶		10	µs
	Stabilization time (Bypass mode)§		30	ns

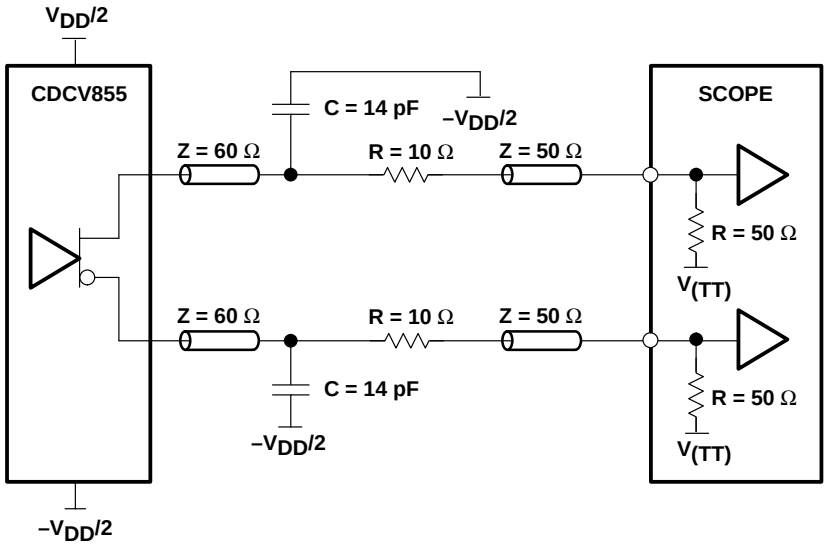
§ Recovery time required when the device goes from power-down mode into bypass mode (test mode with AV_{DD} at GND).
¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}‡	Low-to-high level propagation delay time	Test mode/CLK to any output			4.5		ns
t_{PHL}‡	High-to-low level propagation delay time	Test mode/CLK to any output			4.5		ns
$t_{jit(per)}$§	Jitter (period), See Figure 5	66 MHz		–55		55	ps
		100/133/167/180 MHz		–35		35	ps
$t_{jit(cc)}$§	Jitter (cycle-to-cycle), See Figure 2	66 MHz		–60		60	ps
		100/133/167/180 MHz		–50		50	
$t_{jit(hper)}$§	Half-period jitter, See Figure 6	66 MHz		–130		130	ps
		100 MHz		–90		90	
		133/167/180 MHz		–75		75	
$t_{slr(o)}$	Output clock slew rate, See Figure 7	Load = 120Ω / 14 pF		1		2	V/ns
		Load = 120Ω / 4 pF		1		3	V/ns
$t_{d(Ø)}$§	Dynamic phase offset (this includes jitter), See Figure 3(b)	SSC off	66 MHz	–180		180	ps
			100/133 MHz	–130		130	
			167/180 MHz	–90		90	
		SSC on	66 MHz	–230		230	
			100/133 MHz	–170		170	
			167/180 MHz	–100		100	
$t_{(Ø)}$	Static phase offset, See Figure 3(a)	66 MHz		–150		150	ps
		100/133/167/180 MHz		–100		100	
$tsk_{(o)}$¶	Output skew, See Figure 4					50	ps
tr, tf	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF		650		900	ps

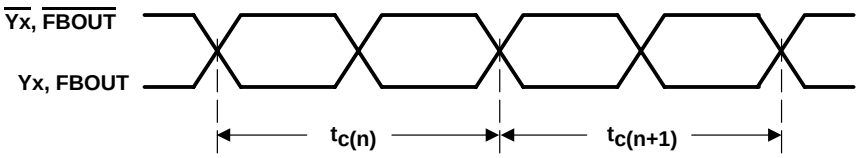
† All typical values are at a respective nominal V_{DDQ}.
‡ Refers to transition of noninverting output
§ This parameter is assured by design but can not be 100% production tested.
¶ All differential output pins are terminated with 120 Ω/14 pF.

PARAMETER MEASUREMENT INFORMATION



NOTE: $V_{(TT)}$ = GND

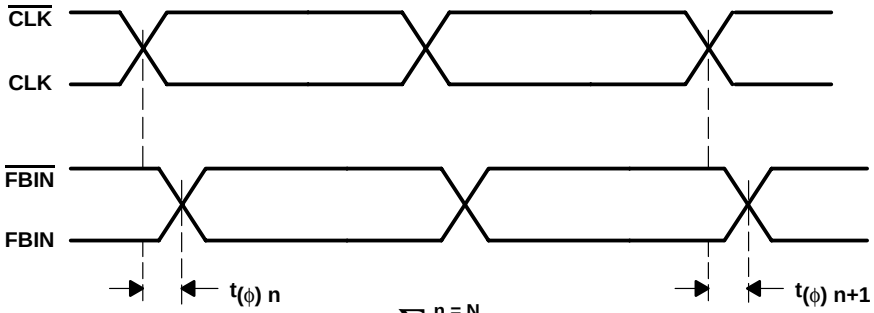
Figure 1. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$

Figure 2. Cycle-to-Cycle Jitter

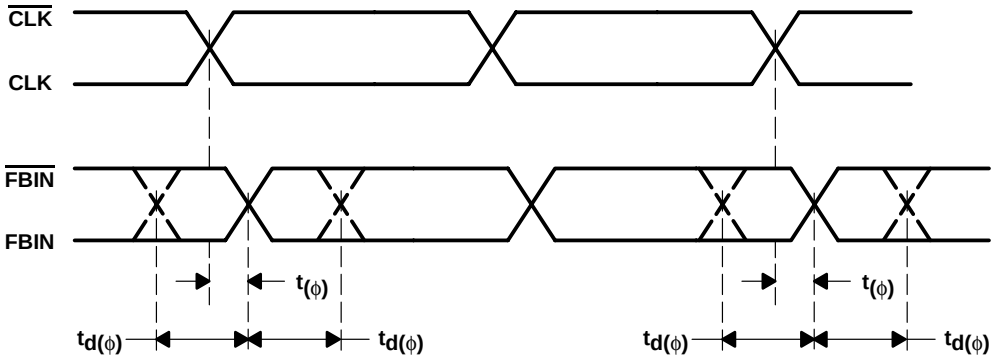
PARAMETER MEASUREMENT INFORMATION



$$t_{(\phi)} = \frac{\sum_{1}^{n=N} t_{(\phi)\,n}}{N}$$

(N is a Large Number of Samples)

(a) Static Phase Offset



(b) Dynamic Phase Offset

Figure 3. Phase Offset

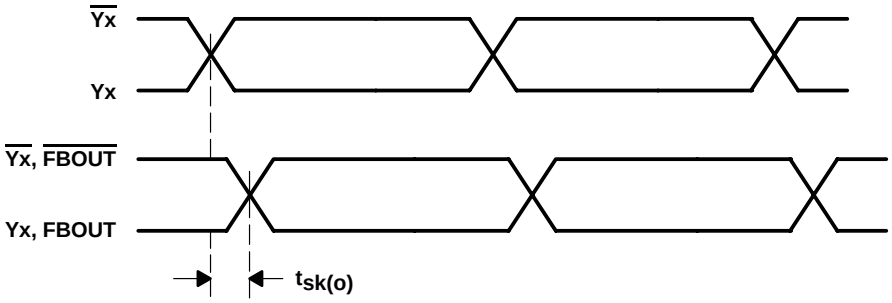


Figure 4. Output Skew

PARAMETER MEASUREMENT INFORMATION

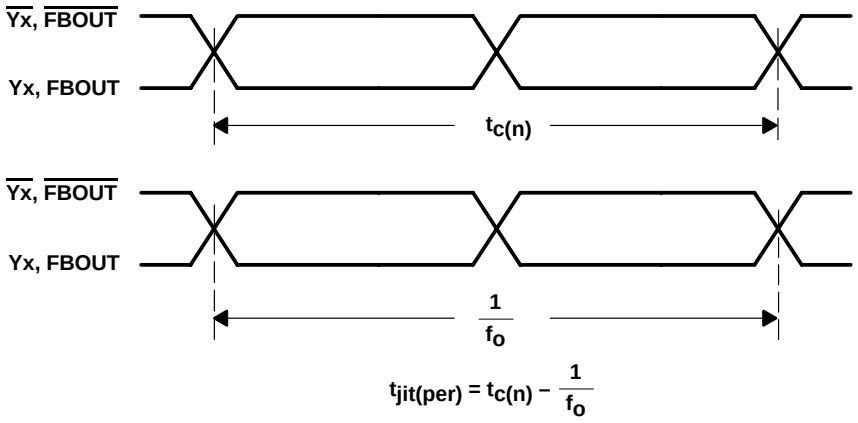


Figure 5. Period Jitter

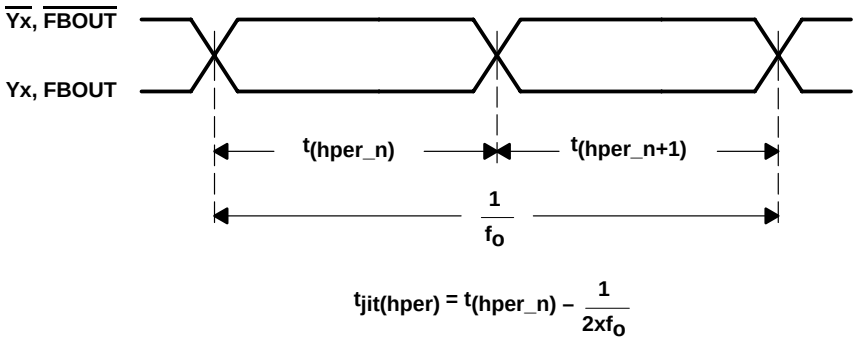


Figure 6. Half-Period Jitter

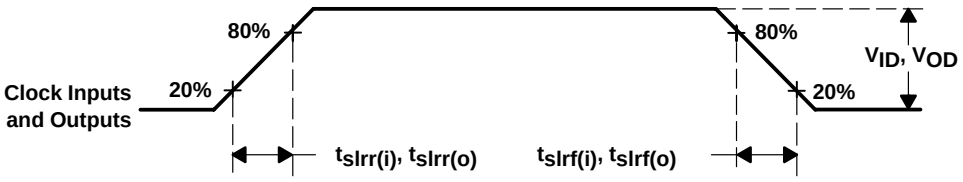
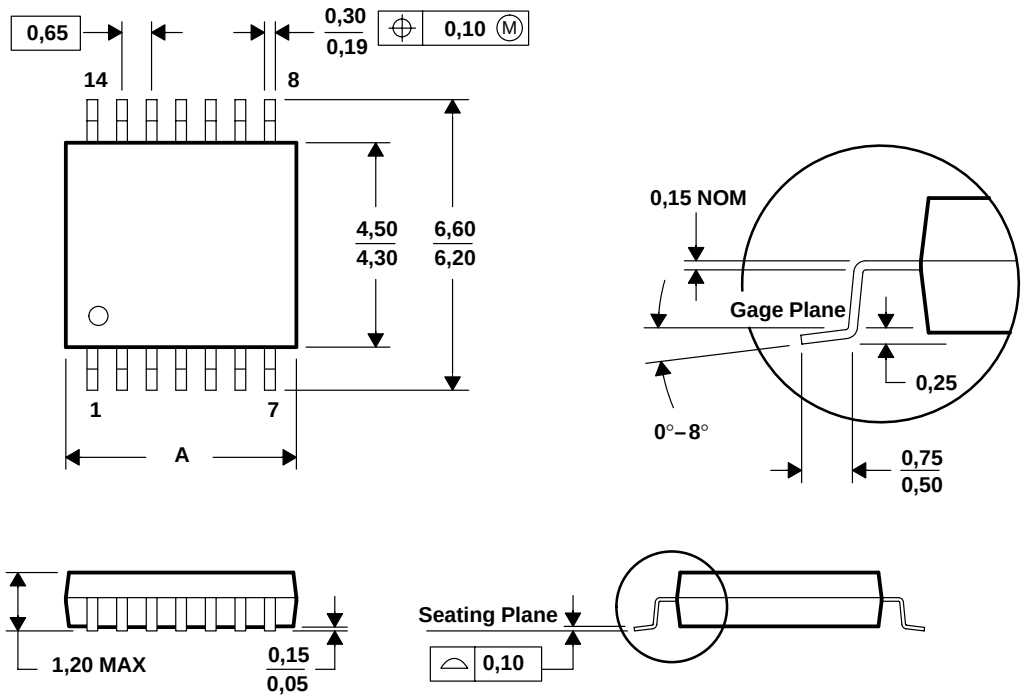


Figure 7. Input and Output Slew Rates

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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