Dual Digitally Controlled Potentiometer (XDCP™) & Voltage Comparator

FEATURES

- **Two digitally controlled potentiometers and two voltage comparators in one package**
- **SPI serial interface**
- **Register oriented format**
  - **—Direct read/write wiper position**
  - **—Store as many as four positions per pot**
- **Fast response comparator**
- **Enable, latch, or shutdown comparator outputs through the ACR**
- **Auto-recall of WCR and ACR data from R0**
- **Hardware write protection, $\overline{WP}$**
- **Separate analog and digital/system supplies**
- **Direct write cell**
  - **—Endurance–100,000 data changes per bit per register**
  - **—Register data retention–100 years**
- **16-bytes of EEPROM memory**
- **Power saving feature and low noise**
- **Two 10kΩ or two 2.5kΩ potentiometers**
- **Resolution: 64 taps each pot**
- **24-lead TSSOP and 24-Lead SOIC packages**

DESCRIPTION

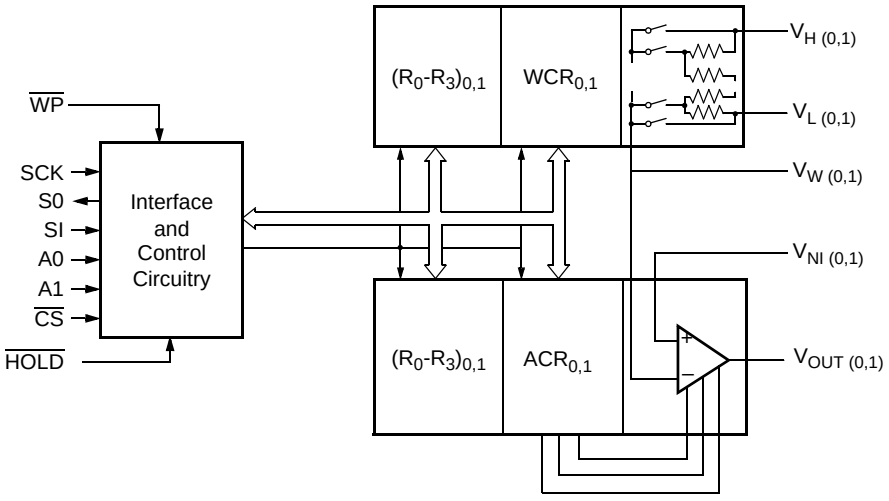
The X9440 integrates two non volatile digitally controlled potentiometers (XDCP) and two voltage comparators on a CMOS monolithic microcircuit.

The X9440 contains two resistor arrays, each composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the SPI serial bus interface.

Each potentiometer has an associated voltage comparator. The comparator compares the external input voltage V_{NI} with the wiper voltage V_W and sets the output voltage level to a logic high or low.

Each resistor array and comparator has associated with it a wiper counter register (WCR), analog control register (ACR), and eight 6 bit data registers that can be directly written and read by the user. The contents of the wiper counter register controls the position of the wiper on the resistor array. The contents of the analog control register controls the comparator and its output. The potentiometer is programmed with a SPI serial interface.

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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PIN DESCRIPTIONS

Host Interface Pins

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9440.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9440 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9440, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

Device Address (A_0-A_1)

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9440. A maximum of 4 devices may share the same SPI serial bus.

Potentiometer Pins

V_H (V_{H0}-V_{H3}), V_L (V_{L0}-V_{L3})

The V_H and V_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0}-V_{W1})

The wiper output V_W is equivalent to the wiper output of a mechanical potentiometer and is connected to the inverting input of the voltage comparator.

Comparator and Device Pins

Voltage Input V_{NI0}, V_{NI1}

V_{NI0} and V_{NI1} are the input voltages to the plus (non-inverting) inputs of the two comparators.

Buffered Voltage Outputs V_{OUT0}, V_{OUT1}

V_{OUT0} and V_{OUT1} are the buffered voltage comparator outputs controlled by bits in the volatile analog control register.

Hardware Write Protect Input $\overline{WP}$

The $\overline{WP}$ pin when low prevents non volatile writes to the wiper counter and analog control registers.

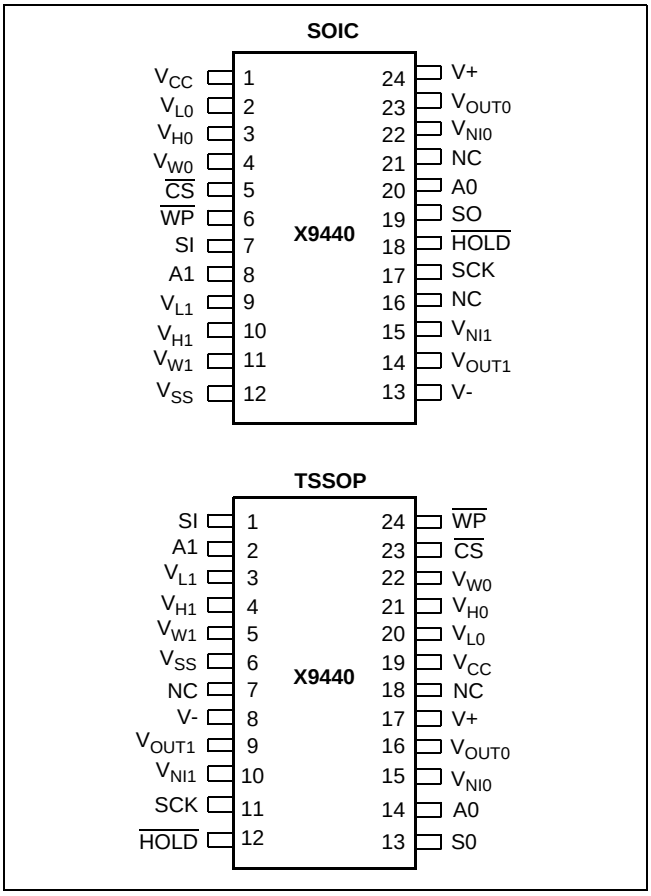
Analog Supplies V+, V-

The Analog Supplies V+, V- are the supply voltages for the XDCP analog section and the voltage comparators.

System Supply V_{CC} and Ground V_{SS}

The system supply, V_{CC} and its reference V_{SS} is used to bias the interface and control circuits.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCK	Serial Clock
S1, SO	Serial Data
A0-A1	Device Address
V_{H0}-V_{H1}, V_{L0}-V_{L1}	Potentiometers (terminal equivalent)
V_{W0}–V_{W1}	Potentiometers (wiper equivalent)
V_{NI0}, V_{NI1}	Comparator Input Voltages
$V_{OUT0,}$ V_{OUT1}	Buffered Comparator Outputs
$\overline{WP}$	Hardware Write Protection
V+,V-	Analog and Voltage Comparator Supplies
V_{CC}	System Supply Voltage
V_{SS}	System Ground
NC	No Connection

PRINCIPLES OF OPERATION

The X9440 is a highly integrated microcircuit incorporating two resistor arrays, two voltage comparators and their associated registers and counters; and the serial interface logic providing direct communication between the host and the digitally-controlled potentiometers and voltage comparators.

Serial Interface

The X9440 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Array Description

The X9440 is comprised of two resistor arrays and two voltage comparators. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by a volatile wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Voltage Comparator

The comparator compares the wiper voltage V_W with the external input voltage V_{NI}. The comparator and its logic level output are controlled by the shutdown, latch, and enable bits of the analog control register (ACR). Enable connects the comparator output to the V_{OUT} pin, Latch memorizes the output logic state, and shutdown removes the analog section supply voltages to save power. The analog control register (ACR) is programmed using the SPI serial interface.

The ACR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the ACR. These data registers and the ACR may be read and written by the host system.

REGISTERS

Both digitally-controlled potentiometers and voltage comparators share the serial interface and share a common architecture. Each potentiometer and voltage comparator is associated with wiper counter and analog control registers and eight data registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter (WCR) and Analog Control Registers (ACR)

The X9440 contains two wiper counter registers: one for each XDCP potentiometer and two Analog Control Registers, and one for each of the two voltage comparators. The wiper counter register is equivalent to a serial-in, parallel-out counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the wiper counter register and analog control register can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers (DR) via the XFR data register instruction (parallel load); it can be modified one step at a time by the increment/ decrement instruction (WCR only). Finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The wiper counter and analog control register are volatile registers; that is, their contents are lost when the X9440 is powered-down. Although the registers are automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

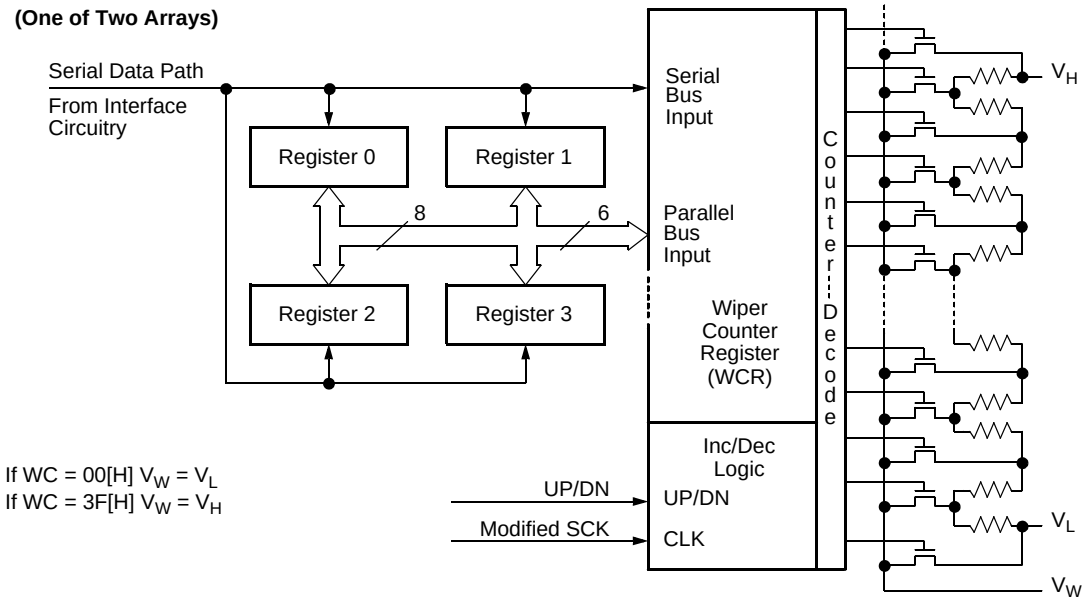
Programming the ACR is similar to the WCR. However, the 6 bits in the WCR positions the wiper in the resistor array while 3 bits in the ACR control the comparator and its output.

Data Registers (DR)

Each potentiometer and each voltage comparator has four non volatile data registers (DR). These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR or ACR. It should be noted all operations changing data in one of these registers is a non volatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer or comparator, these registers can be used as regular memory locations that could store system parameters or user preference data.

Figure 1. Detailed Potentiometer Block Diagram



REGISTER BIT DESCRIPTIONS

Wiper Counter Register (WCR)

0	0	WP5	WP4	WP3	WP2	WP1	WP0
		(volatile)					(LSB)

WP0-WP5 identify wiper position.

Analog Control Register (ACR)

0	0	User-bit5	User-bit4	User-bit3	Latch	Enable	Shut-down
		(volatile)					(LSB)

Shutdown

"1" indicates power is connected to the voltage comparator.

"0" indicates power is not connected to the voltage comparator.

Enable

"1" indicates the output buffer of the voltage comparator is enabled.

"0" indicates the output buffer of the voltage comparator is disabled.

Latch

"1" indicates the output of the voltage comparator is memorized or latched.

"0" indicates the output of the voltage comparator is not latched.

Userbits—available for user applications

Data Registers (DR, R_0-R_3)

Wiper Position or Analog Control Data or User Data
(Nonvolatile)

{Refer to Memory Map, Figure 9}

INSTRUCTIONS AND PROGRAMMING

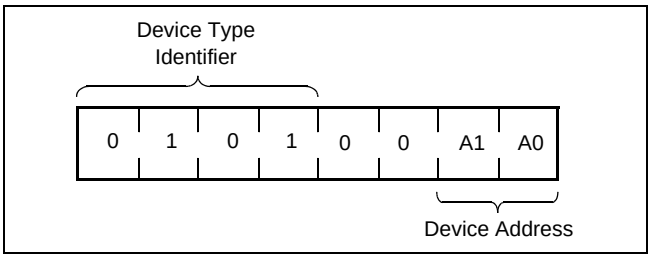
Identification (ID) Byte

The first byte sent to the X9440 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier, for the X9440 this is fixed as 0101[B] (refer to Figure 2).

The two least significant bits in the ID byte select one of four devices on the bus. The physical device address is defined by the state of the A_0-A_1 input pins. The X9440 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9440 to successfully continue the command sequence. The A_0-A_1 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

The remaining two bits in the slave byte must be set to 0.

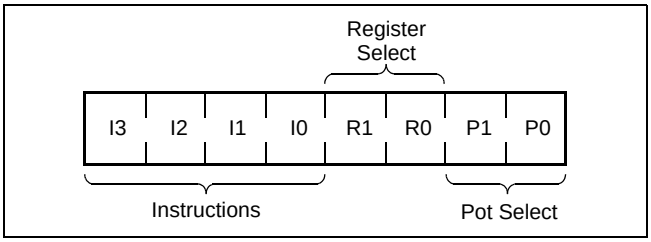
Figure 2. Identification Byte Format



Instruction Byte

The byte following the address contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the two pots or two voltage comparators and when applicable they point to one of four associated registers. The format is shown below in Figure 3.

Figure 3. Instruction Byte Format



The four high order bits of the instruction byte specify the operation. The next two bits (R_1 and R_0) select one of the four data registers that is to be acted upon when a register oriented instruction is issued. The last two bits (P_1 and P_0) selects which one of the four potentiometers is to be affected by the instruction.

The four high order bits define the instruction. The next two bits (R_1 and R_0) select one of the four data registers that is to be acted upon when a register oriented instruction is issued. The last two bits (P_1 and P_0) select which one of the two potentiometers or which one of the two voltage comparators is to be affected by the instruction.

Four of the ten instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 4. These two-byte instructions exchange data between the wiper counter register or analog control register and one of the data registers. A transfer from a data register to a wiper counter register or analog control register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{WRL}. A transfer from the wiper counter register current wiper position to a data register is a write to non volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the two potentiometers or one of the two voltage comparators and one of its associated registers; or it may occur globally, wherein the transfer occurs between both of the potentiometers and voltage comparators and one of their associated registers.

Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9440; either between the host and one of the data registers or directly between the host and the wiper counter and analog control registers. These instructions are: Read Wiper Counter Register or Analog Control Register, read the current wiper position of the selected pot or the comparator control bits, Write Wiper Counter Register or Analog Control Register, i.e. change current wiper position of the selected pot or control the voltage comparator; Read Data Register, read the contents of the selected non volatile register; Write Data Register, write a new value to the selected data register. The bit structures of the instructions are shown in Figure 9.

The sequences of the three byte operations are shown in Figure 5 and Figure 6.

The bit structures of the instructions and the description of the instructions are shown in Figure 10.

Figure 4. Two-Byte Command Sequence

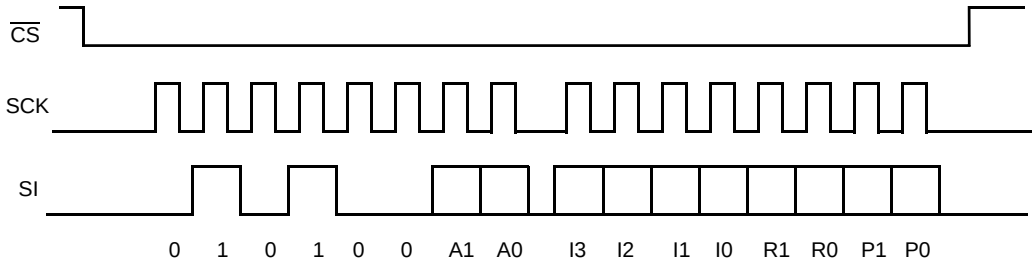


Figure 5. Three-Byte Command Sequence (Write)

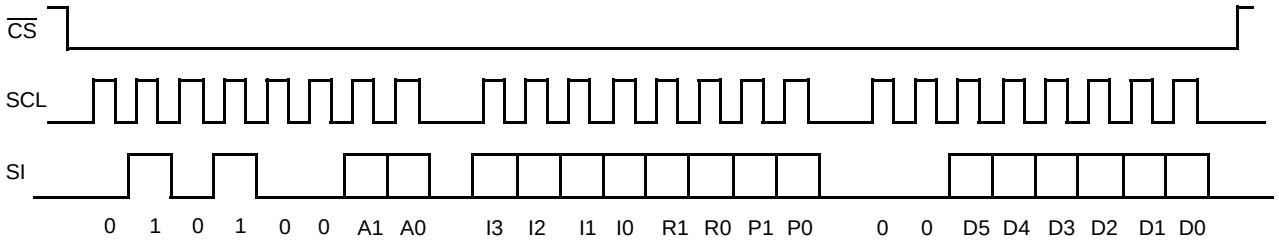


Figure 6. Three-Byte Command Sequence (Read)

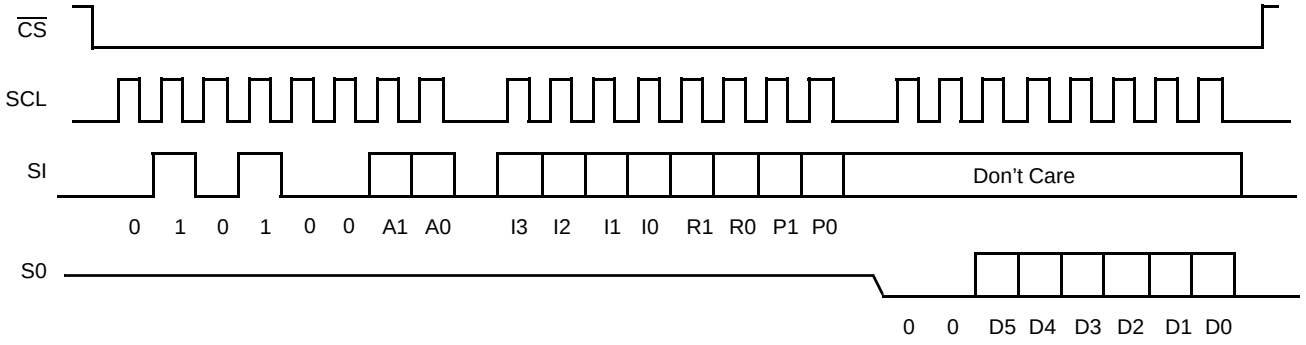
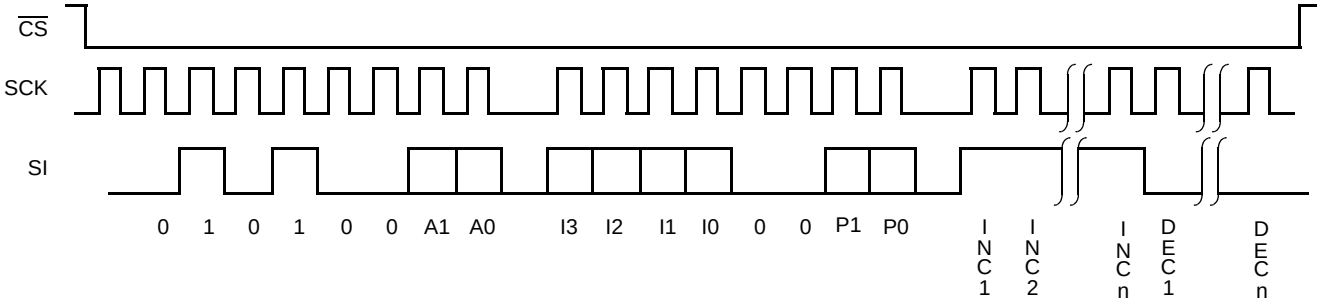


Figure 7. Increment/Decrement Command Sequence



Increment/Decrement

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 7 and 8.

Write in Process

The contents of the data registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a write in process bit (WIP). The WIP bit is read with a read status command.

Figure 8. Increment/Decrement Timing Limits

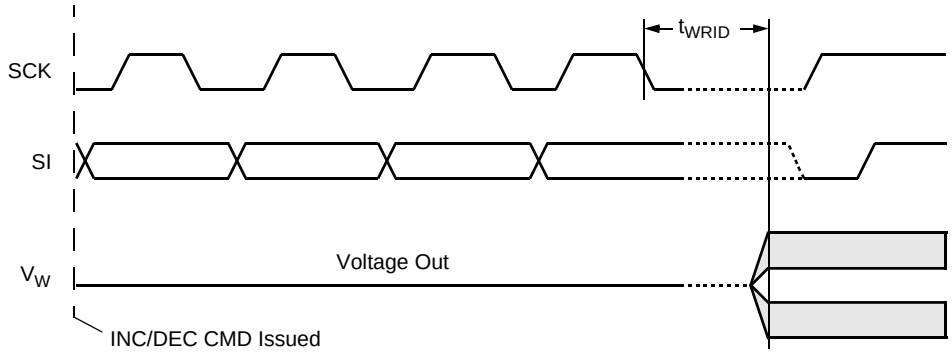


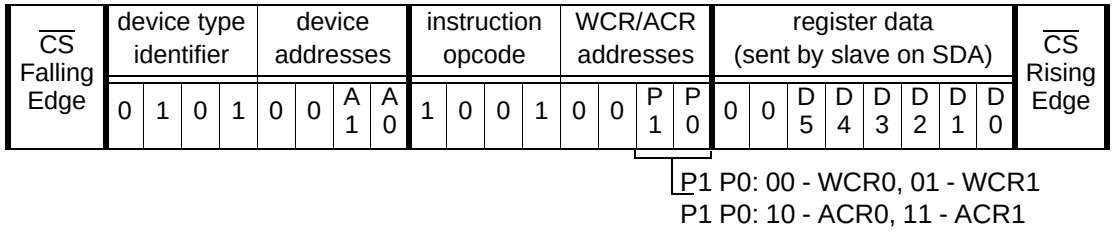
Figure 9. Memory Map

WCRO	WCR1	ACR0	ACR1
R0	R0	R0	R0
R1	R1	R1	R1
R2	R2	R2	R2
R3	R3	R3	R3

Figure 10. Instruction Set

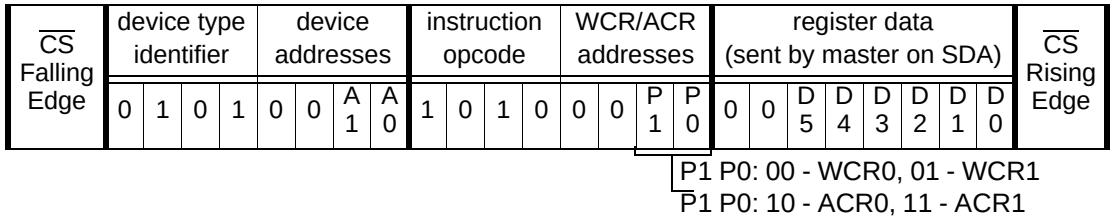
Read Wiper Counter Register (WCR) or Analog Control Register (ACR)

Read the contents of the Wiper Counter Register or Analog Control Register pointed to by P_1 - P_0.



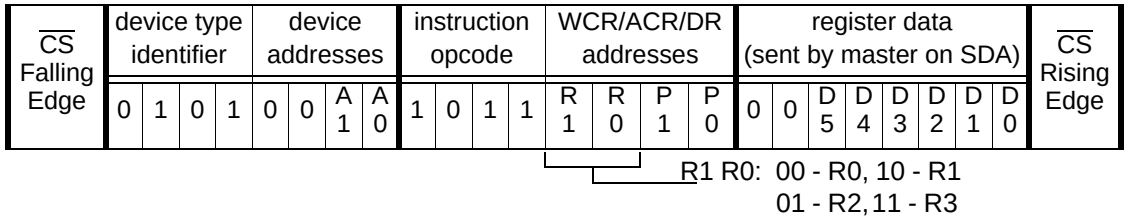
Write Wiper Counter Register (WCR) or Analog Control Register (ACR)

Write new value to the Wiper Counter Register or Analog Control Register pointed to by P_1 - P_0.



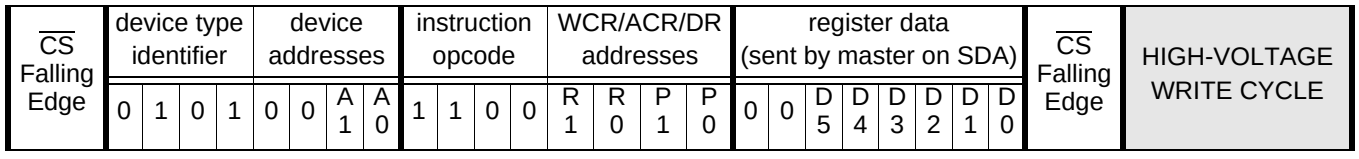
Read Data Register (DR)

Read the contents of the Register pointed to by P_1 - P_0 and R_1 - R_0.



Write Data Register (DR)

Write new value to the Register pointed to by P_1 - P_0 and R_1 - R_0.



Transfer Data Register to Wiper Counter Register or Analog Control Register

Transfer the contents of the Register pointed to by R_1 - R_0 to the WCR or ACR pointed to by P_1 - P_0.

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR/ACR/DR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	P1	P0	

Transfer Wiper Counter or Analog Control Register to Data Register

Transfer the contents of the WCR or ACR pointed to by P_1 - P_0 to the Register pointed to by R_1 - R_0.

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR/ACR/DR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	P1	P0		

Global Transfer Data Register to Wiper Counter or Analog Control Register

Transfer the contents of all four Data Registers pointed to by R_1 - R_0 to their respective WCR or ACR.

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	R1	R0	0	0	

Global Transfer Wiper Counter or Analog Control Register to Data Register

Transfer the contents of all WCRs and ACRs to their respective data Registers pointed to by R_1 - R_0.

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	R1	R0	0	0		

Increment/Decrement Wiper Counter Register

Enable Increment/decrement of the WCR pointed to by P_1 - P_0.

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				increment/decrement (sent by master on SDA)						$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	1	0	0	0	P1	P0	I/D	I/D	. . . .		I/D	I/D	

P1 P0: 00 or 01 only.
I/D: Increment/Decrement, 1/0

Read Status

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				wiper addresses				Data Byte (sent by X9440 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on SCK, SCL or any address input
with respect to V_{SS} ..... -1V to +7V
Voltage on V+ (referenced to V_{SS}) ..... +7V
Voltage on V- (referenced to V_{SS}) ..... -7V
(V+) - (V-) 12V
Any V_H ..... V+
Any V_L ..... V-
Lead temperature (soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Device	Supply Voltage (V_{CC}) Limits
X9440	5V ±10%
X9440-2.7	2.7V to 5.5V

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Test Conditions
R_{TOTAL}	End to end resistance		–20		+20	%	
	Power rating				50	mW	25°C, each pot
I_W	Wiper current		–3		+3	mA	
R_W	Wiper resistance			40	100	Ω	V_{CC} = 5V, Wiper Current = 3mA
				100	250	Ω	V_{CC} = 2.7-5V, Wiper Current = 3mA
Vv+	Voltage on V+ pin	X9440	+4.5		+5.5	V	
		X9440-2.7	+2.7		+5.5		
Vv-	Voltage on V- pin	X9440	-5.5		-4.5	V	
		X9440-2.7	-5.5		-2.7		
V_{TERM}	Voltage on any V_H or V_L pin		V-		V+	V	
	Noise			-120		dBV	Ref: 1kHz
	Resolution (4)			1.6		%	
	Absolute linearity (1)		-1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative linearity (2)		-0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature coefficient of R_{TOTAL}			±300		ppm/°C	

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or $(V_H - V_L)/63$, single pot
(4) Individual array resolutions.

COMPARATOR ELECTRICAL CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{OS}	Input offset voltage	-1 -5		1 5	mV mV	V+/V- = ±3V V+/V- = ±5V
I_B	Input current		10		pA	
V_{IR}	Input voltage range	V-		V+	V	
t_R	Response time		200		ns	note 1
I_O	Output current	-1		1	mA	
A_V	Voltage gain		300		V/mV	
PSRR	Power supply rejection ratio		60		dB	
V_{OR}	Output voltage range	V_{SS}		V_{CC}	V	
T_CV_{OS}	Input offset voltage drift		6		µV/°C	
I_S	Supply current (V+ to V-)		1.2 .5		mA mA	V+/V- = ±5V V+/V- = ±3V
T_{ON}	Comparator enable time		1		µs	note 2
V_{OL}	Output low voltage			0.4	V	I_O = 1mA
V_{OH}	Output high voltage	V_{CC}-0.8			V	I_O = 1mA

Notes: (1) 100mV step with 100mV overdrive, ZL = 10kΩ || 15pF, 10-90% risetime
(2) Time from leading edge of Enable bit to valid V_{OUT}.

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{CC1}	V_{CC} supply current (active)			400	µA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{CC2}	V_{CC} supply current (nonvolatile write)			1	mA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			1	µA	SCK = SI = V_{SS}, Addr. = V_{SS}
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Input LOW voltage	-0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

CAPACITANCE

Symbol	Test	Max.	Unit	Test Conditions
$C_{I/O}$	Output capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input capacitance (A0, A1, SI, and SCK)	6	pF	V_{IN} = 0V
C_L, C_H, C_W	Potentiometer capacitance	10/10/25	pF	

POWER-UP SEQUENCE

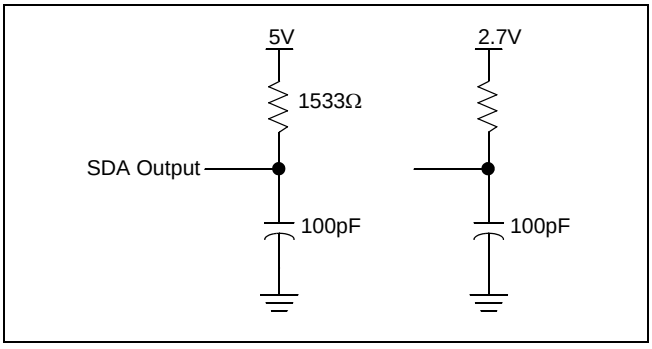
Power-up Sequence(1): (1) V_{CC} (2) V+ and V- {V+ ≤ V_{CC} at all times}
Power-down Sequence: no limitation

A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Note: (1) Applicable to recall and power consumption applications

EQUIVALENT A.C. LOAD CIRCUIT



AC TIMING

Symbol	Parameter	Min.	Max.	Unit
f_{SCK}	SSI/SPI clock frequency		2.0	MHz
t_{CYC}	SSI/SPI clock cycle time	500		ns
t_{WH}	SSI/SPI clock high time	200		ns
t_{WL}	SSI/SPI clock low time	200		ns
t_{LEAD}	Lead time	250		ns
t_{LAG}	Lag time	250		ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
t_{H}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
t_{RI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	µs
t_{FI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	µs
t_{DIS}	SO output disable time	0	500	ns
t_{V}	SO output valid time		100	ns
t_{HO}	SO output hold time	0		ns
t_{RO}	SO output rise time		50	ns
t_{FO}	SO output fall time		50	ns
t_{HOLD}	$\overline{HOLD}$ time	400		ns
t_{HSU}	$\overline{HOLD}$ setup time	100		ns
t_{HH}	$\overline{HOLD}$ hold time	100		ns
t_{HZ}	$\overline{HOLD}$ low to output in high Z		100	ns
t_{LZ}	$\overline{HOLD}$ high to output in low Z		100	ns
T_{I}	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		20	ns
t_{CS}	$\overline{CS}$ Deselect Time	2		µs
t_{WPASU}	$\overline{WP}$, A0 and A1 setup time	0		ns
t_{WPAH}	$\overline{WP}$, A0 and A1 hold time	0		ns

HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Unit
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

XDCP TIMING

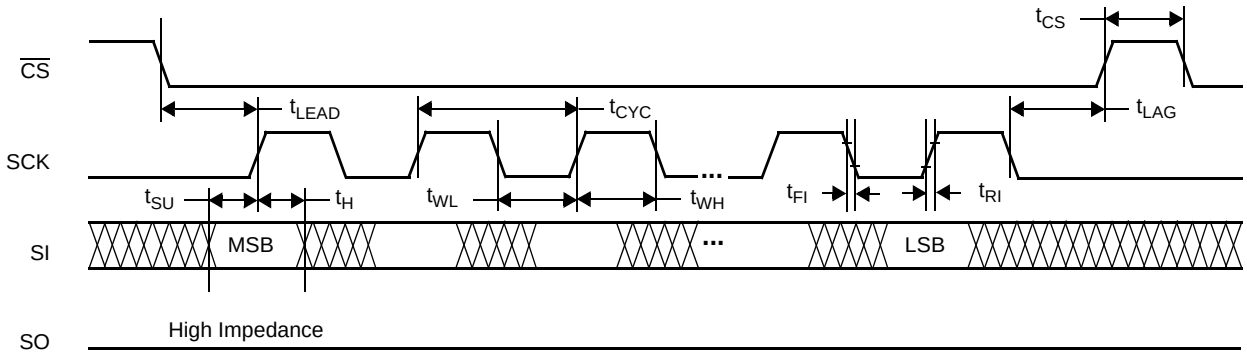
Symbol	Parameter	Min.	Max.	Unit
t_{WRPO}	Wiper response time after the third (last) power supply is stable		10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)		10	µs
t_{WRID}	Wiper response time from an active SCL/SCK edge (increment/decrement instruction)		450	µs

SYMBOL TABLE

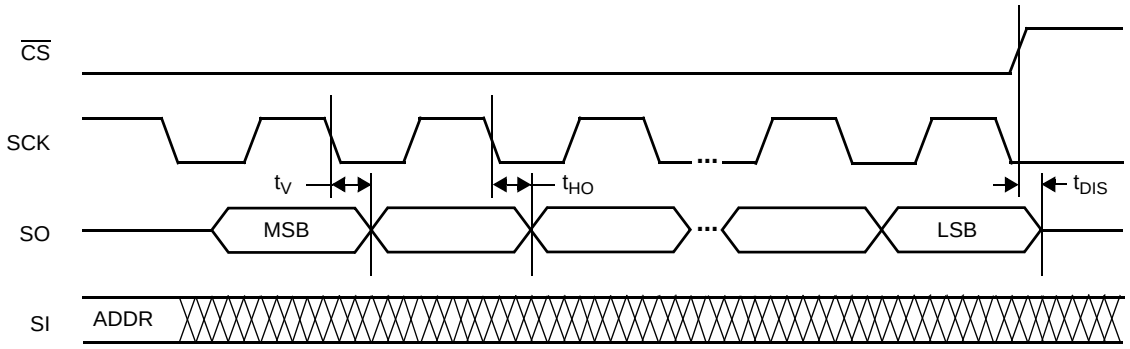
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

TIMING DIAGRAMS

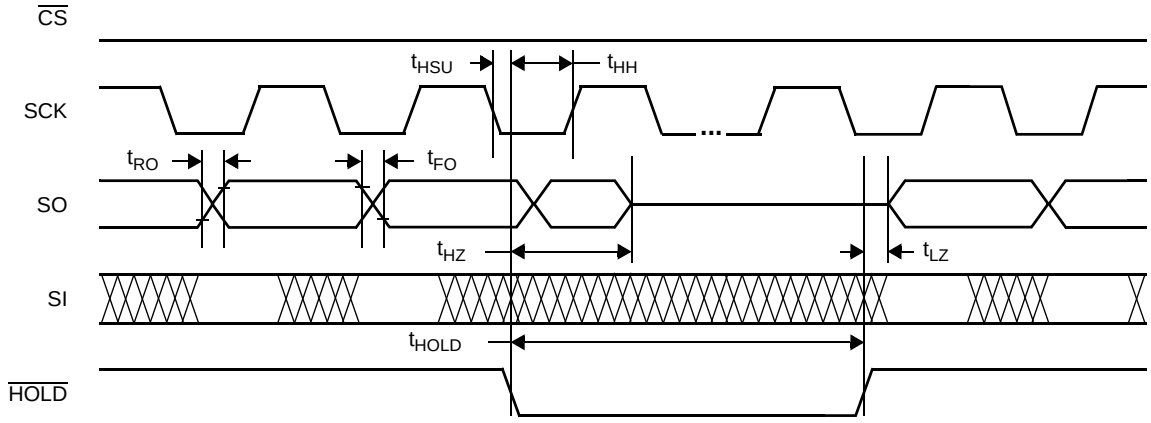
Input Timing



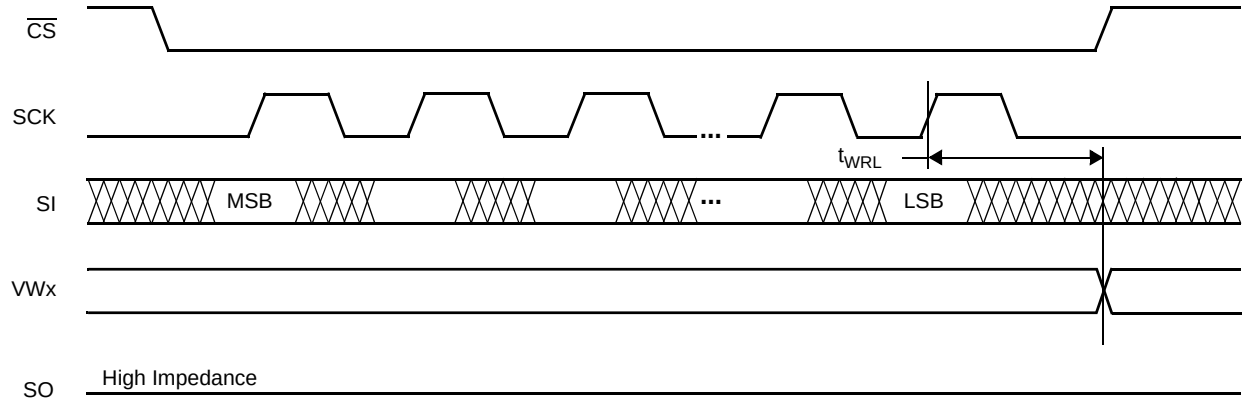
Output Timing



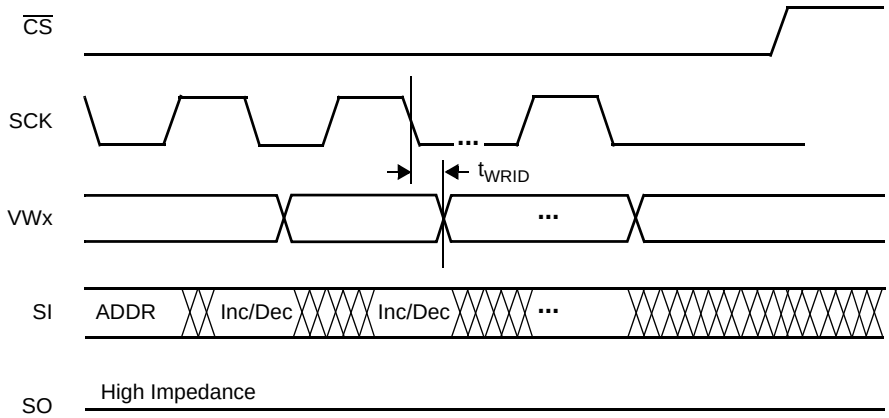
Hold Timing



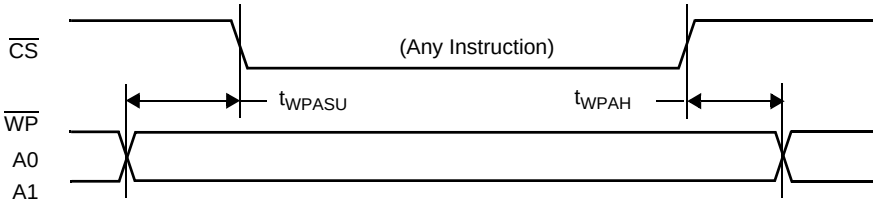
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)

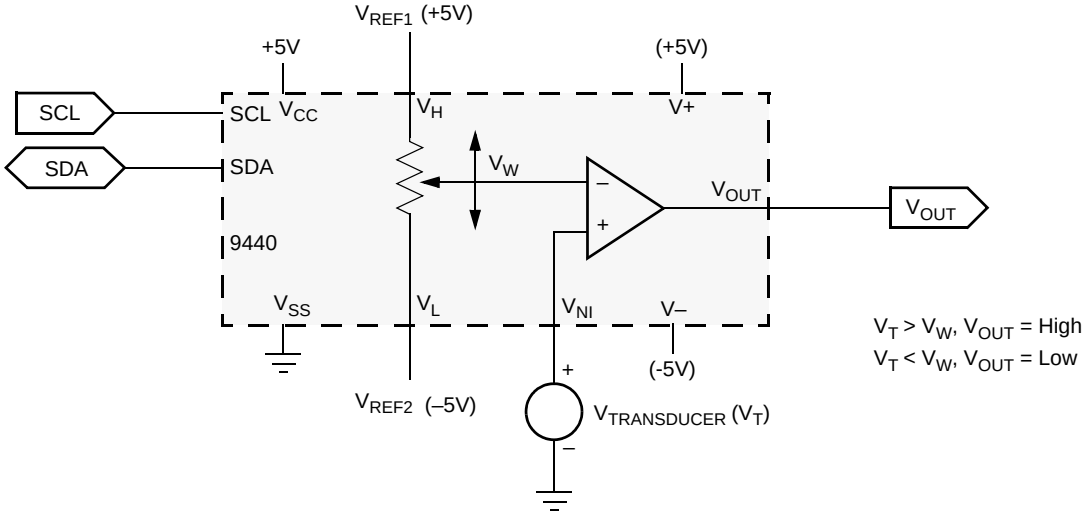


Write Protect and Device Address Pins Timing

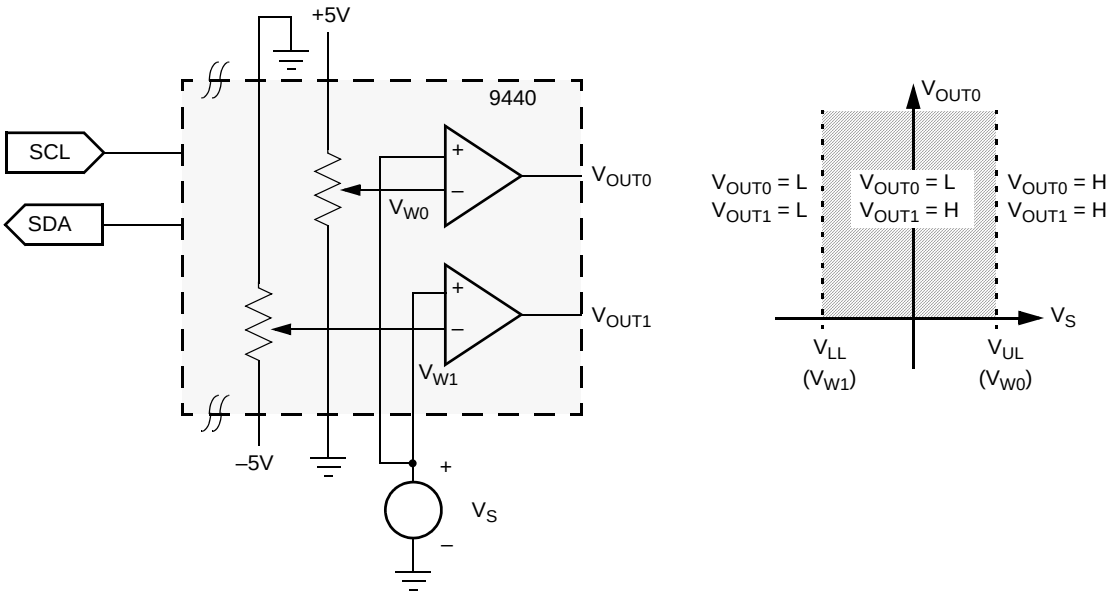


BASIC APPLICATIONS

Programmable Level Detector with Memory (typical bias conditions)



Programmable Window Detector with Memory

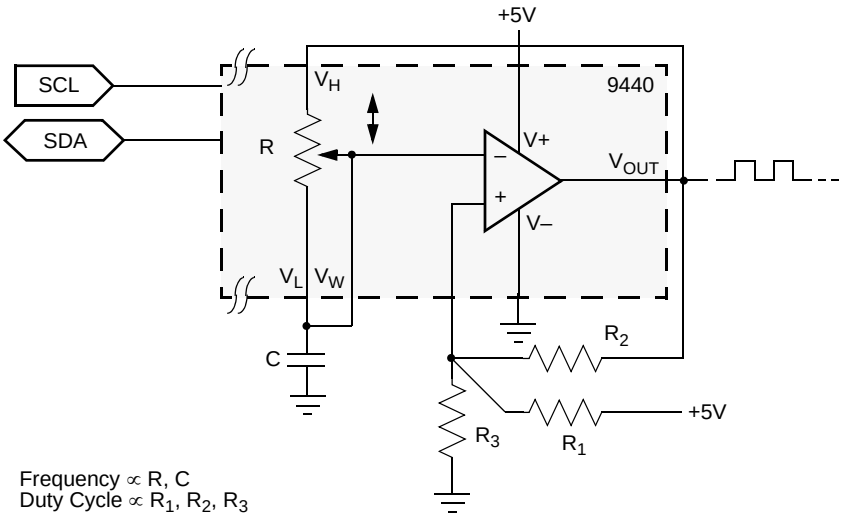


For the signal voltage V_S > the upper limit V_{UL}, (V_{OUT0} = H) • (V_{OUT1} = H)
V_S < the lower limit V_{LL}, (V_{OUT0} = L) • (V_{OUT1} = L)

For the window $V_{LL} \leq V_S \leq V_{UL}$, ($V_{OUT0}$ = L) • (V_{OUT1} = H)

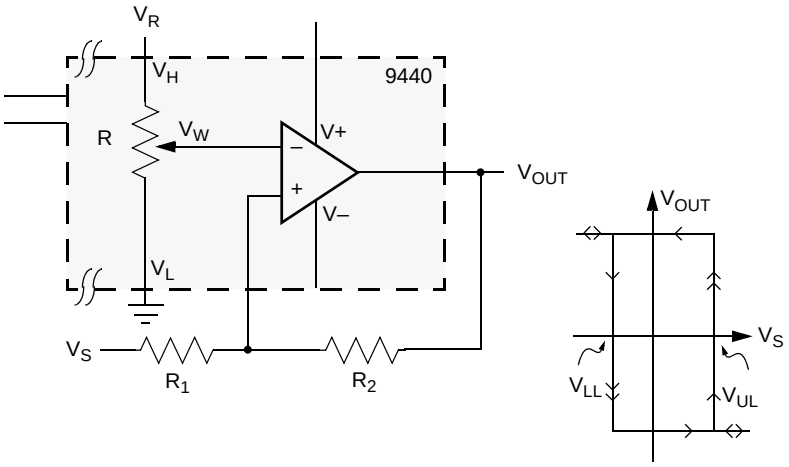
BASIC APPLICATION (continued)

Programmable Oscillator with Memory



Frequency ∝ R, C
Duty Cycle ∝ R_1, R_2, R_3

Programmable Schmitt Trigger with Memory

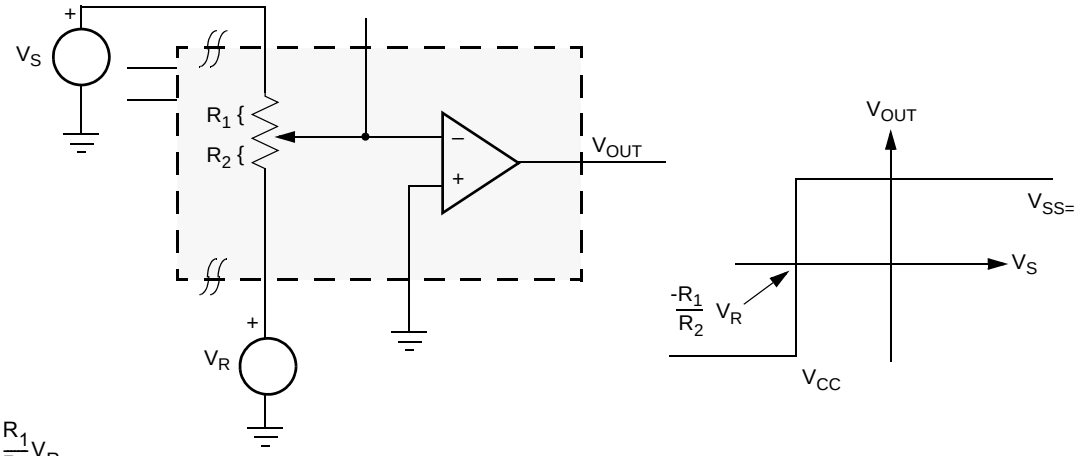


$$V_{UL} = \frac{R_1 + R_2}{R_2} V_W - \frac{R_1}{R_2} V_{OUT(min)}$$

$$V_{LL} = \frac{R_1 + R_2}{R_2} V_W - \frac{R_1}{R_2} V_{OUT(max)}$$

BASIC APPLICATION (continued)

Programmable Level Detector (alternate technique)

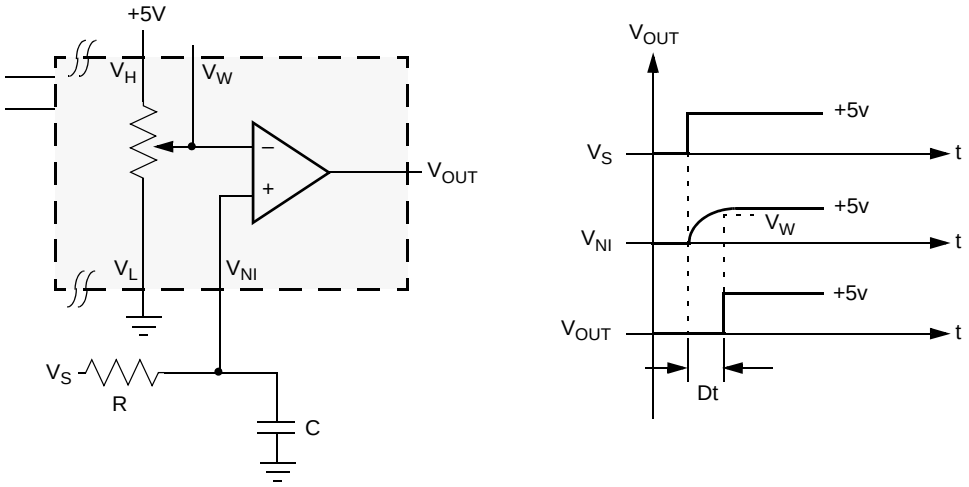


V_{OUT} = High for $V_S < -\frac{R_1}{R_2}V_R$

V_{OUT} = Low for $V_S > -\frac{R_1}{R_2}V_R$

$R_1 + R_2 = R_{POT}$

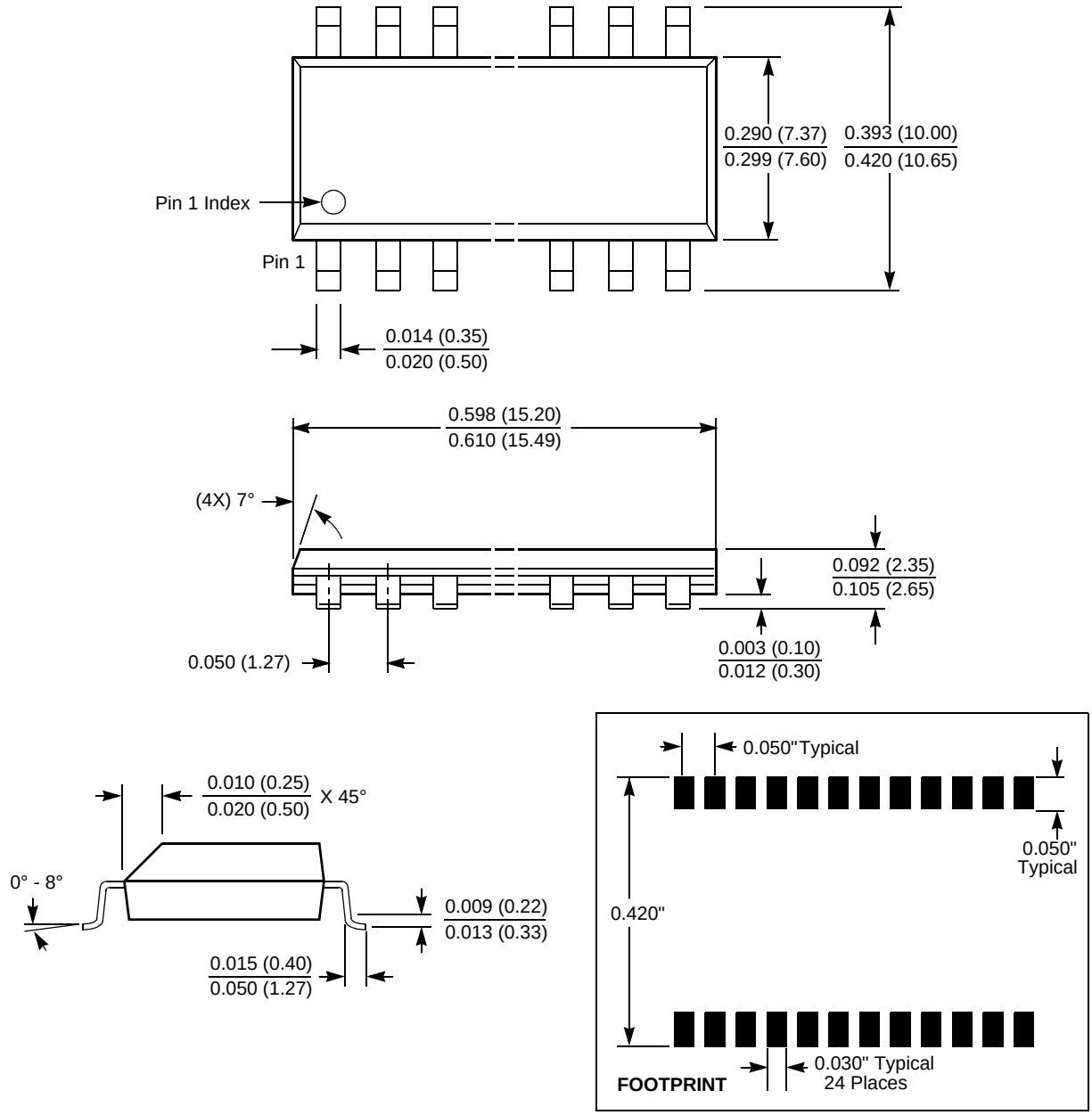
Programmable Time Delay with Memory



$$\Delta t = RC\ \ln\left(\frac{5V}{5V - V_W}\right)$$

PACKAGING INFORMATION

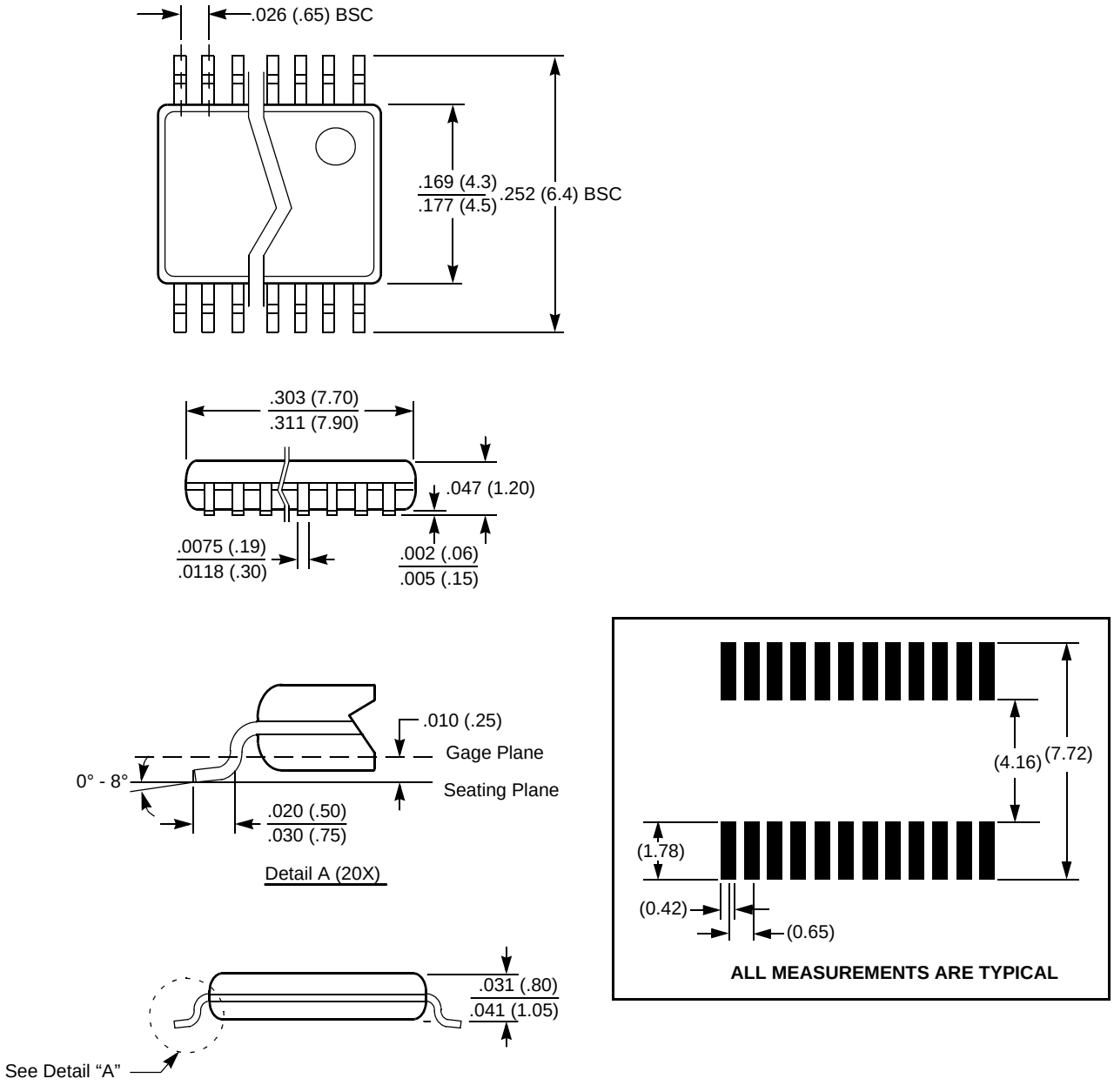
24-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

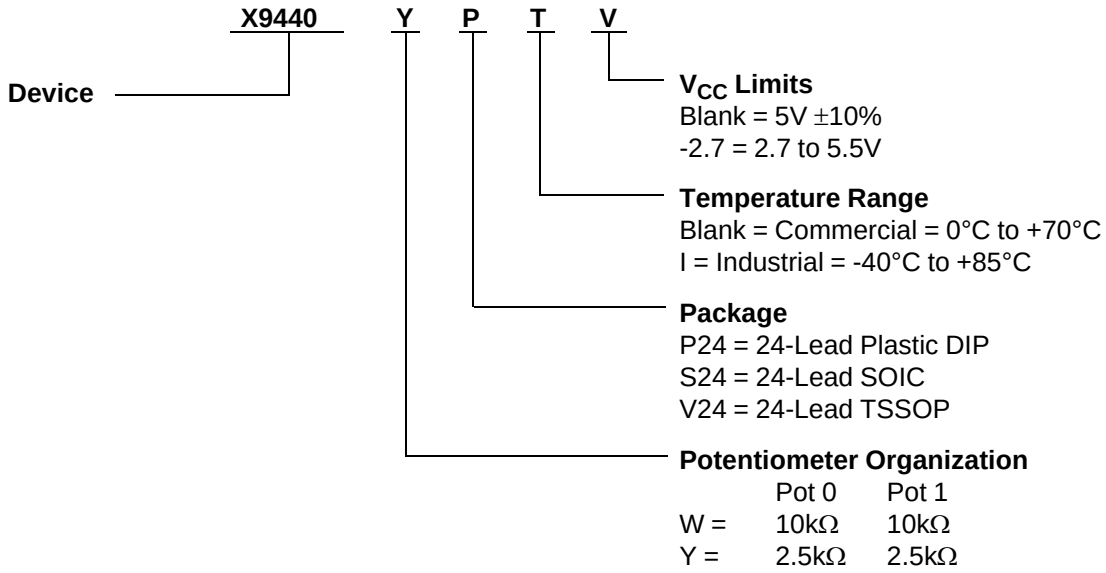
PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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