High Resolution 6 GHz Fractional-N Frequency Synthesizer

ADF4157

FEATURES

RF bandwidth to 6 GHz
25-bit fixed modulus allows subhertz frequency resolution
2.7 V to 3.3 V power supply
Separate V_P allows extended tuning voltage
Programmable charge pump currents
3-wire serial interface
Digital lock detect
Power-down mode
Pin compatible with the following frequency synthesizers:
ADF4110/ADF4111/ADF4112/ADF4113/
ADF4106/ADF4153/ADF4154/ADF4156
Cycle slip reduction for faster lock times

APPLICATIONS

Satellite communications terminals, radar equipment
Instrumentation equipment
Personal mobile radio (PMR)
Base stations for mobile radio
Wireless handsets

GENERAL DESCRIPTION

The ADF4157 is a 6 GHz fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing subhertz frequency resolution at 6 GHz. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a Σ-Δ based fractional interpolator to allow programmable fractional-N division. The INT and FRAC registers define an overall N divider, N = INT + (FRAC/2^{25}). The ADF4157 features cycle slip reduction circuitry, which leads to faster lock times without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

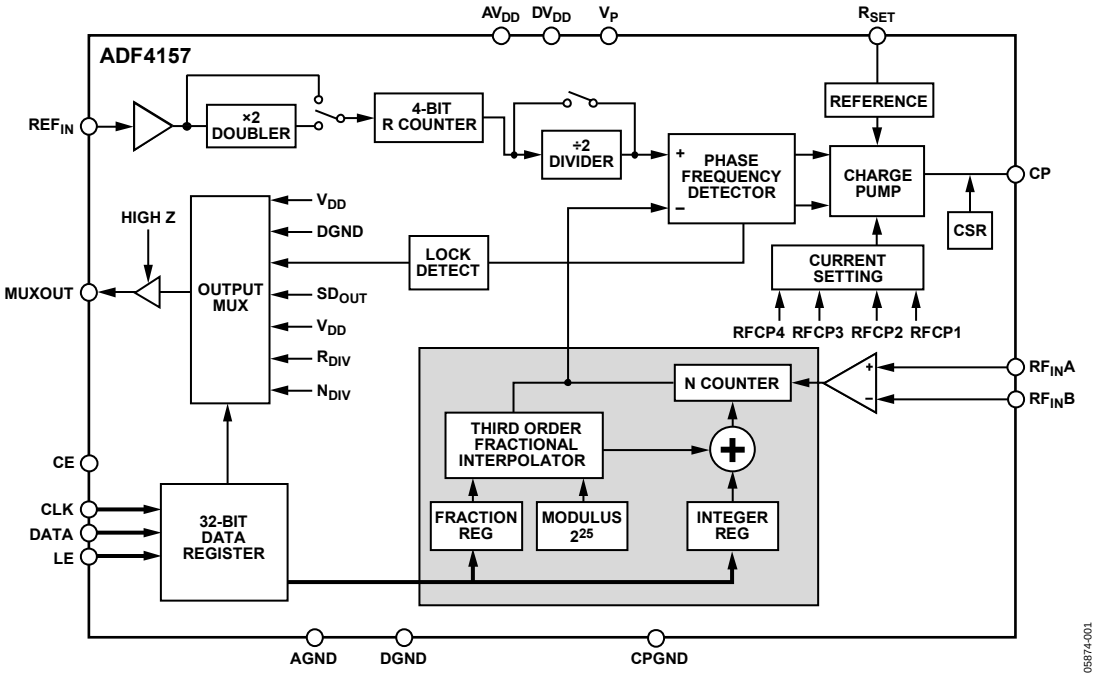


Figure 1.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2007 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

7/07—Revision 0: Initial Revision

SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
RF CHARACTERISTICS (3 V)			
RF Input Frequency (RF_{IN})	0.5/6.0	GHz min/max	−10 dBm/0 dBm min/max. For lower frequencies, ensure slew rate (SR) > 400 V/µs.
REFERENCE CHARACTERISTICS			
REF_{IN} Input Frequency	10/300	MHz min/max	For f < 10 MHz, ensure slew rate > 50 V/µs.
REF_{IN} Input Sensitivity	0.4/AV_{DD}	V p-p min/max	For 10 MHz < REF_{IN} < 250 MHz. Biased at $AV_{DD}/2$[2].
	0.7/AV_{DD}	V p-p min/max	For 250 MHz < REF_{IN} < 300 MHz. Biased at $AV_{DD}/2$[2].
REF_{IN} Input Capacitance	10	pF max	
REF_{IN} Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[3]	32	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source			Programmable.
High Value	5	mA typ	With R_{SET} = 5.1 kΩ.
Low Value	312.5	µA typ	
Absolute Accuracy	2.5	% typ	With R_{SET} = 5.1 kΩ.
R_{SET} Range	2.7/10	kΩ min/max	
I_{CP} Three-State Leakage Current	1	nA typ	Sink and source current.
Matching	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. V_{CP}	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. Temperature	2	% typ	V_{CP} = V_P/2.
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.4	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	1.4	V min	Open-drain 1 kΩ pull-up to 1.8 V.
V_{OH}, Output High Voltage	VDD − 0.4	V min	CMOS output chosen.
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA.
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	V min/V max	
I_{DD}	29	mA max	23 mA typical.
Low Power Sleep Mode	10	µA typ	
NOISE CHARACTERISTICS			
Phase Noise Figure of Merit[4]	−207	dBc/Hz typ	
ADF4157 Phase Noise Floor[5]	−137	dBc/Hz typ	@ 10 MHz PFD frequency.
	−133	dBc/Hz typ	@ 25 MHz PFD frequency.
Phase Noise Performance[6]			@ VCO output.
5800 MHz Output[7]	−87	dBc/Hz typ	@ 2 kHz offset, 25 MHz PFD frequency.

[1] Operating temperature of B version is −40°C to +85°C.
[2] AC-coupling ensures $AV_{DD}/2$ bias.
[3] Guaranteed by design. Sample tested to ensure compliance.
[4] This figure can be used to calculate phase noise for any application. Use the formula −207 + 10log(f_{PFD}) + 20logN to calculate in-band phase noise performance as seen at the VCO output.
[5] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
[6] The phase noise is measured with the EVAL-ADF4157EB1Z and the Agilent E5052A phase noise system.
[7] f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; offset frequency = 2 kHz; RF_{OUT} = 5800.25 MHz; N = 232; loop bandwidth = 20 kHz.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	25	ns min	CLOCK high duration
t_5	25	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	20	ns min	LE pulse width

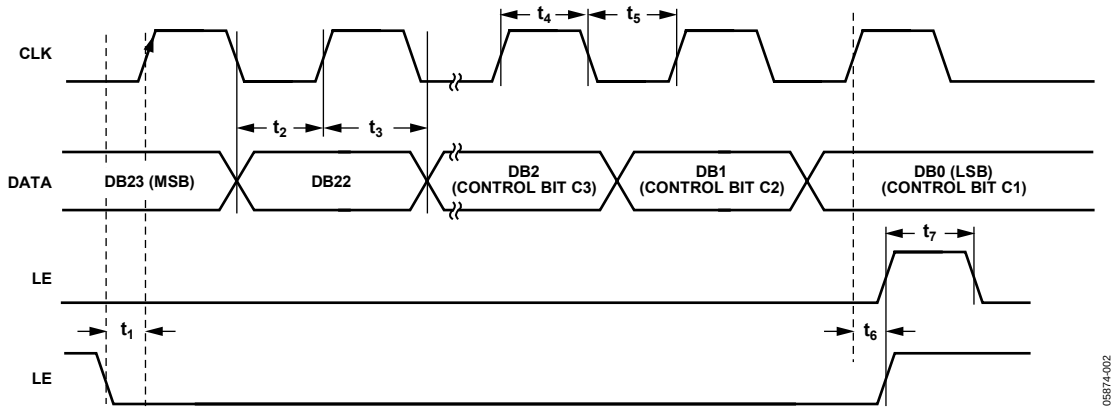


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = 0 V, V_{DD} = AV_{DD} = DV_{DD}, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
V_{DD} to V_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
TSSOP	112	°C/W
LFCSP (Paddle Soldered)	30.4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

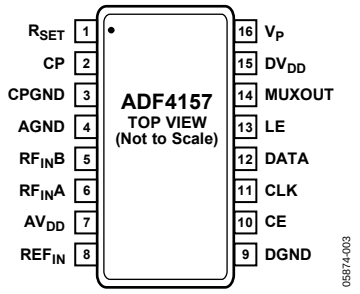


Figure 3. TSSOP Pin Configuration

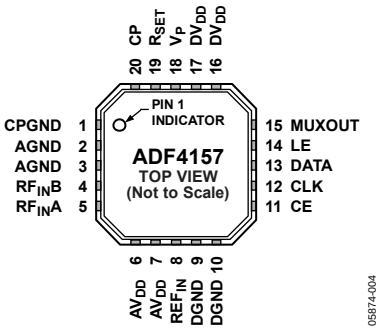


Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

TSSOP	LFCSP	Mnemonic	Description
1	19	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $I_{CPMAX} = \frac{25.5}{R_{SET}}$ where: R_{SET} = 5.1 kΩ. I_{CPMAX} = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter which, in turn, drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
7	6, 7	AV_{DD}	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV_{DD} has a value of 3 V ± 10%. AV_{DD} must have the same voltage as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the five latches, the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} has a value of 3 V ± 10%. DV_{DD} must have the same voltage as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

PFD = 25 MHz, loop bandwidth = 20 kHz, reference = 100 MHz, I_{CP} = 313 µA, phase noise measurements taken on the Agilent E5052A phase noise system.

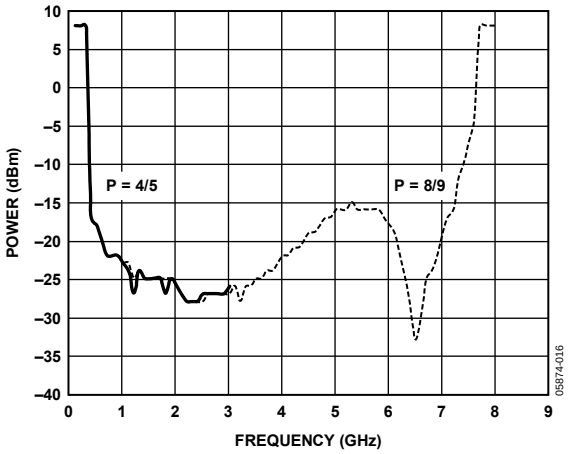


Figure 5. RF Input Sensitivity

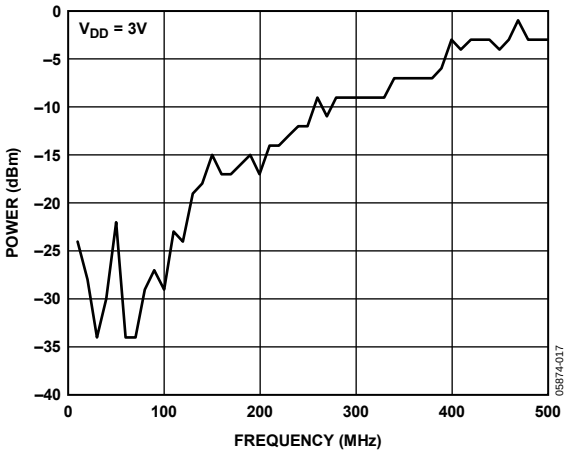


Figure 6. Reference Input Sensitivity

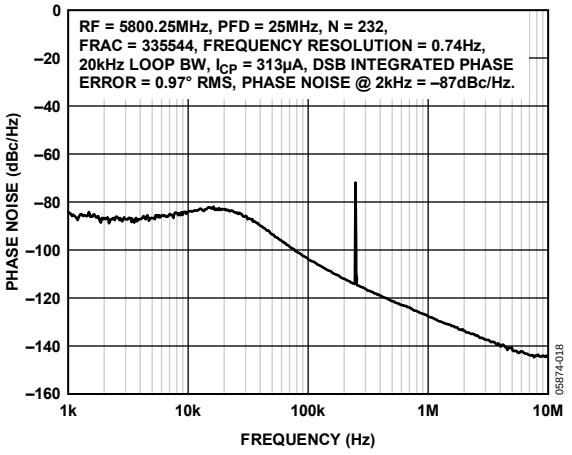


Figure 7. Phase Noise and Spurs
(Note that the 250 kHz spur is an integer boundary spur; see the Spur Mechanisms section for more information.)

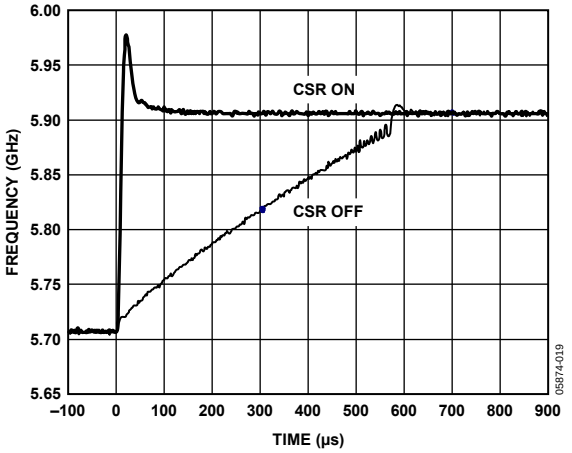


Figure 8. Lock Time for 200 MHz Jump from 5705 MHz to 5905 MHz with CSR On and Off

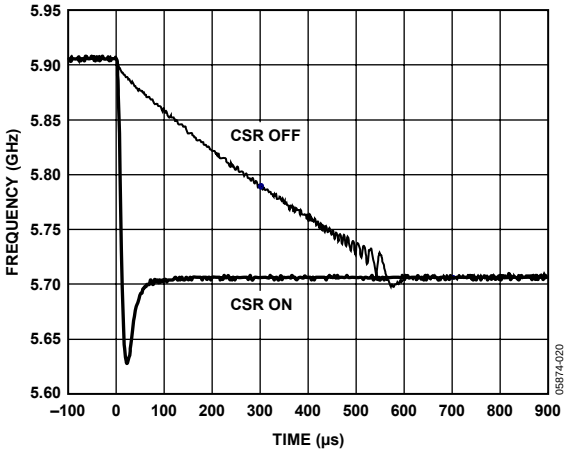


Figure 9. Lock Time for 200 MHz Jump from 5905 MHz to 5705 MHz with CSR On and Off

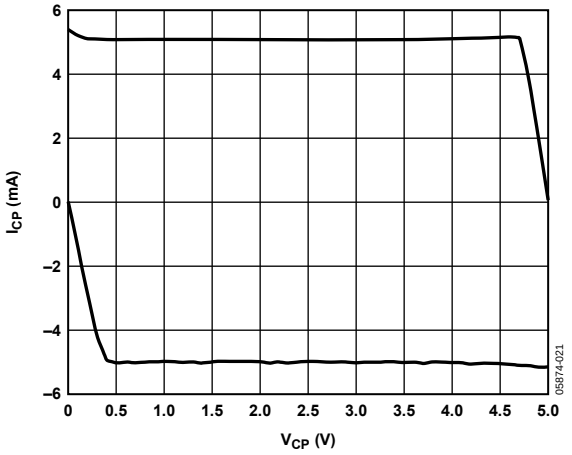


Figure 10. Charge Pump Output Characteristics, Pump Up and Pump Down

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 11. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

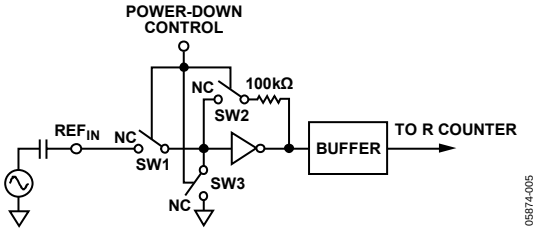


Figure 11. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 12. It is followed by a 2-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

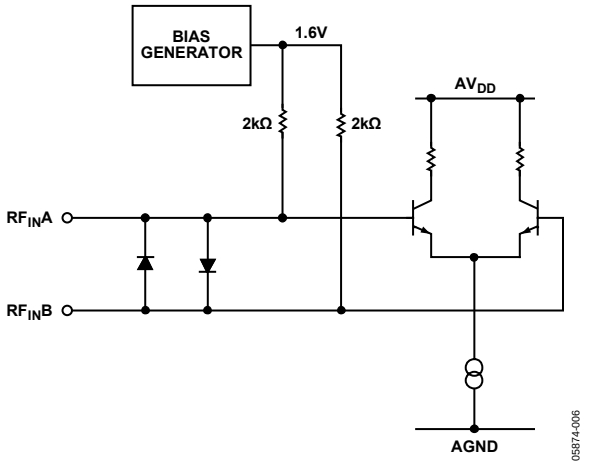


Figure 12. RF Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

25-BIT FIXED MODULUS

The ADF4157 has a 25-bit fixed modulus. This allows output frequencies to be spaced with a resolution of

$$f_{RES} = f_{PFD}/2^{25}$$

where f_{PFD} is the frequency of the phase frequency detector (PFD). For example, with a PFD frequency of 10 MHz, frequency steps of 0.298 Hz are possible.

INT, FRAC, AND R RELATIONSHIP

The INT and FRAC values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (1)$$

where:

RF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO).

INT is the preset divide ratio of the binary 12-bit counter (23 to 4095).

FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1+T))] \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit.

R is the preset divide ratio of the binary 5-bit programmable reference counter (1 to 32).

T is the REF_{IN} divide-by-2 bit (0 or 1).

RF R COUNTER

The 5-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

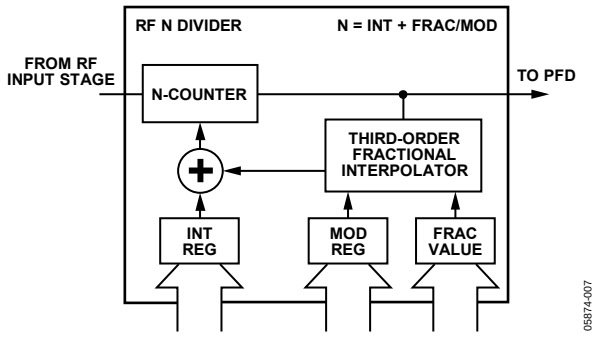


Figure 13. RF N Divider

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and the N counter and produces an output proportional to the phase and frequency difference between them. Figure 14 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

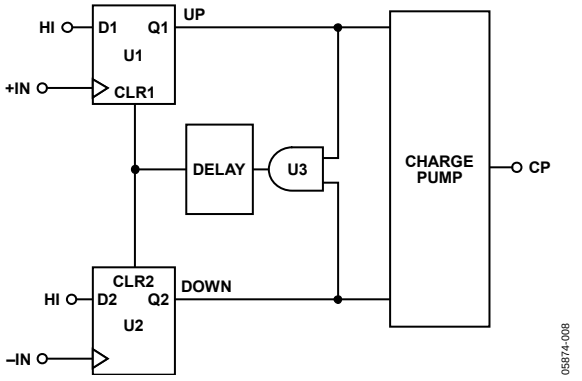


Figure 14. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4157 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M4, M3, M2, and M1 (see Figure 17). Figure 15 shows the MUXOUT section in block diagram form.

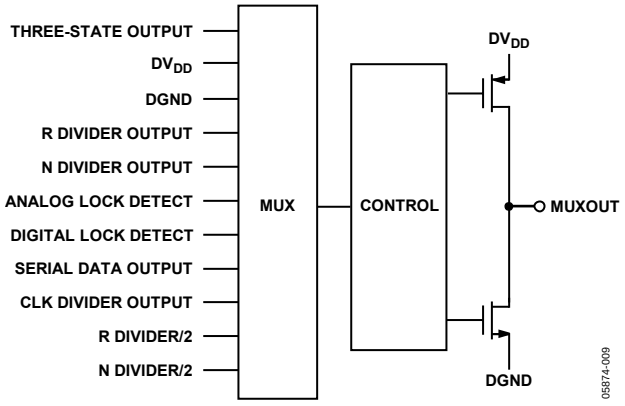


Figure 15. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4157 digital section includes a 5-bit RF R counter, a 12-bit RF N counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of five latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These are the three LSBs, DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 16 shows a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 16 through Figure 21 show how to set up the program modes in the ADF4157.

Several settings in the ADF4157 are double-buffered. These include the LSB FRAC value, R counter value, reference doubler, and current setting. This means that two events have to occur before the part uses a new value of any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, updating the fractional value can involve a write to the 13 LSB bits in R1 and the 12 MSB bits in R0. R1 should be written to first, followed by the write to R0. The frequency change begins after the write to R0. Double buffering ensures that the bits written to in R1 do not take effect until after the write to R0.

Table 6. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register R0
0	0	1	Register R1
0	1	0	Register R2
0	1	1	Register R3
1	0	0	Register R4

REGISTER MAPS

FRAC/INT REGISTER (R0)

RESERVED	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

LSB FRAC REGISTER (R1)

RESERVED				13-BIT LSB FRACTIONAL VALUE (FRAC) (DBB)													RESERVED												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(0)	C1(1)

R DIVIDER REGISTER (R2)

RESERVED	RESERVED	CSR EN	CURRENT SETTING DBB				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	5-BIT R-COUNTER DBB					RESERVED												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	C1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED																	SD RESET	RESERVED							LDP	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	U12	0	0	0	0	0	0	U11	U10	U9	U8	U7	C3(0)	C2(1)	C1(1)

TEST REGISTER (R4)

RESERVED																													CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(0)	C1(0)

NOTES
1. DBB = DOUBLE BUFFERED BIT(S).

05874-010

Figure 16. Register Summary

FRAC/INT REGISTER (R0) MAP

With R0[2, 1, 0] set to [0, 0, 0], the on-chip Frac/Int register is programmed as shown in Figure 17.

Reserved Bit

The reserved bit should be set to 0 for normal operation.

MUXOUT

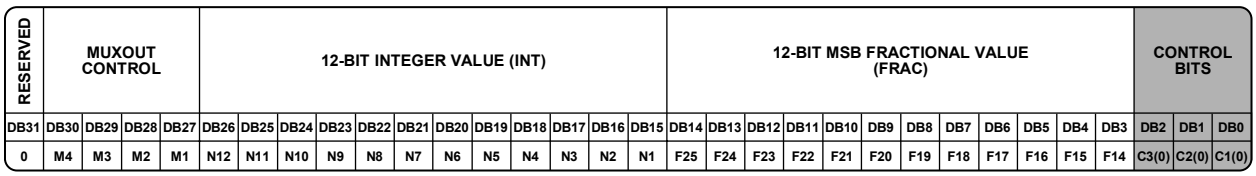
The on-chip multiplexer is controlled by DB[30], DB[29], DB[28] and DB[27] on the ADF4157. See Figure 17 for the truth table.

12-Bit INT Value

These twelve bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 1. See the INT, FRAC, and R Relationship section for more information.

12-Bit MSB FRAC Value

These twelve bits, along with Bits DB[27:15] in the LSB FRAC register (R1), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 1. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits DB[27:15] in the LSB FRAC register (R1) are the least significant bits (LSB). See the RF Synthesizer: A Worked Example section for more information.



M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R DIVIDER OUTPUT
0	1	0	0	N DIVIDER OUTPUT
0	1	0	1	RESERVED
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	CLK DIVIDER
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	R DIVIDER/2
1	1	1	0	N DIVIDER/2
1	1	1	1	RESERVED

F12	F11	.....	F2	F1	MSB FRACTIONAL VALUE (FRAC)*
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	4092
1	1	.....	0	1	4093
1	1	.....	1	0	4094
1	1	.....	1	1	4095

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER 0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER 1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	0	0	0	1	0	1	1	1	23
0	0	0	0	0	0	0	1	1	0	0	0	24
0	0	0	0	0	0	0	1	1	0	0	1	25
0	0	0	0	0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

05874-011

Figure 17. FRAC/INT Register (R0) Map

LSB FRAC REGISTER (R1) MAP

With R1[2, 1, 0] set to [0, 0, 1], the on-chip LSB FRAC register is programmed as shown in Figure 18.

13-Bit LSB FRAC Value

These thirteen bits, along with Bits DB[14:3] in the INT/FRAC register (R0), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 1. These 13 bits are the least significant bits of the 25-bit FRAC value, and Bits DB[14:3] in the INT/FRAC register are the most significant bits. See the RF Synthesizer: A Worked Example section for more information.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

RESERVED				13-BIT LSB FRACTIONAL VALUE (FRAC)												RESERVED												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(0)	C1(1)

F25	F24	.....	F14	F13	LSB FRACTIONAL VALUE (FRAC)*
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	8188
1	1	.....	0	1	8189
1	1	.....	1	0	8190
1	1	.....	1	1	8191

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER 0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER 1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

05874-012

Figure 18. LSB FRAC Register (R1) Map

R DIVIDER REGISTER (R2) MAP

With R1[2, 1, 0] set to [0, 1, 0], the on-chip R divider register is programmed as shown in Figure 19.

CSR Enable

Setting this bit to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the PFD must have a 50% duty cycle in order for cycle slip reduction to work. In addition, the charge pump current setting must be set to a minimum. See the Cycle Slip Reduction for Faster Lock Times section for more information.

Note also that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is set to negative.

Charge Pump Current Setting

DB[27], DB[26], DB[25], and DB[24] set the charge pump current setting. This should be set to the charge pump current that the loop filter is designed with (see Figure 19).

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4157 above 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value.

With P = 4/5, N_{MIN} = 23.

With P = 8/9, N_{MIN} = 75.

RDIV2

Setting this bit to 1 inserts a divide-by-2 toggle flip flop between the R counter and the PFD. This can be used to provide a 50% duty cycle signal at the PFD for use with cycle slip reduction.

Reference Doubler

Setting DB[20] to 0 feeds the REF_{IN} signal directly to the 5-bit RF R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 5-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising edge and falling edge of REF_{IN} become active edges at the PFD input.

The maximum allowed REF_{IN} frequency when the doubler is enabled is 30 MHz.

5-Bit R Counter

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 32 are allowed.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

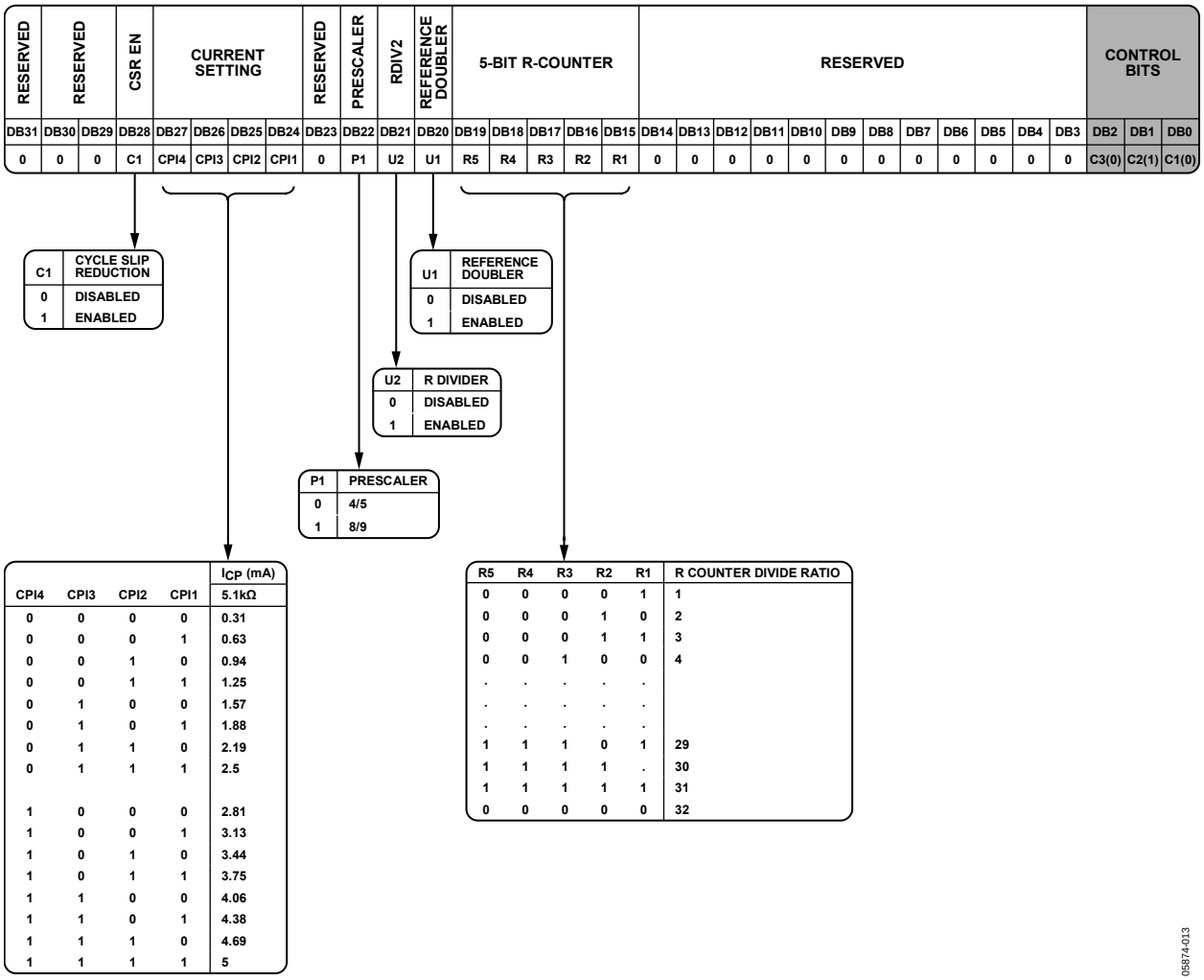


Figure 19. R Divider Register (R2) Map

FUNCTION REGISTER (R3) MAP

With R2[2, 1, 0] set to [0, 1, 1], the on-chip function register is programmed as shown in Figure 20.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Σ-Δ Reset

For most applications, DB14 should be set to 0. When DB14 is set to 0, the Σ-Δ modulator is reset on each write to Register 0. If it is not required that the Σ-Δ modulator be reset on each Register 0 write, this bit should be set to 1.

Lock Detect Precision (LDP)

When DB[7] is programmed to 0, 24 consecutive PFD cycles of 15 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector Polarity

DB[6] in the ADF4157 sets the phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

RF Power-Down

DB[5] on the ADF4157 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation.

While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

RF Charge Pump Three-State

DB[4] puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

RF Counter Reset

DB[3] is the RF counter reset bit for the ADF4157. When this is 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be 0.

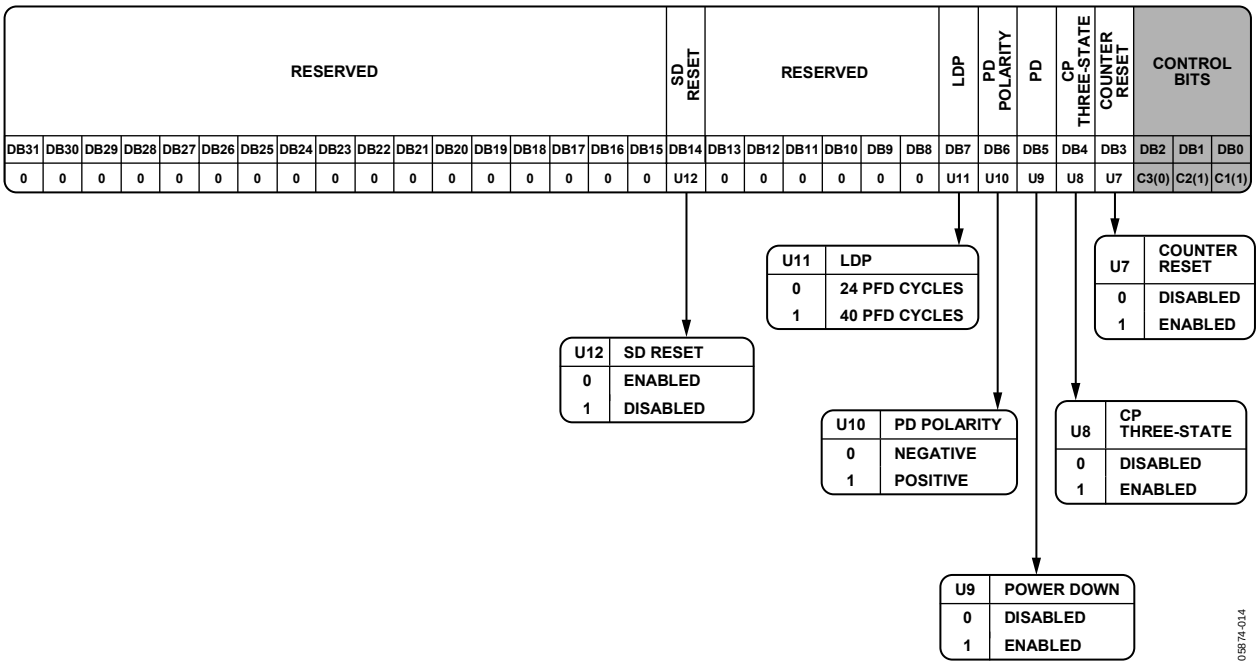


Figure 20. Function Register (R3) Map

TEST REGISTER (R4) MAP

With R3[2, 1, 0] set to [1, 0, 0], the on-chip test register (R4) is programmed as shown in Figure 21.

Reserved Bits

DB[31:3] should be set to 0 in this register.

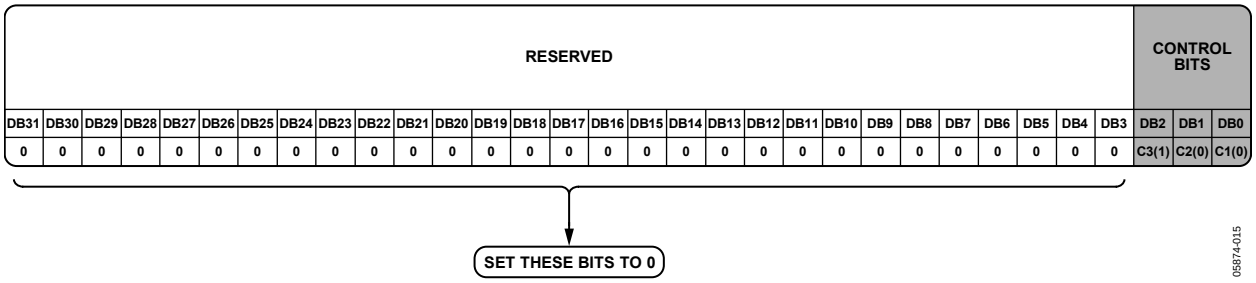


Figure 21. Test Register (R4) Map

APPLICATIONS INFORMATION

INITIALIZATION SEQUENCE

After powering up the part, this programming sequence must be followed:

1. Test Register (R4)
2. Function Register (R3)
3. R Divider Register (R2)
4. LSB FRAC Register (R1)
5. FRAC/INT Register (R0)

RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer should be programmed:

$$RF_{OUT} = [N + (FRAC/2^{25})] \times [f_{PFD}] \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
N is the integer division factor.
$FRAC$ is the fractionality.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide-by-2 bit (0 or 1).

For example, in a system where a 5.8002 GHz RF frequency output (RF_{OUT}) is required and a 10 MHz reference frequency input (REF_{IN}) is available, the frequency resolution is

$$f_{RES} = REF_{IN}/2^{25}$$
$$f_{RES} = 10 \text{ MHz}/2^{25} = 0.298 \text{ Hz}$$

From Equation 4,

$$f_{PFD} = [10 \text{ MHz} \times (1 + 0)/1] = 10 \text{ MHz}$$
$$5.8002 \text{ GHz} = 10 \text{ MHz} \times (N + FRAC/2^{25})$$

Calculating N and FRAC values,

$$N = int(RF_{OUT}/f_{PFD}) = 580$$
$$FRAC = F_{MSB} \times 2^{13} + F_{LSB}$$
$$F_{MSB} = int(((RF_{OUT}/f_{PFD}) - \text{N}) \times 2^{12}) = 81$$
$$F_{LSB} = int(((((RF_{OUT}/f_{PFD}) - \text{N}) \times 2^{12}) - F_{MSB}) \times 2^{13}) = 7537$$

where:
F_{MSB} is the 12-bit MSB FRAC value in Register R0.
F_{LSB} is the 13-bit LSB FRAC value in Register R1.
$int()$ makes an integer of the argument in brackets.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot be operated above 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

In fast-locking applications, a wide loop filter bandwidth is required for fast frequency acquisition, resulting in increased integrated phase noise and reduced spur attenuation. Using cycle slip reduction, the loop bandwidth can be kept narrow to reduce integrated phase noise and attenuate spurs while still realizing fast lock times.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared to the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction, slowing down the lock time dramatically. The ADF4157 contains a cycle slip reduction circuit to extend the linear range of the PFD, allowing faster lock times without loop filter changes.

When the ADF4157 detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Stability is maintained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4157 turns on another charge pump cell. This continues until the ADF4157 detects that the VCO frequency has gone past the desired frequency. It then begins to turn off the extra charge pump cells one by one until they are all turned off and the frequency is settled.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB28 in the R Divider register (R2) to 1 enables cycle slip reduction. Note that a 45% to 55% duty cycle is needed on the signal at the PFD in order for CSR to operate correctly. The reference divide-by-2 flip-flop can help to provide a 50% duty cycle at the PFD. For example, if a 100 MHz reference frequency is available, and the user wants to run the PFD at 10 MHz, setting the R divide factor to 10 results in a 10 MHz PFD signal that is not 50% duty cycle. By setting the R divide factor to 5 and enabling the reference divide-by-2 bit, a 50% duty cycle 10 MHz signal can be achieved.

Note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is set to negative.

SPUR MECHANISMS

The fractional interpolator in the ADF4157 is a third-order Σ-Δ modulator (SDM) with a 25-bit fixed modulus (MOD). The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD. The various spur mechanisms possible with fractional-N synthesizers, and how they affect the ADF4157, are discussed in this section.

Fractional Spurs

In most fractional synthesizers, fractional spurs can appear at the set channel spacing of the synthesizer. In the ADF4157, these spurs do not appear. The high value of the fixed modulus in the ADF4157 makes the Σ-Δ modulator quantization error spectrum look like broadband noise, effectively spreading the fractional spurs into noise.

Integer Boundary Spurs

Interactions between the RF VCO frequency and the PFD frequency can lead to spurs known as integer boundary spurs. When these frequencies are not integer related (which is the purpose of the fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the PFD and the VCO frequency.

These spurs are named integer boundary spurs because they are more noticeable on channels close to integer multiples of the PFD where the difference frequency can be inside the loop bandwidth. These spurs are attenuated by the loop filter.

Figure 7 shows an integer boundary spur. The RF frequency is 5800.25 MHz, and the PFD frequency is 25 MHz. The integer boundary spur is 250 kHz from the carrier at an integer times the PFD frequency (232 × 25 MHz = 5800 MHz). The spur also appears on the upper sideband.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is the feedthrough of low levels of on-chip reference switching noise out through the RF_{IN} pin back to the VCO, resulting in reference spur levels as high as –90 dBc. Care should be taken in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

LOW FREQUENCY APPLICATIONS

The specification on the RF input is 0.5 GHz minimum; however, RF frequencies lower than this can be used providing the minimum slew rate specification of 400 V/µs is met. An appropriate LVDS driver can be used to square up the RF signal before it is fed back to the ADF4157 RF input. The FIN1001 from Fairchild Semiconductor is one such LVDS driver.

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user implement PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL™ software. The software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

INTERFACING

The ADF4157 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When latch enable (LE) is high, the 29 bits that have been clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz.

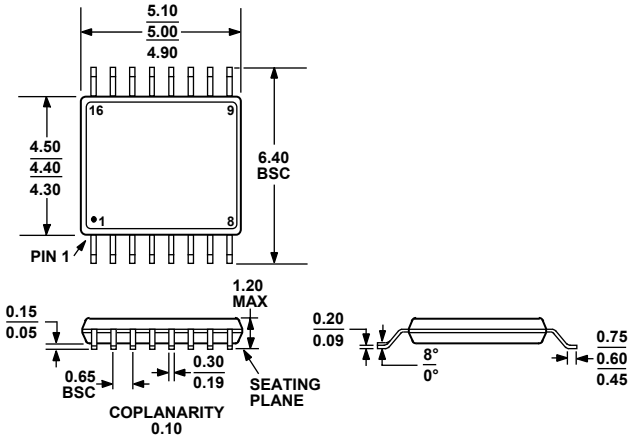
PCB DESIGN GUIDELINES FOR THE CHIP SCALE PACKAGE

The lands on the chip scale package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

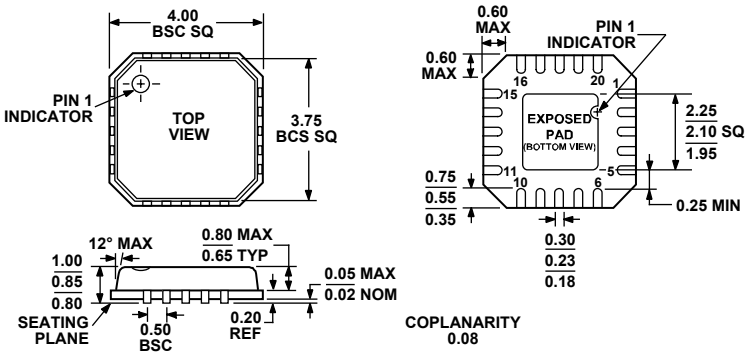
Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 23. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Description	Temperature Range	Package Option
ADF4157BRUZ[1]	16-Lead Thin Shrink Small Outline Package [TSSOP]	−40°C to +85°C	RU-16
ADF4157BRUZ-RL[1]	16-Lead Thin Shrink Small Outline Package [TSSOP]	−40°C to +85°C	RU-16
ADF4157BRUZ-RL7[1]	16-Lead Thin Shrink Small Outline Package [TSSOP]	−40°C to +85°C	RU-16
ADF4157BCPZ[1]	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	−40°C to +85°C	CP-20-1
ADF4157BCPZ-RL[1]	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	−40°C to +85°C	CP-20-1
ADF4157BCPZ-RL7[1]	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	−40°C to +85°C	CP-20-1
EVAL-ADF4157EB1Z[1]	Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru