HCPL-3150 (Single Channel), HCPL-315J (Dual Channel)

0.5 Amp Output Current IGBT Gate Drive Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-315X consists of an LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200 V/50 A. For IGBTs with higher ratings, the HCPL-3150/315J can be used to drive a discrete power stage which drives the IGBT gate.

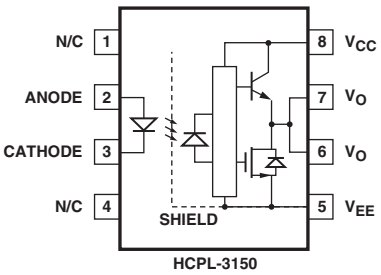
Applications

- Isolated IGBT/MOSFET gate drive
- AC and brushless dc motor drives
- Industrial inverters
- Switch Mode Power Supplies (SMPS)
- Uninterruptable Power Supplies (UPS)

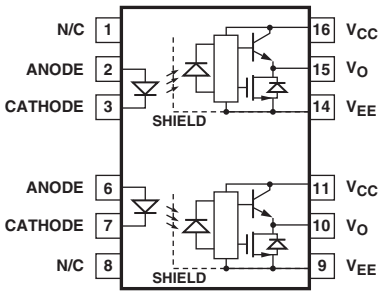
Features

- 0.6A maximum peak output current
- 0.5 A minimum peak output current
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- 1.0 V maximum low level output voltage (V_{OL}) eliminates need for negative gate drive
- I_{CC} = 5 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} range: 15 to 30 volts
- 0.5 µs maximum propagation delay
- +/– 0.35 µs maximum delay between devices/ channels
- Industrial temperature range: -40°C to 100°C
- HCPL-315J: channel one to channel two output isolation = 1500 Vrms/1 min.
- Safety and regulatory approval:
  UL recognized (UL1577),
  3750 Vrms/1 min (HCPL-3150)
  5000 Vrms/1 min (HCPL-315J)
  IEC/EN/DIN EN 60747-5-2 approved
  V_{IORM} = 630 V_{peak} (HCPL-3150 option 060 only)
  V_{IORM} = 1230 V_{peak} (HCPL-315J) CSA certified

Functional Diagram



HCPL-3150



HCPL-315J

TRUTH TABLE

LED	V_{CC} - V_{EE} "Positive Going" (i.e., Turn-On)	V_{CC} - V_{EE} "Negative-Going" (i.e., Turn-Off)	V_O
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1 µF bypass capacitor must be connected between the V_{CC} and V_{EE} pins for each channel.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide: Invertor Gate Drive Optoisolators

Package Type	8-Pin DIP (300 mil)				Widebody (400 mil)	Small Outline SO-16		
Part Number	HCPL-3150	HCPL-3120	HCPL-J312	HCPL-J314	HCNW-3120	HCPL-315J	HCPL-316J	HCPL-314J
Number of Channels	1	1	1	1	1	2	1	2
IEC/EN/DIN EN 60747-5-2 Approvals	V_{IORM} 630 Vpeak Option 060		V_{IORM} 1230Vpeak		V_{IORM} 1414 Vpeak	V_{IORM} 1230 Vpeak		
UL Approval	5000 Vrms/1 min.		5000 Vrms/1 min.		5000 Vrms/1min.	5000 Vrms/1 min.		
Output Peak Current	0.5A	2A	2A	0.4A	2A	0.5A	2A	0.4A
CMR (minimum)	15 kV/µs			10 kV/µs	15 kV/µs			10 kV/µs
UVLO	Yes			No	Yes			No
Fault Status	No						Yes	No

Ordering Information

HCPL-3150 is UL Recognized with 3750 Vrms for 1 minute per UL1577. HCPL-315J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	Non RoHS Compliant						
HCPL-3150	-000E	No option	300 mil DIP-8					50 per tube
	-300E	#300		x	x			50 per tube
	-500E	#500		x	x	x		1000 per reel
	-060E	#060					x	50 per tube
	-360E	#360		x	x		x	50 per tube
	-560E	#560		x	x	x	x	1000 per reel
HCPL-315J	-000E	No option	SO-16	x			x	45 per tube
	-500E	#500		x		x	x	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-3150-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Example 2:

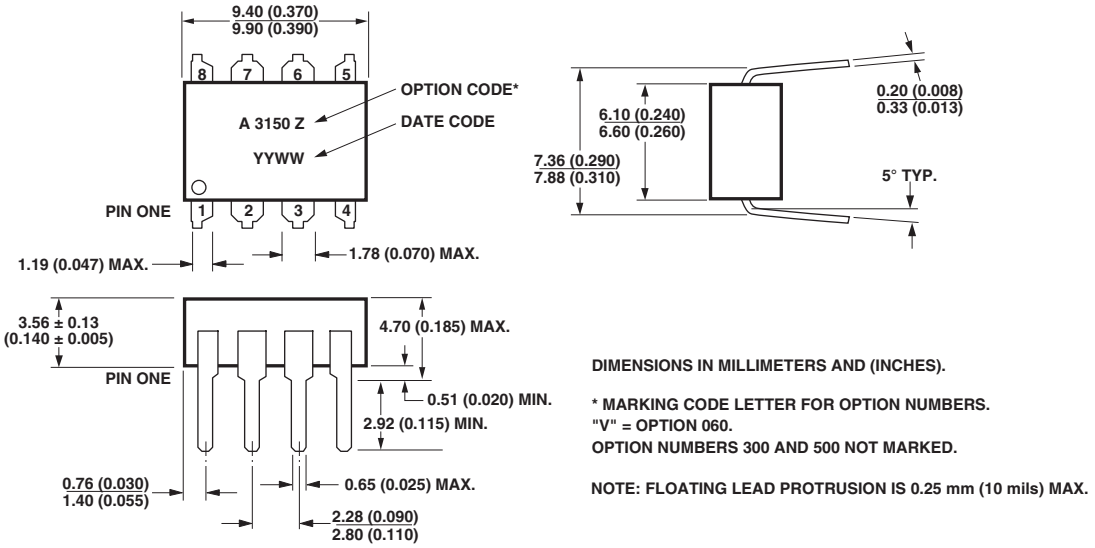
HCPL-3150 to order product of 300 mil DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawings

Standard DIP Package



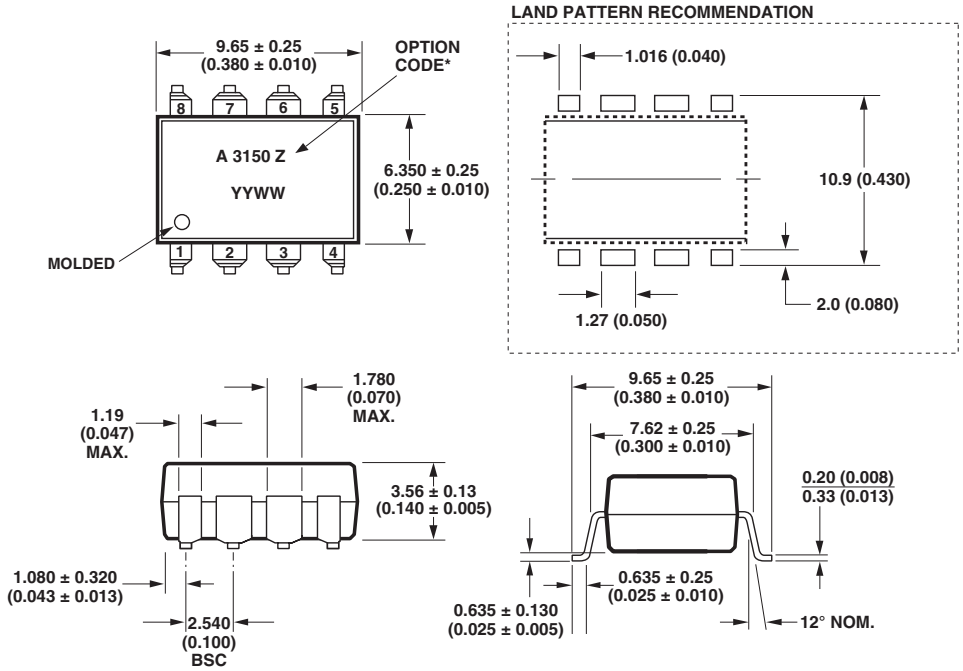
DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060.
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Package Outline Drawings

Gull-Wing Surface-Mount Option 300



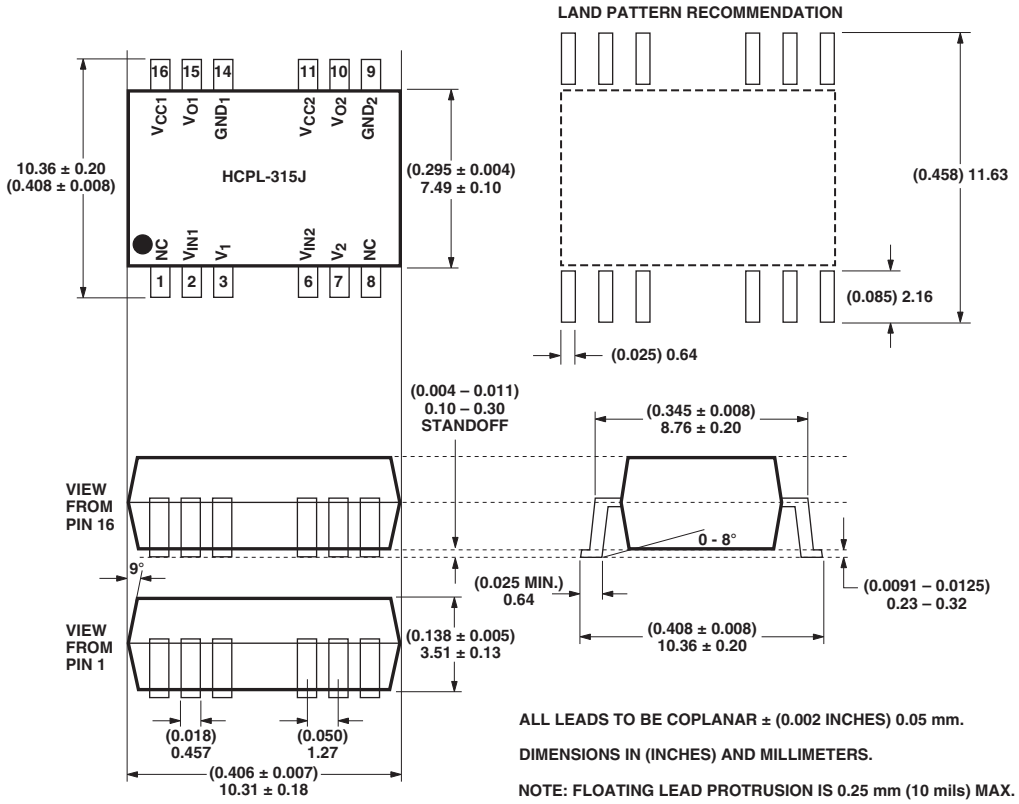
DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060.
OPTION NUMBERS 300 AND 500 NOT MARKED.

16 - Lead Surface Mount



ALL LEADS TO BE COPLANAR ± (0.002 INCHES) 0.05 mm.

DIMENSIONS IN (INCHES) AND MILLIMETERS.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The HCPL-3150 and HCPL-315J have been approved by the following organizations:

UL
Recognized under UL 1577, Component Recognition Program, File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2
Approved under:
IEC 60747-5-5:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01.
(Option 060 and HCPL-315J only)

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics

Description	Symbol	HCPL-3150#060	HCPL-315J	Unit
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 150 Vrms			I - IV	
for rated mains voltage ≤ 300 Vrms		I - IV	I - IV	
for rated mains voltage ≤ 600 Vrms		I - III	I - IV	
for rated mains voltage ≤ 1000Vrms		I - II	I-III	
Climatic Classification	55/100/21	55/100/21		
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	1230	Vpeak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1181	2306	Vpeak
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	945	1968	Vpeak
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	Vpeak
Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure, Also See Figure 37, Thermal Derating Curve.				
Case Temperature T_S	175	175	°C	
Input Current	$I_{S, INPUT}$	230	400	mA
Output Power	$P_{S, OUTPUT}$	600	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description of Method a and Method b partial discharge test profiles.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation and Safety Related Specifications

Parameter Symbol		HCPL-3150	HCPL-315J	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	8.3	mm	Measured from input terminals to output erminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	≥0.5	mm	Through insulation distance conductor to conductor.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	≥175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance wtih CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1, 16
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	Volts	
"High" Peak Output Current	$I_{OH(PEAK)}$		0.6	A	2, 16
"Low" Peak Output Current	$I_{OL(PEAK)}$		0.6	A	2, 16
Supply Voltage	$(V_{CC} - V_{EE})$	0	35	Volts	
Output Voltage	$V_{O(PEAK)}$	0	V_{CC}	Volts	
Output Power Dissipation	P_O		250	mW	3, 16
Total Power Dissipation	P_T		295	mW	4, 16
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	Volts
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V
Operating Temperature	T_A	-40	100	°C

Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground, each channel) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.1	0.4		A	V_O = (V_{CC} - 4 V) 2, 3,	5	
		0.5				V_O = (V_{CC} - 15 V)	17	2
Low Level Output Current	I_{OL}	0.1	0.6		A	V_O = (V_{EE} + 2.5 V)	5, 6,	5
		0.5				V_O = (V_{EE} + 15 V)	18	2
High Level Output Voltage	V_{OH}	(V_{CC} - 4)	(V_{CC} - 3)		V	I_O = -100 mA	1, 3, 19	6, 7
Low Level Output Voltage	V_{OL}		0.4	1.0	V	I_O = 100 mA	4, 6, 20	
High Level Supply Current	I_{CCH}		2.5	5.0	mA	Output Open, 7, 8 I_F = 7 to 16 mA	16	
Low Level Supply Current	I_{CCL}		2.7	5.0	mA	Output Open, V_F = -3.0 to +0.8 V		
Threshold Input Current Low to High	I_{FLH}		2.2	5.0	mA	HCPL-3150 I_O = 0 mA,	9, 15,	
			2.6	6.4		HCPL-315J V_O > 5 V	21	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	HCPL-3150 I_F = 10 mA	16	
			1.6	1.95		HCPL-315J		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	HCPL-3150 I_R = 10 µA		
		3				HCPL-315J I_R = 10 µA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	11.0	12.3	13.5	V	V_O > 5 V,	22,	
	V_{UVLO-}	9.5	10.7	12.0		I_F = 10 mA	36	
UVLO Hysteresis	$UVLO_{HYS}$		1.6		V			

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground, each channel) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 47 Ω, Cg = 3 nF, f = 10 kHz, Duty Cycle = 50%	10, 11, 12, 13, 14, 23	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.3	0.50	µs			
Pulse Width Distortion	PWD			0.3	µs			15
Propagation Delay Difference Between Any Two Parts or Channels	PDD (t_{PHL} - t_{PLH})	-0.35		0.35	µs		34, 36	10
Rise Time	t_r		0.1		µs		23	
Fall Time	t_f		0.1		µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$		0.8		µs	V_O > 5 V, I_F = 10 mA	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	V_O < 5 V, I_F = 10 mA		
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, I_F = 10 to 16 mA, V_{CM} = 1500 V, V_{CC} = 30 V	24	11, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_F = 0 V, V_{CC} = 30 V		11, 13

Package Characteristics (each channel, unless otherwise specified)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	HCPL-3150	3750			Vrms	RH < 50%, t = 1 min., T_A = 25°C		8, 9
		HCPL-315J	5000						
Output-Output Momentary Withstand Voltage**	V_{O-O}	HCPL-315J	1500			Vrms	RH < 50% t = 1 min., T_A = 25°C		17
Resistance (Input - Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V_{DC}		9
Capacitance (Input - Output)	C_{I-O}	HCPL-3150		0.6		pF	f = 1 MHz		
		HCPL-315J		1.3					
LED-to-Case Thermal Resistance	θ_{LC}	HCPL-3150		391		°C/W	Thermocouple located at center underside of package	28	18
LED-to-Detector Thermal Resistance	θ_{LD}	HCPL-3150		439		°C/W			
Detector-to-Case Thermal Resistance	θ_{DC}	HCPL-3150		119		°C/W			

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

**The Input-Output/Output-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output/output-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.5 A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL1577, each HCPL-3150 optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms (≥ 6000 Vrms for the HCPL-315J) for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. The difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test condition.
11. Pins 1 and 4 (HCPL-3150) and pins 3 and 4 (HCPL-315J) need to be connected to LED common.
12. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15.0 V).
13. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
14. This load condition approximates the gate load of a 1200 V/25 A IGBT.
15. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
16. Each channel.
17. Device considered a two terminal device: Channel one output side pins shorted together, and channel two output side pins shorted together.
18. See the thermal model for the HCPL-315J in the application section of this data sheet.

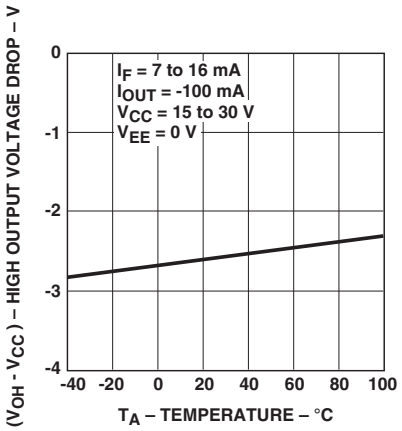


Figure 1. V_{OH} vs. Temperature.

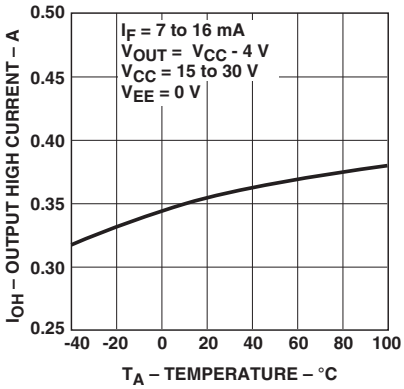


Figure 2. I_{OH} vs. Temperature.

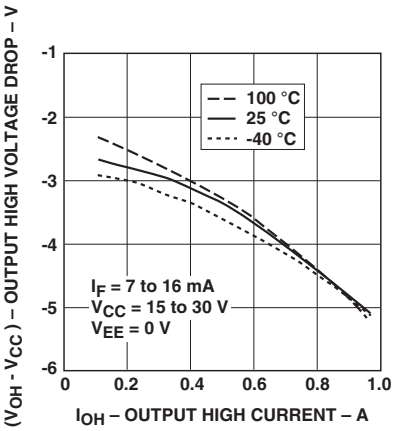


Figure 3. V_{OH} vs. I_{OH}.

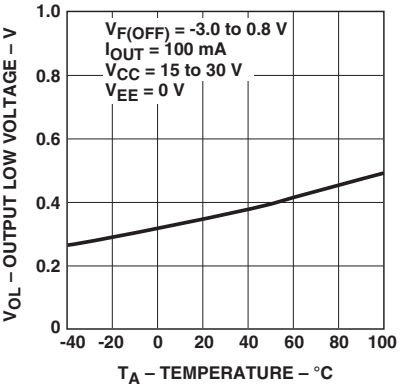


Figure 4. V_{OL} vs. Temperature.

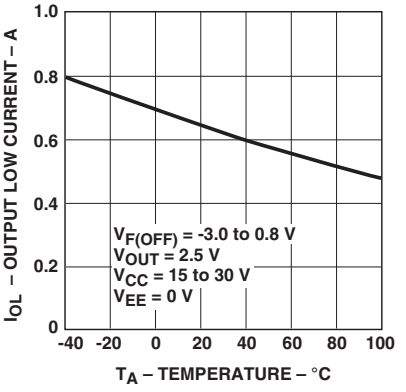


Figure 5. I_{OL} vs. Temperature.

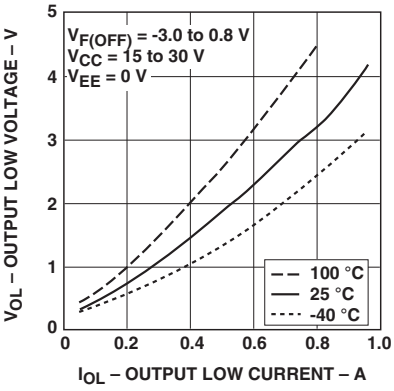


Figure 6. V_{OL} vs. I_{OL}.

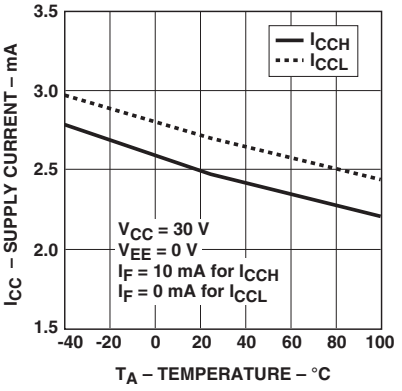


Figure 7. I_{CC} vs. Temperature.

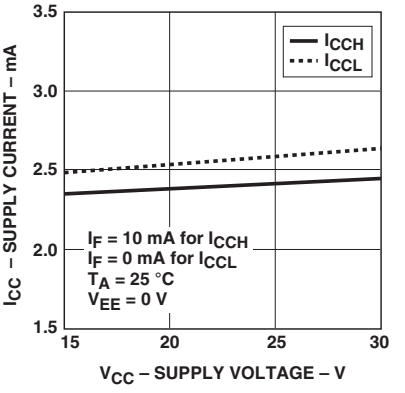


Figure 8. I_{CC} vs. V_{CC}.

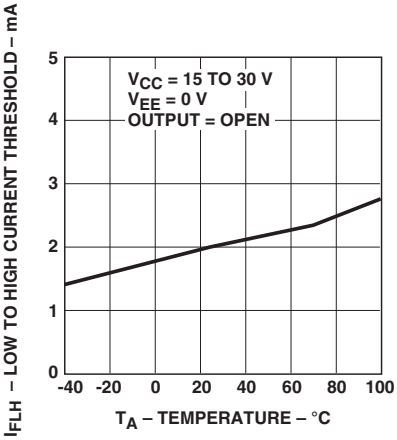


Figure 9. I_{FLH} vs. Temperature.

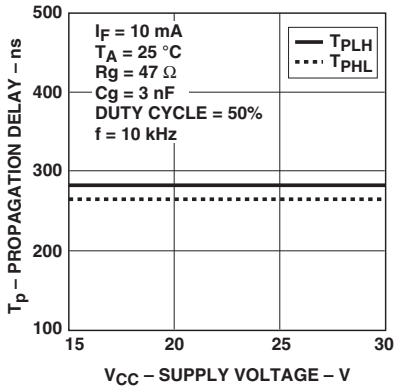


Figure 10. Propagation Delay vs. V_{cc}.

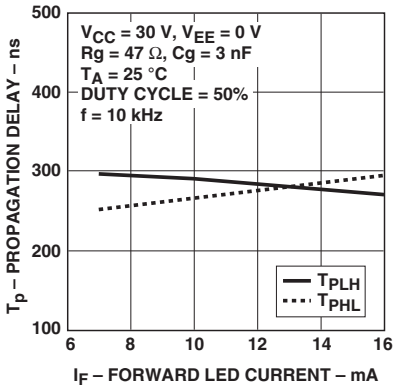


Figure 11. Propagation Delay vs. I_F.

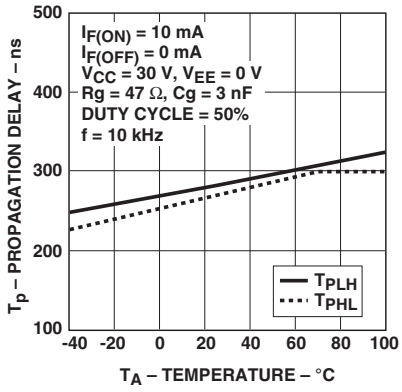


Figure 12. Propagation Delay vs. Temperature.

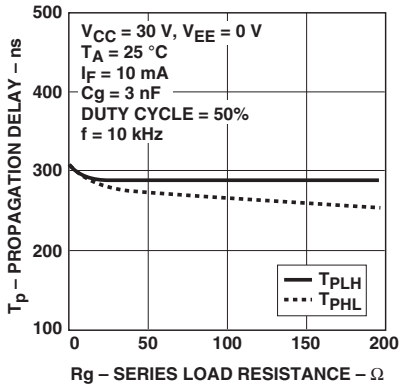


Figure 13. Propagation Delay vs. Rg.

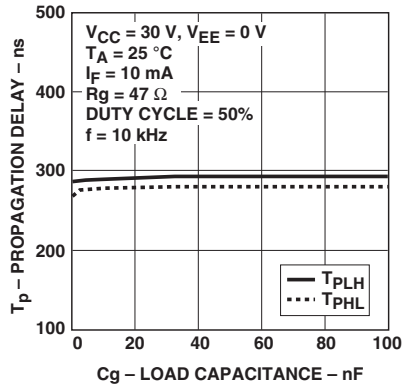


Figure 14. Propagation Delay vs. Cg.

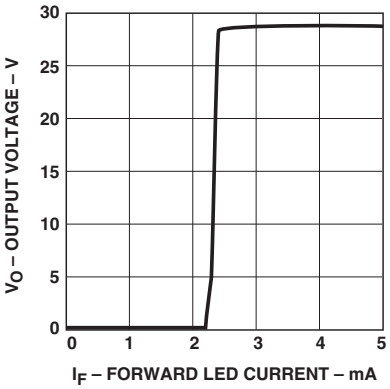


Figure 15. Transfer Characteristics.

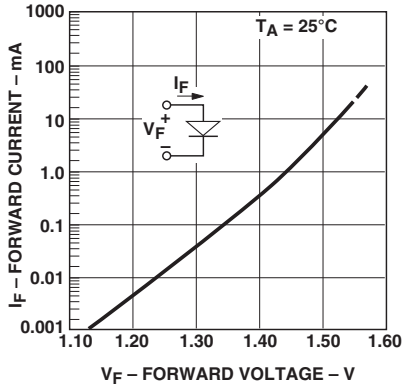


Figure 16. Input Current vs. Forward Voltage.

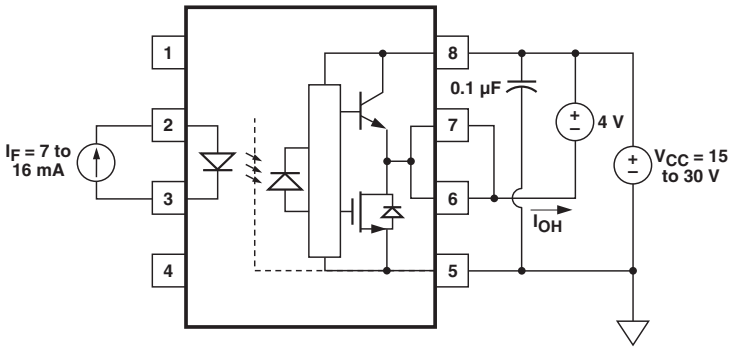


Figure 17. I_{OH} Test Circuit.

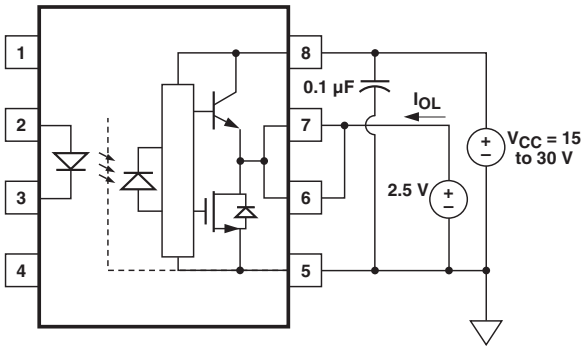


Figure 18. I_{OL} Test Circuit.

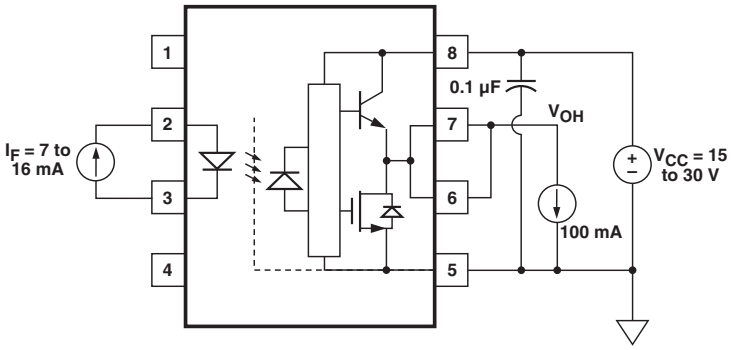


Figure 19. V_{OH} Test Circuit.

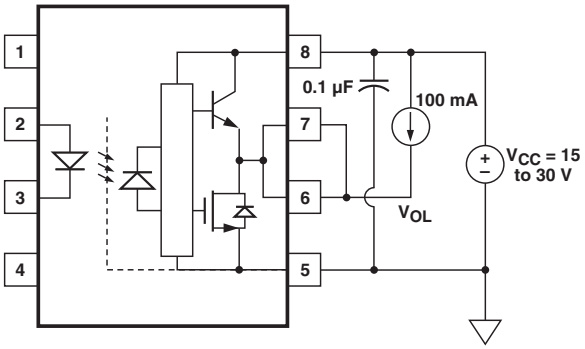


Figure 20. V_{OL} Test Circuit.

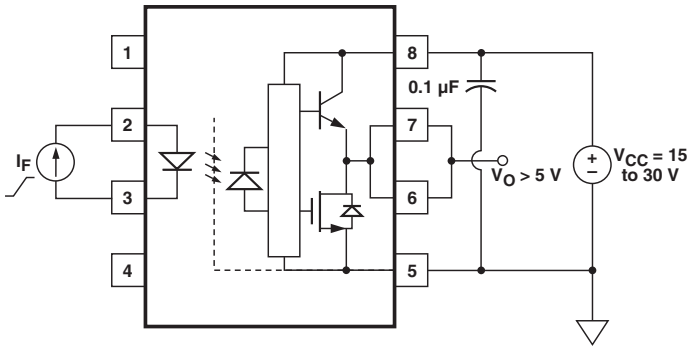


Figure 21. I_{FLH} Test Circuit.

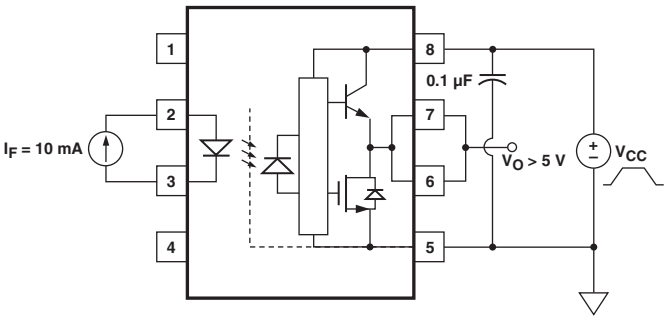


Figure 22. UVLO Test Circuit.

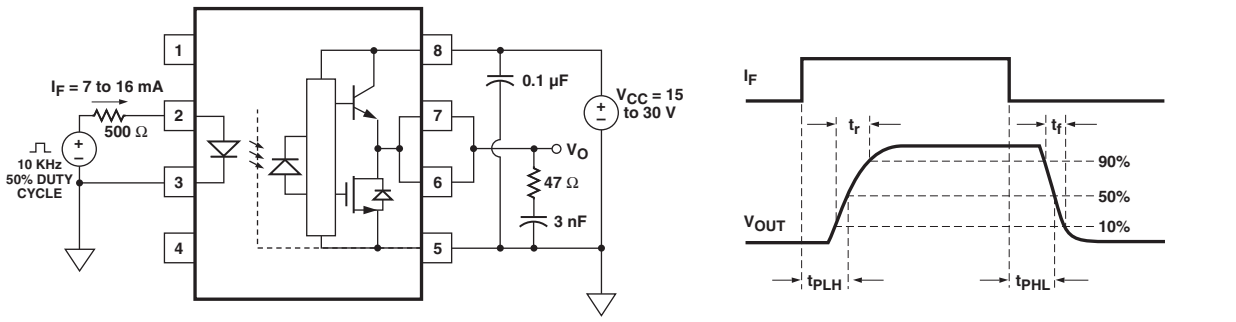


Figure 23. t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit and Waveforms.

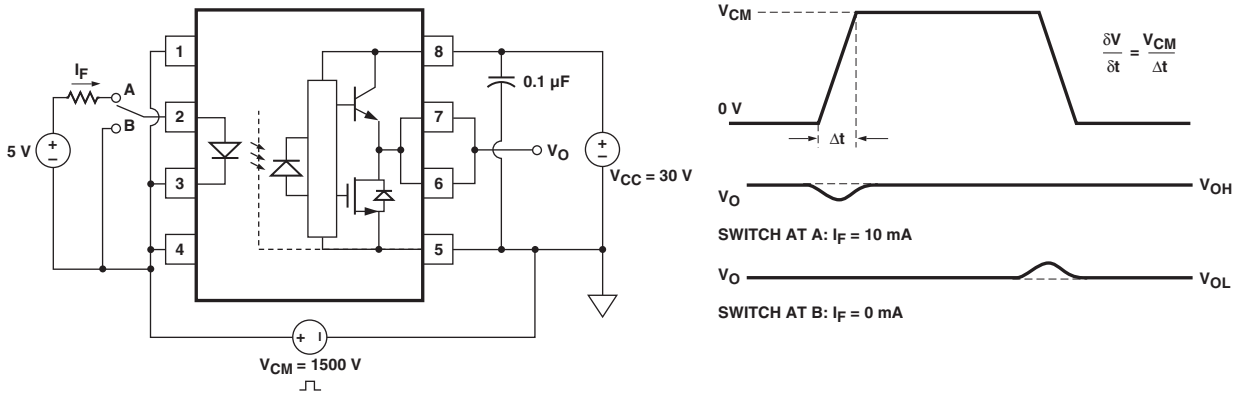


Figure 24. CMR Test Circuit and Waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3150/315J has a very low maximum V_{OL} specification of 1.0 V. The HCPL-3150/315J realizes this very low V_{OL} by using a DMOS transistor with 4 Ω (typical) on resistance in its pull down circuit. When the HCPL-3150/315J is in the low state, the IGBT gate is shorted to the emitter by Rg + 4 Ω. Minimizing Rg and the lead inductance from the HCPL-3150/315J to the IGBT gate and emitter (possibly by mounting the HCPL-3150/315J on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3150/315J input as this can result in unwanted coupling of transient signals into the HCPL-3150/315J and degrade performance. (If the IGBT drain must be routed near the HCPL-3150/315J input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3150/315J.)

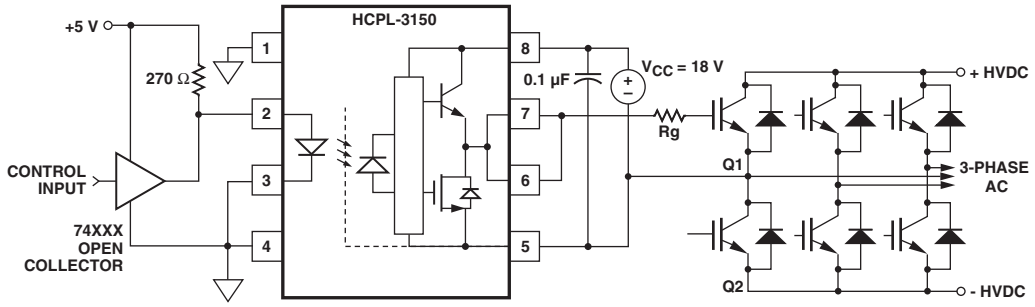


Figure 25a. Recommended LED Drive and Application Circuit.

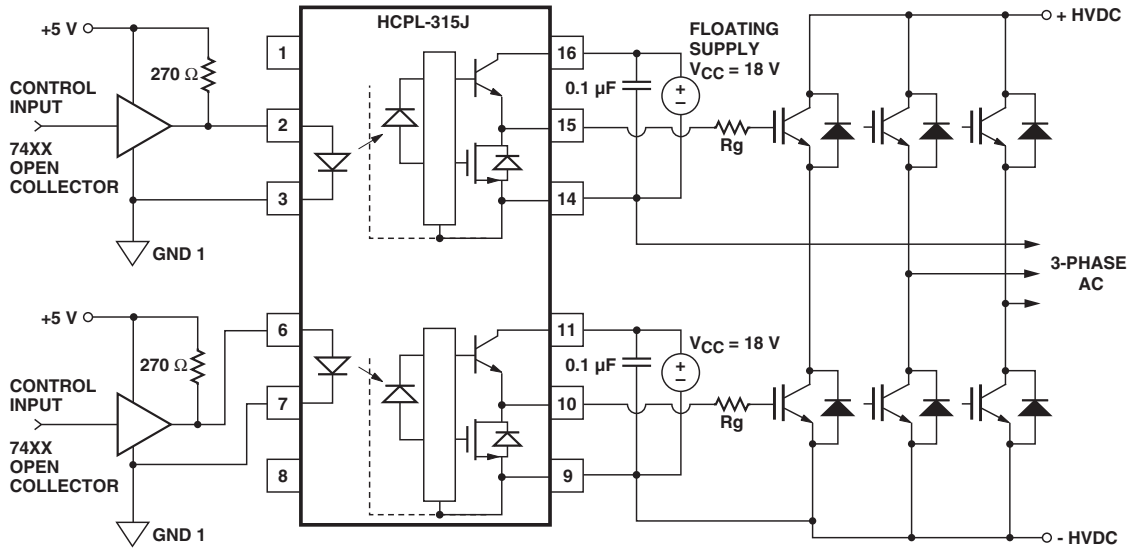


Figure 25b. Recommended LED Drive and Application Circuit (HCPL-315J)

Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses.

Step 1: Calculate Rg Minimum From the I_{0L} Peak Specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3150/315J.

$$Rg \geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}}$$

$$= \frac{(V_{CC} - V_{EE} - 1.7\ V)}{I_{OLPEAK}}$$

$$= \frac{(15\ V + 5\ V - 1.7\ V)}{0.6\ A}$$

$$= 30.5\ \Omega$$

The V_{OL} value of 2V in the previous equation is a conservative value of V_{OL} at the peak current of 0.6 A (see Figure 6). At lower Rg values the voltage supplied by the HCPL-3150/315J is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used V_{EE} in the previous equation is equal to zero volts.

Step 2: Check the HCPL-3150/315J Power Dissipation and Increase Rg if Necessary. The HCPL-3150/315J total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$$P_T = P_E + P_O$$

$$P_E = I_F \cdot V_F \cdot Duty\ Cycle$$

$$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$$

$$= I_{CC} \cdot (V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G) \cdot f$$

For the circuit in Figure 26 with I_F (worst case) = 16 mA, Rg = 30.5 Ω, Max Duty Cycle = 80%, Qg = 500 nC, f = 20 kHz and T_A max = 90°C:

$$P_E = 16\ mA \cdot 1.8\ V \cdot 0.8 = 23\ mW$$

$$P_O = 4.25\ mA \cdot 20\ V + 4.0\ \mu J \cdot 20\ kHz$$

$$= 85\ mW + 80\ mW$$

$$= 165\ mW > 154\ mW\ (P_{O(MAX)}\ @\ 90°C$$

$$= 250\ mW - 20C \cdot 4.8\ mW/C)$$

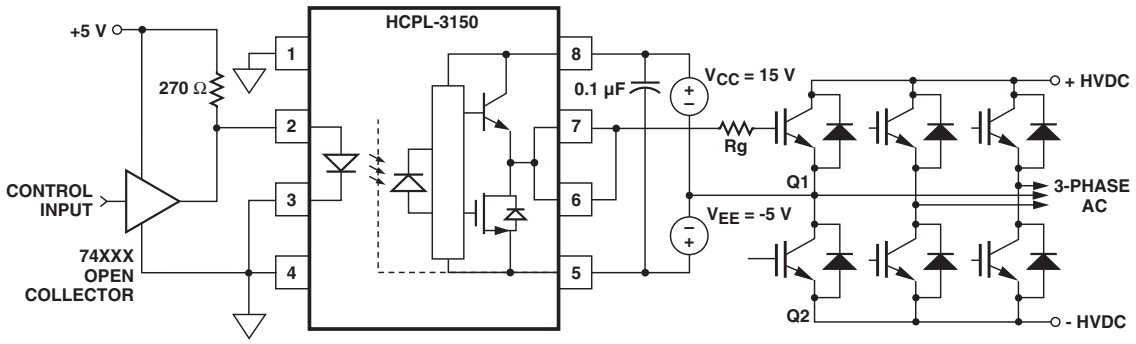


Figure 26a. HCPL-3150 Typical Application Circuit with Negative IGBT Gate Drive.

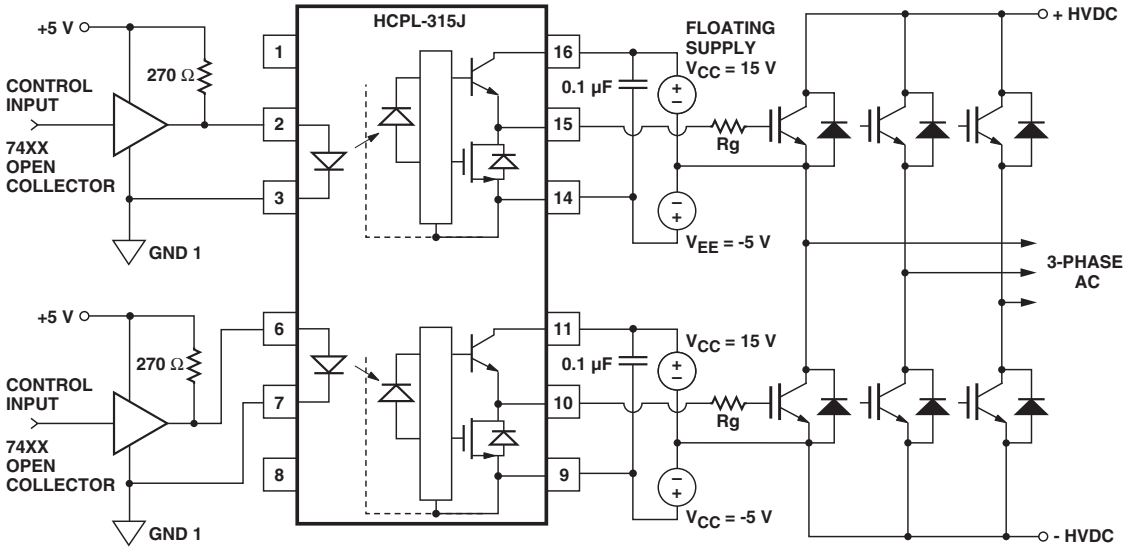


Figure 26b. HCPL-315J Typical Application Circuit with Negative IGBT Gate Drive.

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

P_O Parameter	Description
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
E_{SW}(Rg,Qg)	Energy Dissipated in the HCPL-3150/315J for each IGBT Switching Cycle (See Figure 27)
f	Switching Frequency

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -40°C) to I_{CC} max at 90°C (see Figure 7).

Since P_O for this case is greater than $P_{O(MAX)}$, Rg must be increased to reduce the HCPL-3150 power dissipation.

$$P_{O(SWITCHING\ MAX)} = P_{O(MAX)} - P_{O(BIAS)}$$
$$= 154\ mW - 85\ mW$$
$$= 69\ mW$$

$$E_{SW(MAX)} = \frac{P_{O(SWITCHINGMAX)}}{f}$$
$$= \frac{69\ mW}{20\ kHz} = 3.45\ \mu J$$

For Qg = 500 nC, from Figure 27, a value of E_{SW} = 3.45 µJ gives a Rg = 41 Ω.

Thermal Model (HCPL-3150)

The steady state thermal model for the HCPL-3150 is shown in Figure 28a. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL-3150 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA} value of 83°C/W.

From the thermal mode in Figure 28a the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \cdot (\theta_{LC} \| (\theta_{LD} + \theta_{DC}) + \theta_{CA}) + P_D \cdot \left(\frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + T_A$$

$$T_{JD} = P_E \left(\frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + P_D \cdot (\theta_{DC} \| (\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 28 gives:

$$T_{JE} = P_E \cdot (230°C/W + \theta_{CA}) + P_D \cdot (49°C/W + \theta_{CA}) + T_A$$

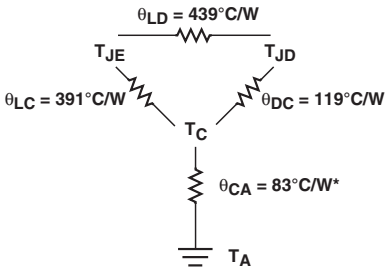
$$T_{JD} = P_E \cdot (49°C/W + \theta_{CA}) + P_D \cdot (104°C/W + \theta_{CA}) + T_A$$

For example, given P_E = 45 mW, P_O = 250 mW, T_A = 70°C and θ_{CA} = 83°C/W:

$$T_{JE} = P_E \cdot 313°C/W + P_D \cdot 132°C/W + T_A$$
$$= 45\ mW \cdot 313°C/W + 250\ mW \cdot 132°C/W + 70°C = 117°C$$

$$T_{JD} = P_E \cdot 132°C/W + P_D \cdot 187°C/W + T_A$$
$$= 45\ mW \cdot 132C/W + 250\ mW \cdot 187°C/W + 70°C = 123°C$$

T_{JE} and T_{JD} should be limited to 125°C based on the board layout and part placement (θ_{CA}) specific to the application.



T_{JE} = LED junction temperature
T_{JD} = detector IC junction temperature
T_C = case temperature measured at the center of the package bottom
θ_{LC} = LED-to-case thermal resistance
θ_{LD} = LED-to-detector thermal resistance
θ_{DC} = detector-to-case thermal resistance
θ_{CA} = case-to-ambient thermal resistance
*θ_{CA} will depend on the board design and the placement of the part.

Figure 28a. Thermal Model.

Thermal Model Dual-Channel (SOIC-16) HCPL-315J Optoisolator

Definitions

θ_1, θ_2, θ_3, θ_4, θ_5, θ_6, θ_7, θ_8, θ_9, θ_{10}: Thermal impedances between nodes as shown in Figure 28b. Ambient Temperature: Measured approximately 1.25 cm above the optocoupler with no forced air.

Description

This thermal model assumes that a 16-pin dual-channel (SOIC-16) optocoupler is soldered into an 8.5 cm x 8.1 cm printed circuit board (PCB). These optocouplers are hybrid devices with four die: two LEDs and two detectors. The temperature at the LED and the detector of the optocoupler can be calculated by using the equations below.

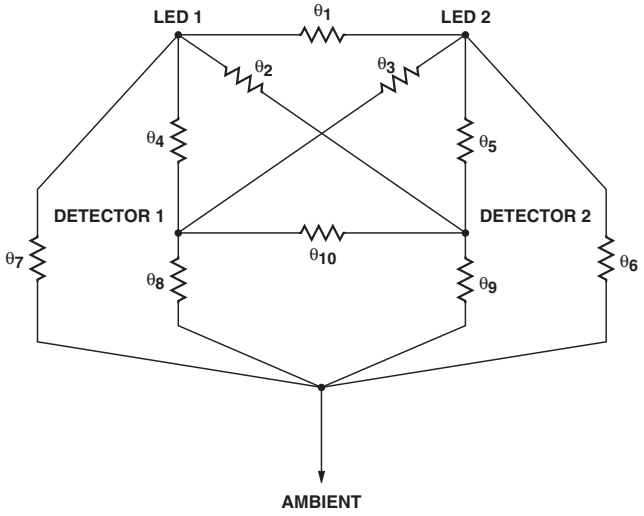


Figure 28b. Thermal Impedance Model for HCPL-315J.

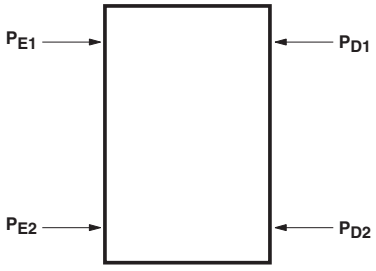
$$\Delta T_{E1A} = A_{11}P_{E1} + A_{12}P_{E2} + A_{13}P_{D1} + A_{14}P_{D2}$$

$$\Delta T_{E2A} = A_{21}P_{E1} + A_{22}P_{E2} + A_{23}P_{D1} + A_{24}P_{D2}$$

$$\Delta T_{D1A} = A_{31}P_{E1} + A_{32}P_{E2} + A_{33}P_{D1} + A_{34}P_{D2}$$

$$\Delta T_{D2A} = A_{41}P_{E1} + A_{42}P_{E2} + A_{43}P_{D1} + A_{44}P_{D2}$$

where:



ΔT_{E1A} = Temperature difference between ambient and LED 1
ΔT_{E2A} = Temperature difference between ambient and LED 2
ΔT_{D1A} = Temperature difference between ambient and detector 1
ΔT_{D2A} = Temperature difference between ambient and detector 2
P_{E1} = Power dissipation from LED 1;
P_{E2} = Power dissipation from LED 2;
P_{D1} = Power dissipation from detector 1;
P_{D2} = Power dissipation from detector 2
A_{xy} thermal coefficient (units in °C/W) is a function of thermal impedances θ_1 through θ_{10}.

Thermal Coefficient Data (units in °C/W)

Part Number	A_{11}, A_{22}	A_{12}, A_{21}	A_{13}, A_{31}	A_{24}, A_{42}	A_{14}, A_{41}	A_{23}, A_{32}	A_{33}, A_{44}	A_{34}, A_{43}
HCPL-315J	198	64	62	64	83	90	137	69

Note: Maximum junction temperature for above part: 125°C.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The HCPL-3150/315J improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. How ever, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 15 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 15 kV/µs CMR.

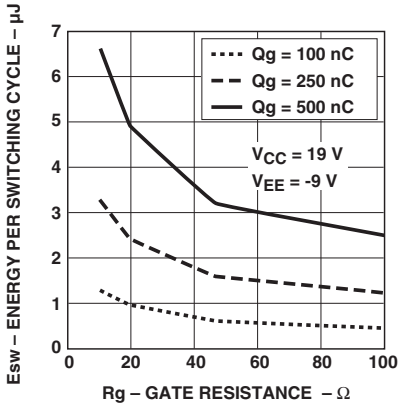


Figure 27. Energy Dissipated in the HCPL-3150 for Each IGBT Switching Cycle.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \le V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 32, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 33 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Under Voltage Lockout Feature

The HCPL-3150/315J contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3150/315J supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3150/315J output is in the high state and the supply voltage drops below the HCPL-3150/315J V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$), the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 µs. When the HCPL-3150/315J output is in the low state and the supply voltage rises above the HCPL-3150/315J V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$), the optocoupler will go into the high state (assuming LED is "ON") with a typical delay, UVLO TURN On Delay, of 0.8 µs.

IPM Dead Time and Propagation Delay Specifications

The HCPL-3150/315J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high- to the low-voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 34. The amount of delay necessary to achieve this conditions is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 35. The maximum dead time for the HCPL-3150/315J is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

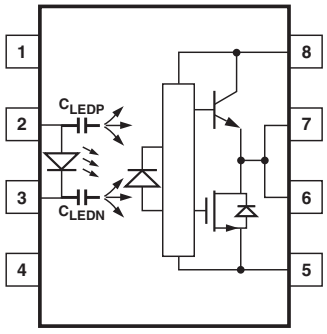


Figure 29. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

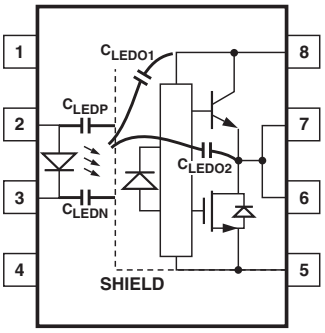


Figure 30. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

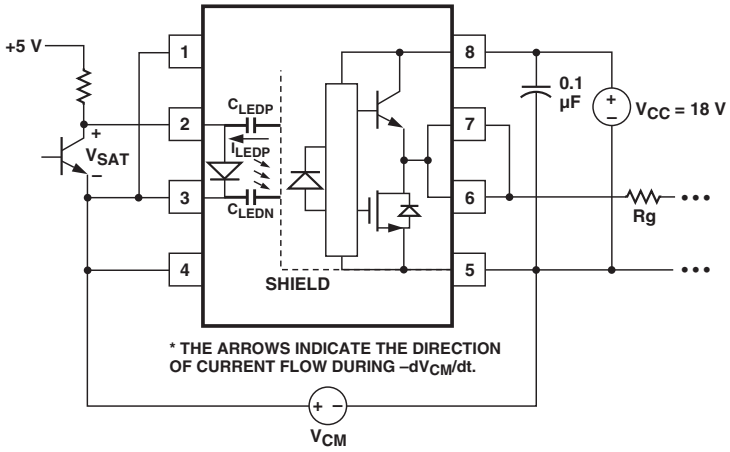


Figure 31. Equivalent Circuit for Figure 25 During Common Mode Transient.

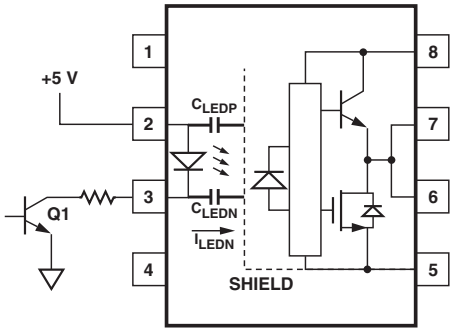


Figure 32. Not Recommended Open Collector Drive Circuit.

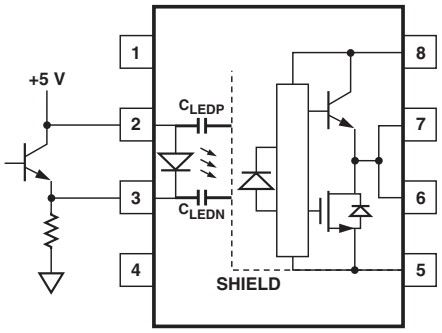
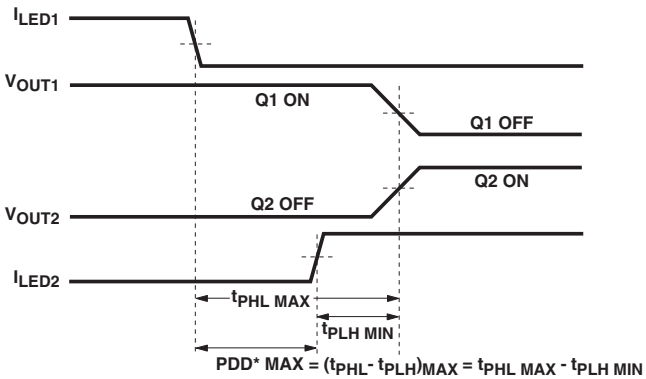
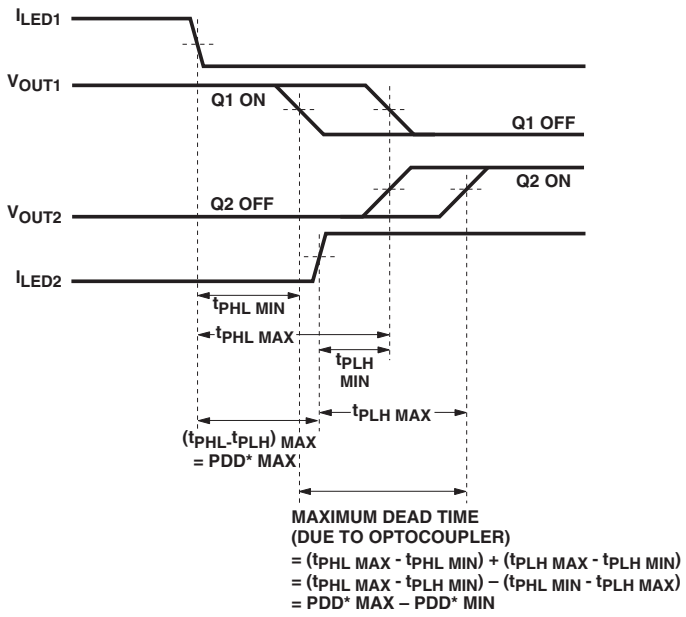


Figure 33. Recommended LED Drive Circuit for Ultra-High CMR.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 34. Minimum LED Skew for Zero Dead Time.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 35. Waveforms for Dead Time.

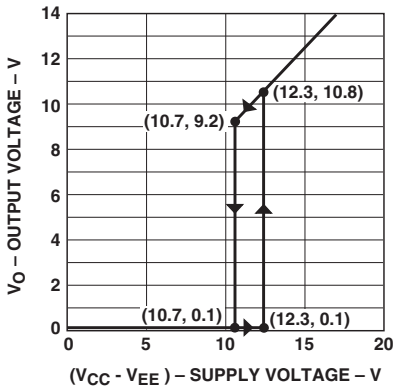


Figure 36. Under Voltage Lock Out.

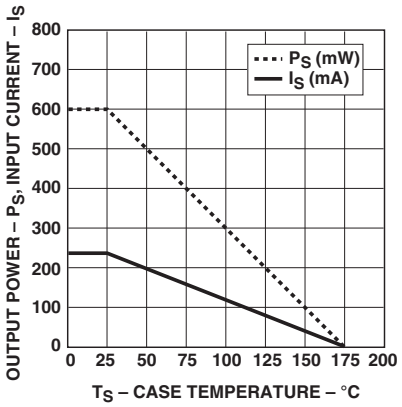


Figure 37a. HCPL-3150: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-2.

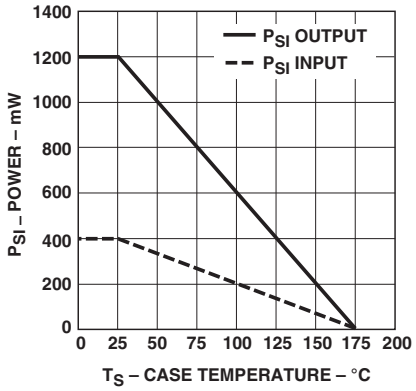


Figure 37b. HCPL-315J: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-2.

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