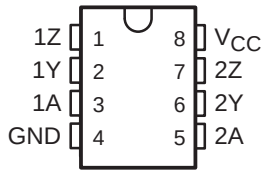
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **Single 5-V Supply**
- **Balanced-Line Operation**
- **TTL Compatible**
- **High Output Impedance in Power-Off Condition**
- **High-Current Active-Pullup Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Input Clamp Diodes**

**D, P, OR PS† PACKAGE**
**(TOP VIEW)**



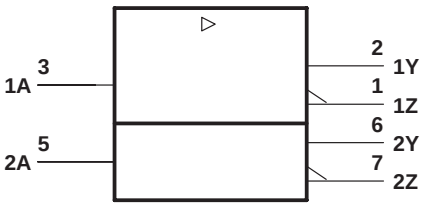

† The PS package is only available left-end taped and reeled, i.e., order SN75158PSLE.

## description

The SN75158 is a dual differential line driver designed to satisfy the requirements set by the ANSI EIA/TIA-422-B and ITU V.11 interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

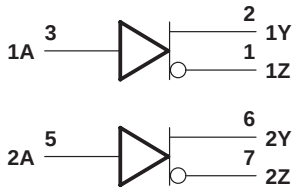
The SN75158 is characterized for operation from 0°C to 70°C.

### logic symbol‡




‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)

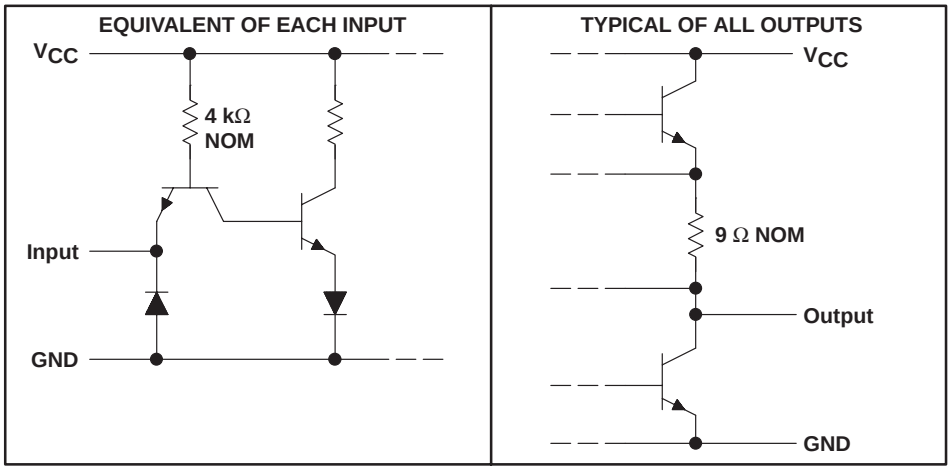



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## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage, $V_I$ . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage $V_{OD}$, are with respect to network ground terminal. $V_{OD}$ is at the Y output with respect to the Z output.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |
| PS | 450 mW | 3.6 mW/°C | 288 mW |

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | –40 | mA |
| Low-level output current, $I_{OL}$ | | | 40 | mA |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = –12 mA | | | –0.9 | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V, $I_{OH}$ = –40 mA | | 2.4 | 3 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V, $I_{OL}$ = 40 mA | | | 0.2 | 0.4 | V |
| $\lvert V_{OD1}\rvert$ | Differential output voltage | $V_{CC}$ = MAX, $I_O$ = 0 | | | 3.5 | $2\times V_{OD2}$ | V |
| $\lvert V_{OD2}\rvert$ | Differential output voltage | $V_{CC}$ = MIN | $R_L$ = 100 Ω, See Figure 1 | 2 | 3 | | V |
| $\Delta V_{OD}$ | Change in magnitude of differential output voltage§ | $V_{CC}$ = MIN | | | ±0.02 | ±0.4 | V |
| $V_{OC}$ | Common-mode output voltage¶ | $V_{CC}$ = MAX | | | 1.8 | 3 | V |
| | | $V_{CC}$ = MIN | | | 1.5 | 3 | |
| $\Delta V_{OC}$ | Change in magnitude of common-mode output voltage§ | $V_{CC}$ = MIN or MAX | | | ±0.02 | ±0.4 | V |
| $I_O$ | Output current with power off | $V_{CC}$ = 0 | $V_O$ = 6 V | | 0.1 | 100 | μA |
| | | | $V_O$ = – 0.25 V | | –0.1 | –100 | |
| | | | $V_O$ = – 0.25 to 6 V | | | ±100 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | –1 | –1.6 | mA |
| $I_{OS}$ | Short-circuit output current# | $V_{CC}$ = MAX | | –40 | –90 | –150 | mA |
| $I_{CC}$ | Supply current (both drivers) | $V_{CC}$ = MAX, $T_A$ = 25°C, | Inputs grounded, No load | | 37 | 50 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C except for $V_{OC}$, for which $V_{CC}$ is as stated under test conditions.
§ $\Delta V_{OD}$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, $V_{OC}$, which is the average of the two output voltages with respect to ground, is called output offset voltage, $V_{OS}$.
# Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 2, Termination A | | 16 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 10 | 20 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 2, Termination B | | 13 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 9 | 15 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | See Figure 2, Termination A | | 4 | 20 | ns |
| $t_{TLH}$ | Transition time, high-to-low-level output | | | 4 | 20 | ns |
| | Overshoot factor | See Figure 2, Termination C | | | 10% | |

## PARAMETER MEASUREMENT INFORMATION

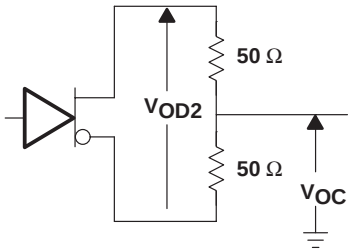
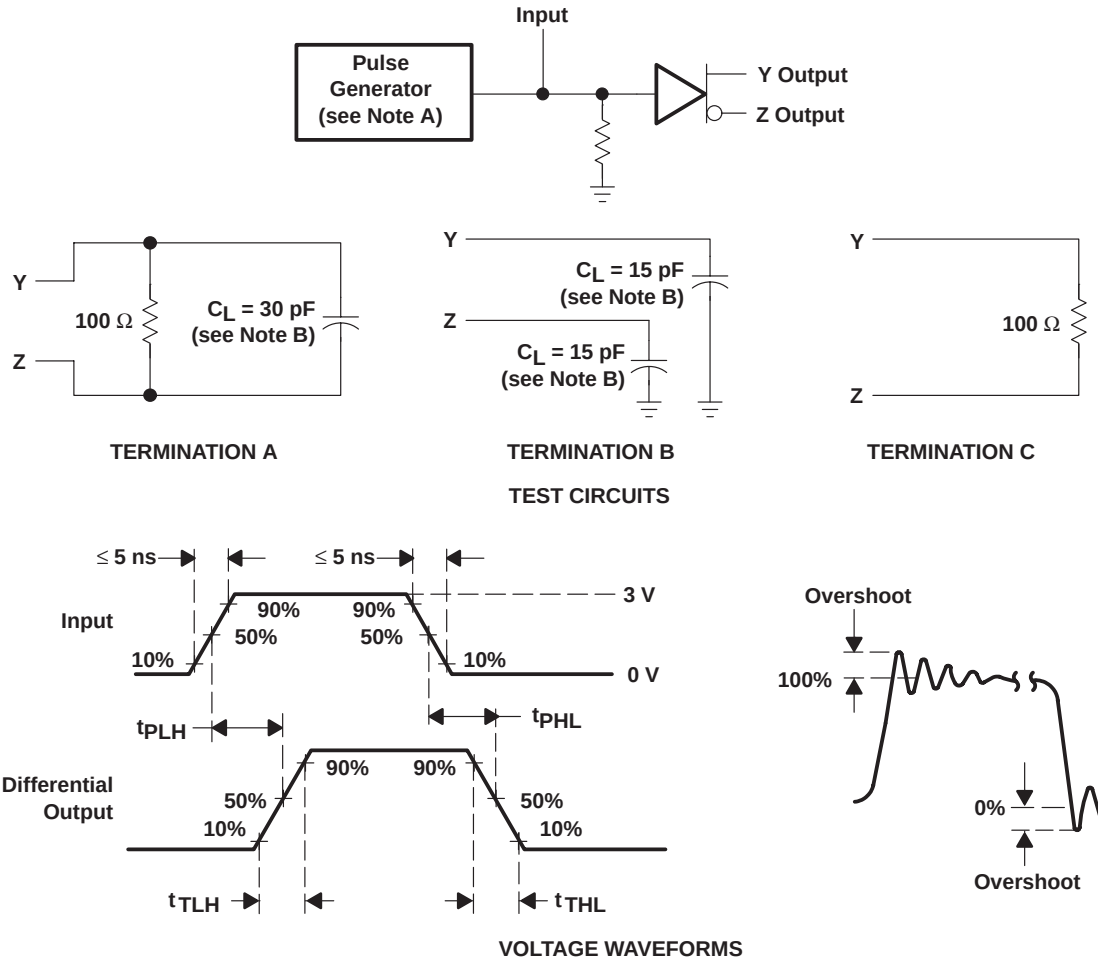



**Figure 1. Differential and Common-Mode Output Voltages**




NOTES: A. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, $t_W$ = 25 ns, PRR ≤ 10 MHz.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs DATA INPUT VOLTAGE**

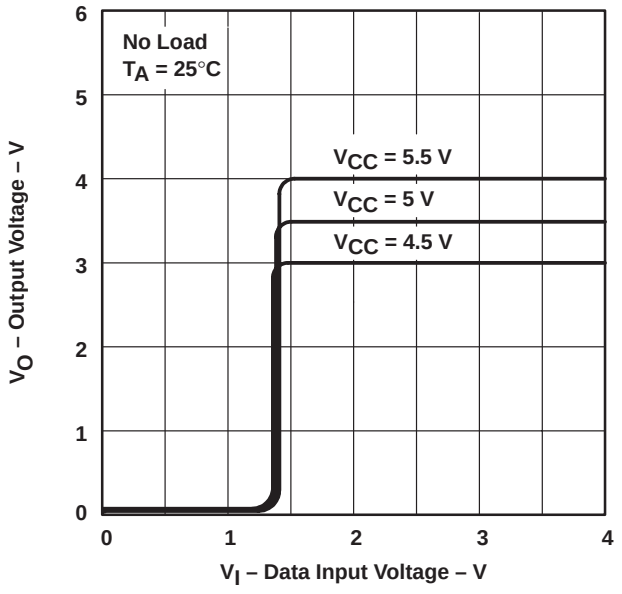



Figure 3

**OUTPUT VOLTAGE vs DATA INPUT VOLTAGE**

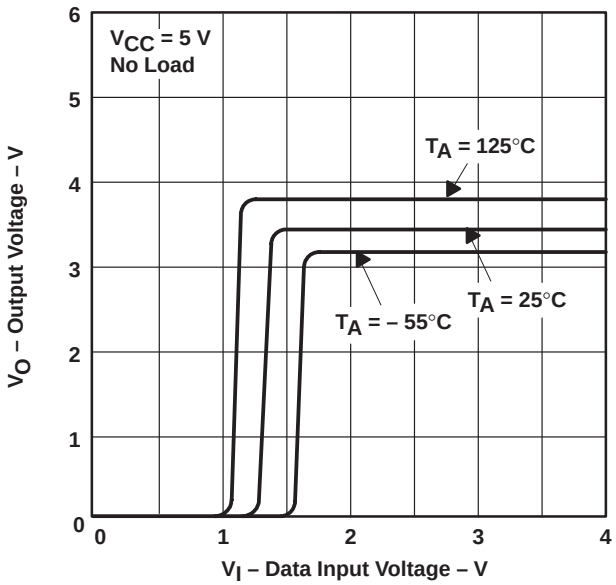



Figure 4

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

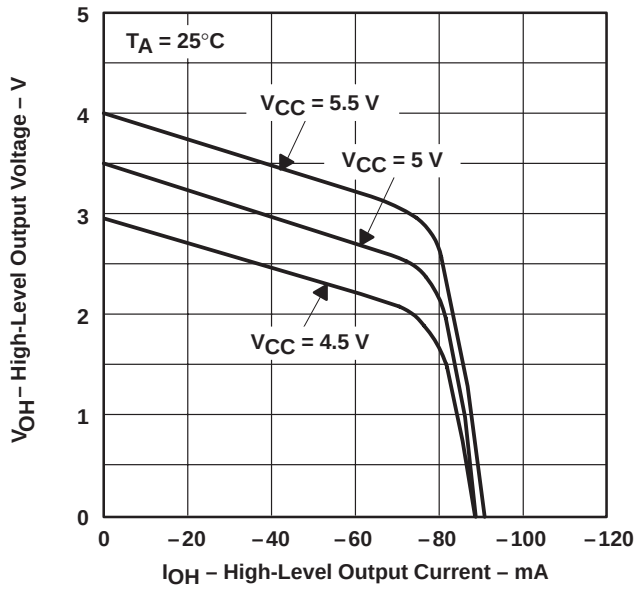



Figure 5

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

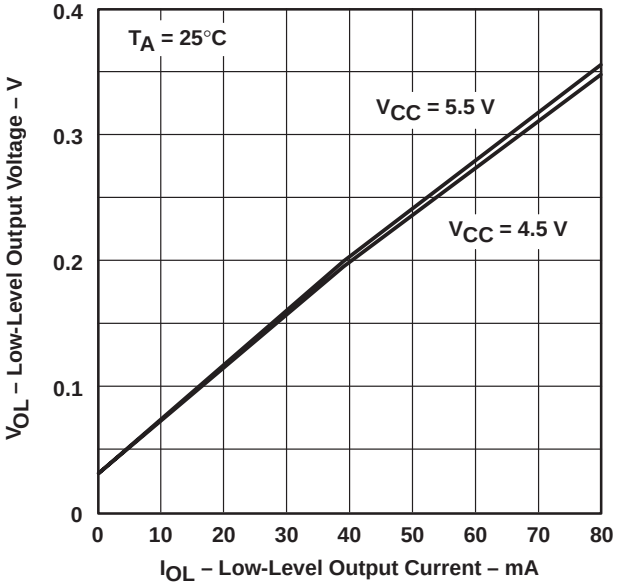



Figure 6

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

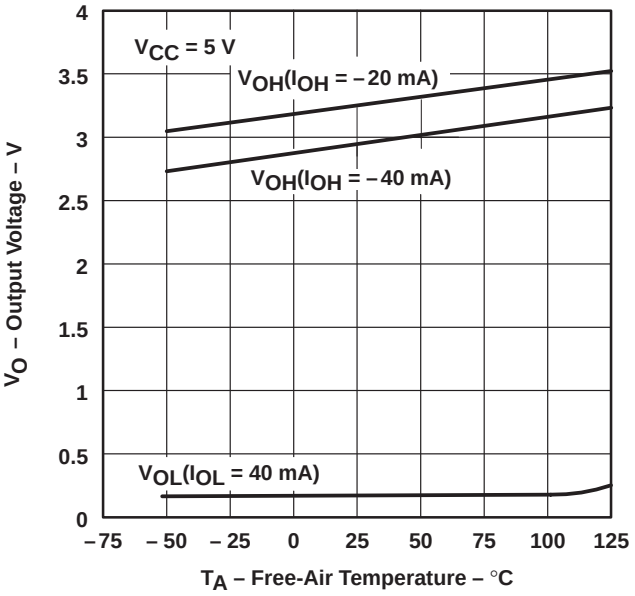



Figure 7

**PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE**

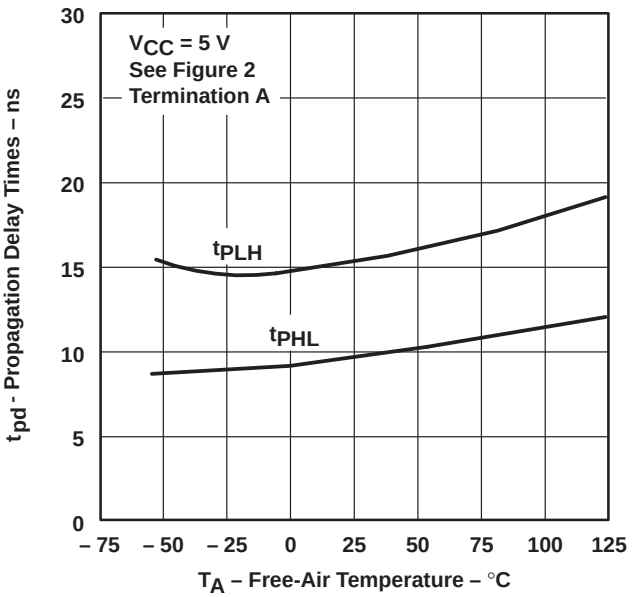



Figure 8

**SUPPLY CURRENT (BOTH DRIVERS) vs SUPPLY VOLTAGE**

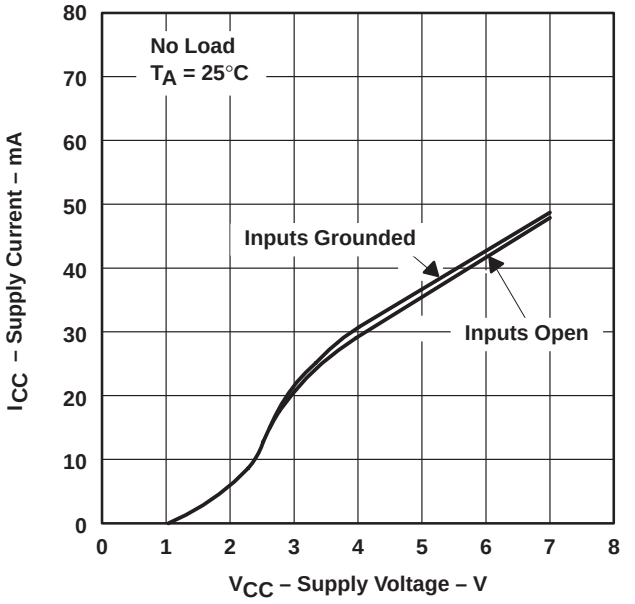



Figure 9

**SUPPLY CURRENT (BOTH DRIVERS) vs FREE-AIR TEMPERATURE**

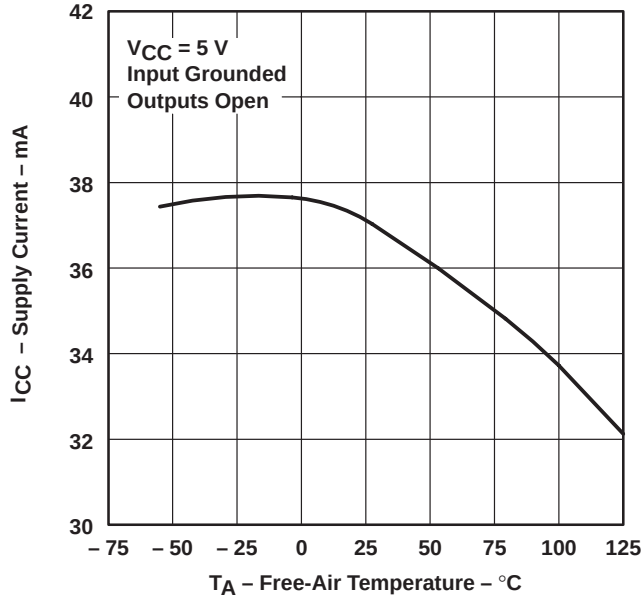



Figure 10

## TYPICAL CHARACTERISTICS

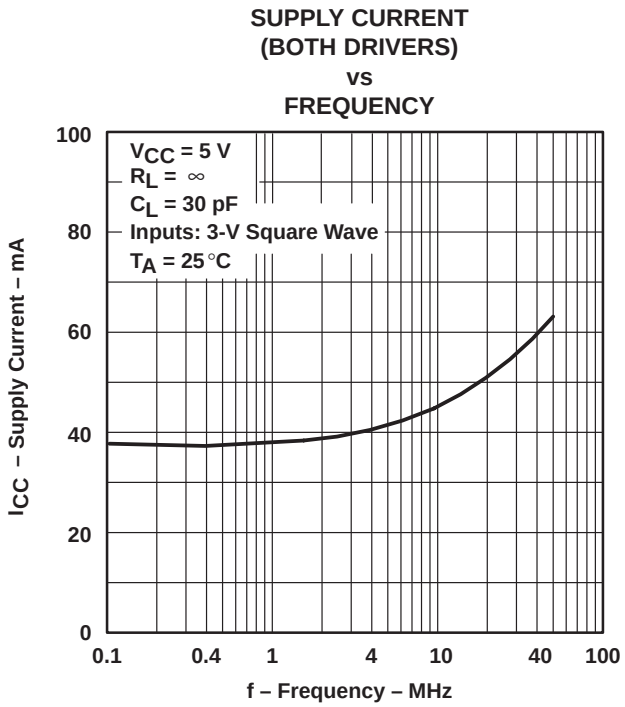



**Figure 11**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN75158D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75158PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75158PSLE | OBSOLETE | SO | PS | 8 | | TBD | Call TI | Call TI |
| SN75158PSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158PSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75158PSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

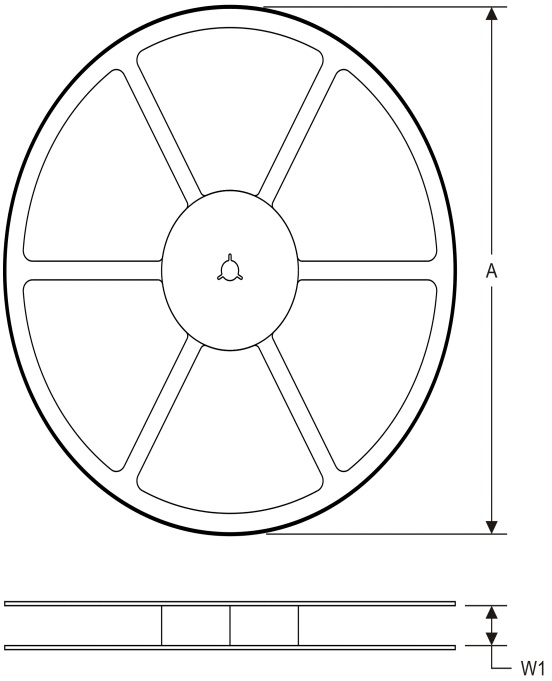
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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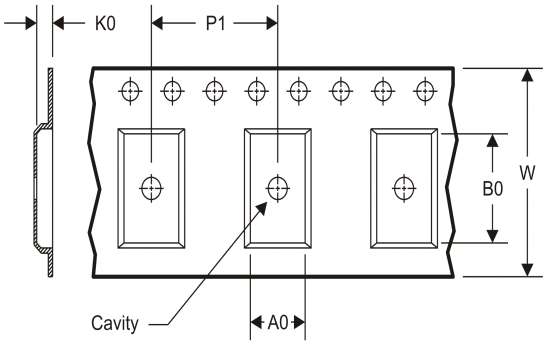
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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



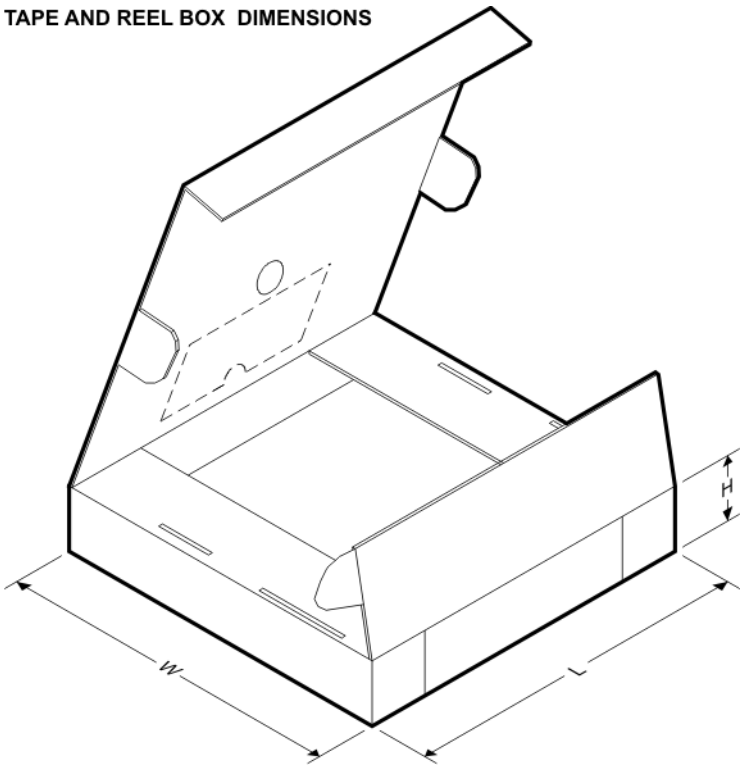

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75158DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75158PSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |

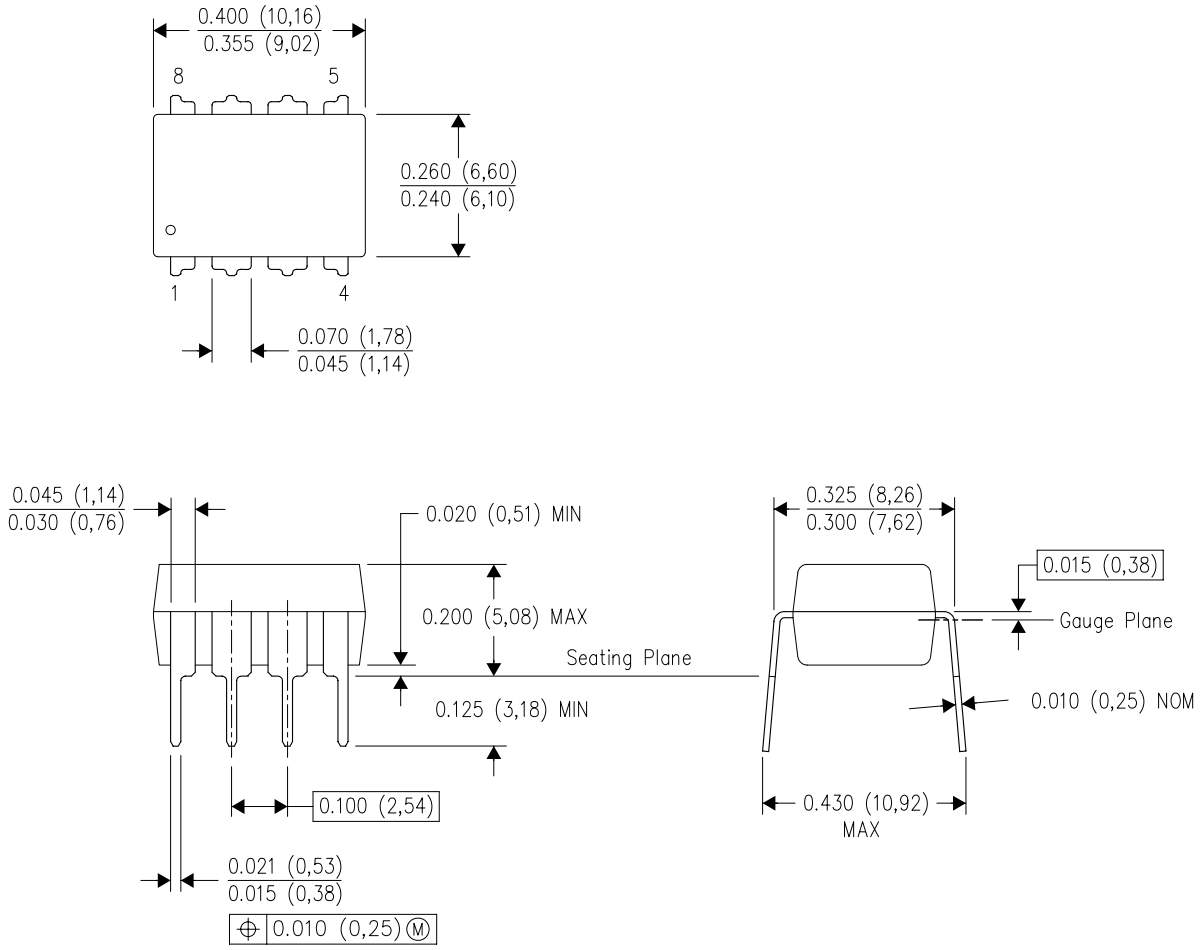
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

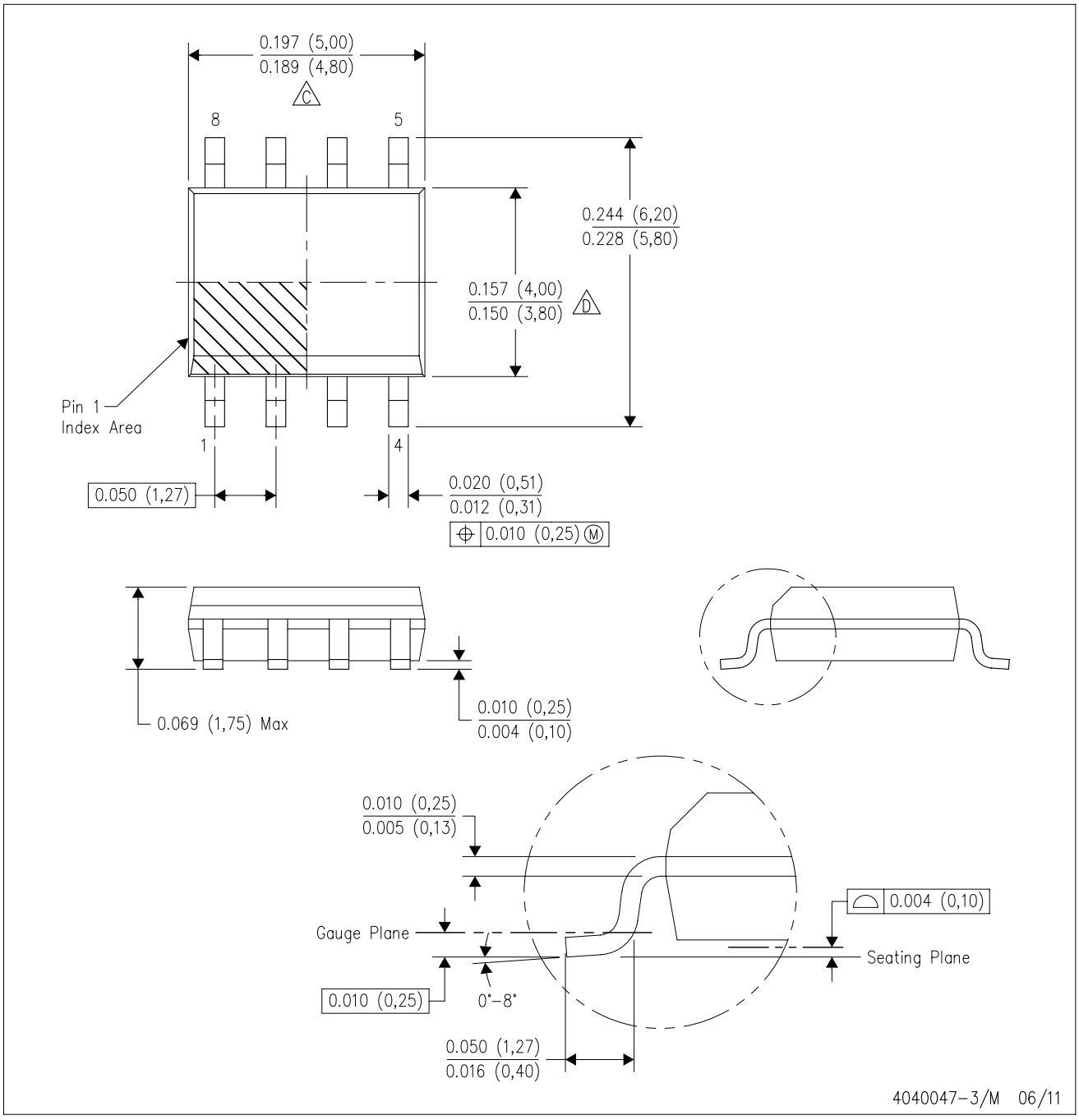
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75158DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN75158PSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



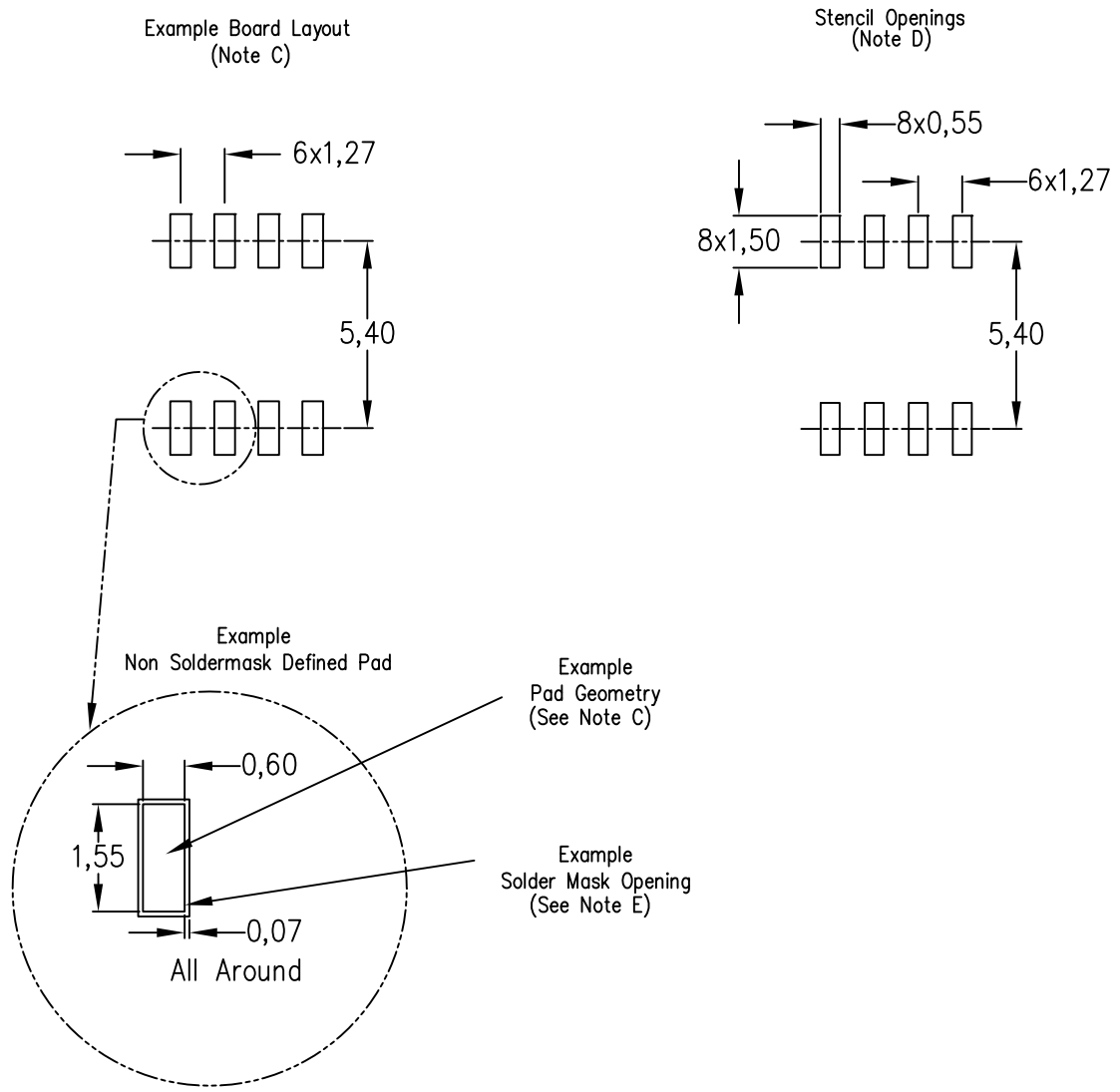

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

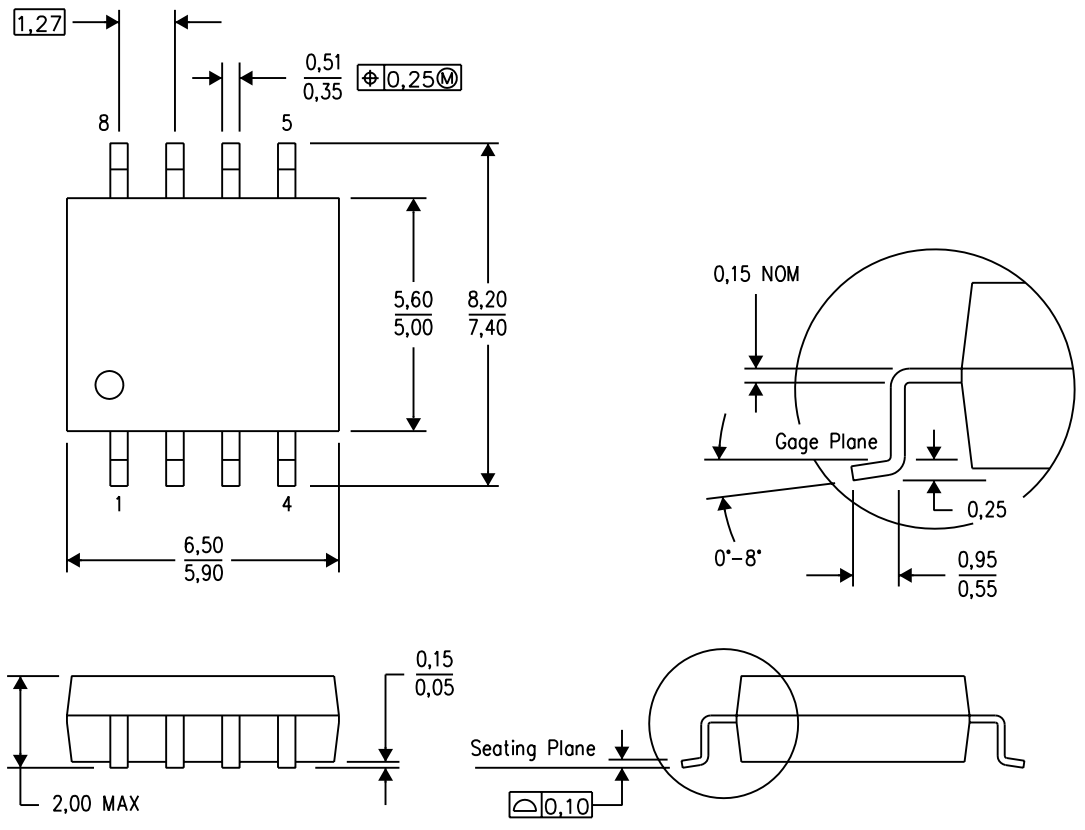
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

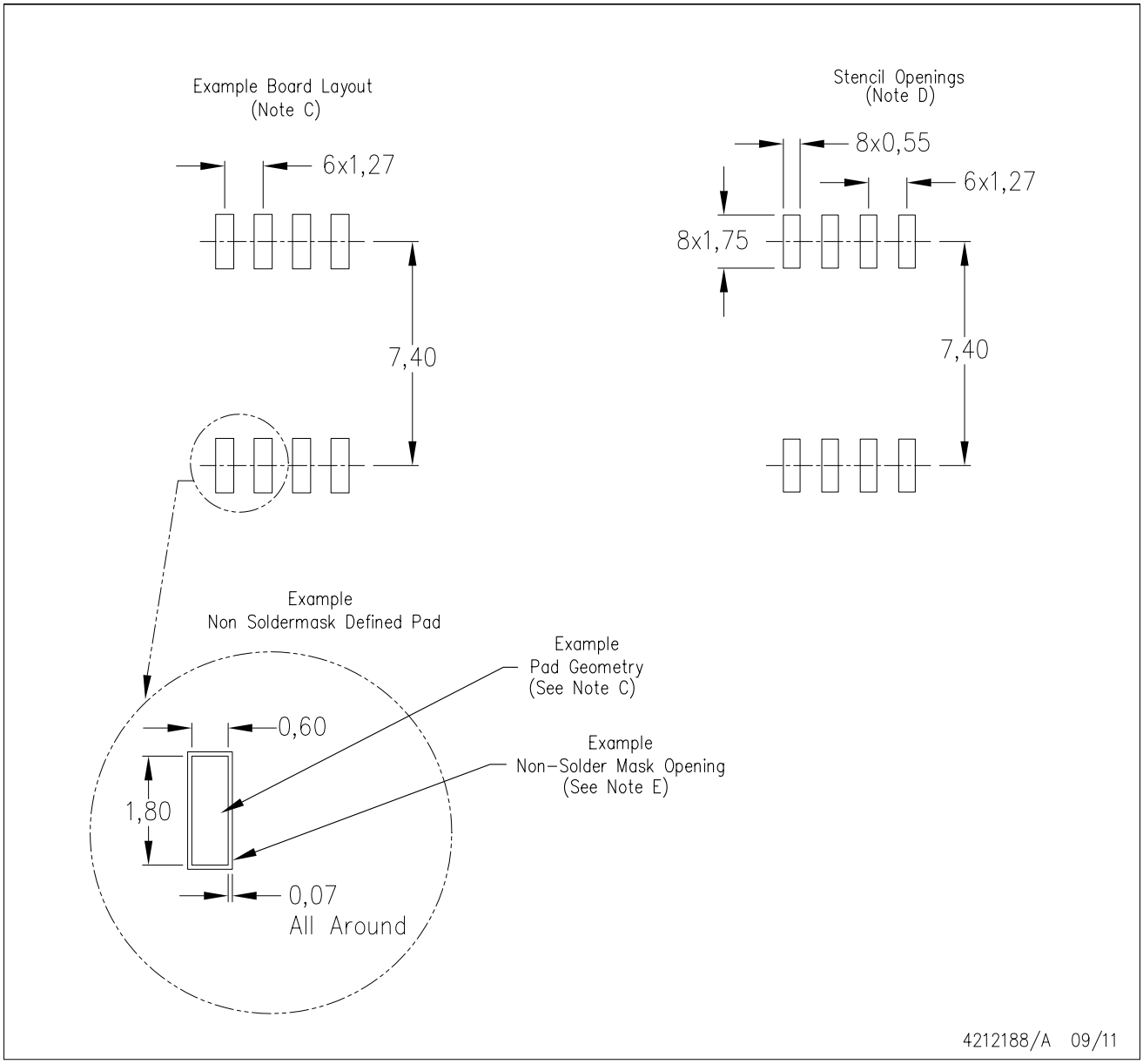
**PS (R-PDSO-G8)** **PLASTIC SMALL-OUTLINE PACKAGE**




4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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