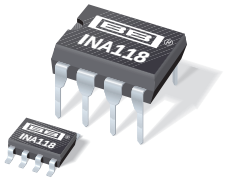
BURR-BROWN®



INA118

Precision, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±1.35 to ±18V
- LOW QUIESCENT CURRENT: 350μA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

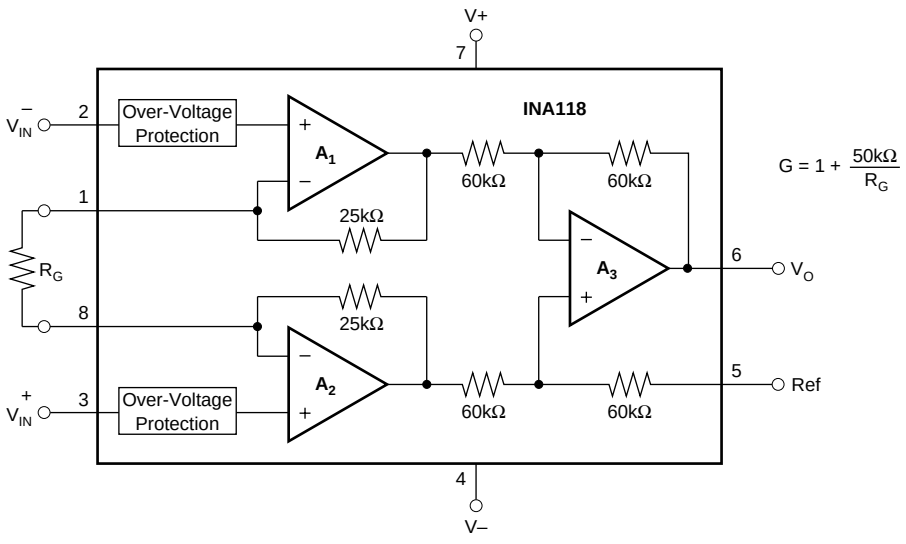
DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (70kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA118 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as ±1.35V, and quiescent current is only 350μA—ideal for battery operated systems.

The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SBOS027

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ unless otherwise noted.

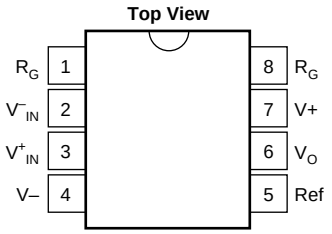
PARAMETER	CONDITIONS	INA118PB, UB			INA118P, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 ± 50/G	±50 ± 500/G		±25 ±100/G	±125±1000/G	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±0.2 ± 2/G	±0.5 ± 20/G		±0.2 ± 5/G	±1 ± 20/G	µV/°C
vs Power Supply	V_S = ±1.35V to ±18V		±1 ±10/G	±5 ± 100/G		*	±10 ±100/G	µV/V
Long-Term Stability			±0.4 ±5/G			*		µV/mo
Impedance, Differential			10^{10} || 1			*		Ω || pF
Common-Mode			10^{10} || 4			*		Ω || pF
Linear Input Voltage Range		(V+) – 1	(V+) – 0.65		*	*		V
		(V–) + 1.1	(V–) + 0.95		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ							
	G = 1	80	90		73	*		dB
	G = 10	97	110		89	*		dB
	G = 100	107	120		98	*		dB
	G = 1000	110	125		100	*		dB
BIAS CURRENT			±1	±5		*	±10	nA
vs Temperature			±40			*		pA/°C
OFFSET CURRENT			±1	±5		*	±10	nA
vs Temperature			±40			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			11			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.28			*		µVp-p
Noise Current								
f=10Hz			2.0			*		pA/√Hz
f=1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			80			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.024		*	±0.1	%
	G = 10		±0.02	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5	±1		*	±2	%
Gain vs Temperature	G = 1		±1	±10		*	±10	ppm/°C
50kΩ Resistance[1]			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0003	±0.001		*	±0.002	% of FSR
	G = 10		±0.0005	±0.002		*	±0.004	% of FSR
	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 1000		±0.002	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1	(V+) – 0.8		*	*		V
Negative	R_L = 10kΩ	(V–) + 0.35	(V–) + 0.2		*	*		V
Single Supply High	V_S = +2.7V/0V[2], R_L = 10kΩ	1.8	2.0		*	*		V
Single Supply Low	V_S = +2.7V/0V[2], R_L = 10kΩ	60	35		*	*		mV
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+5/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	V_O = ±10V, G = 10		0.9			*		V/µs
Settling Time, 0.01%	G = 1		15			*		µs
	G = 10		15			*		µs
	G = 100		21			*		µs
	G = 1000		210			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±1.35	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±350	±385		*	*	µA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

PIN CONFIGURATION

8-Pin DIP and SO-8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA118P	8-Pin Plastic DIP	006	–40°C to +85°C
INA118PB	8-Pin Plastic DIP	006	–40°C to +85°C
INA118U	SO-8 Surface-Mount	182	–40°C to +85°C
INA118UB	SO-8 Surface-Mount	182	–40°C to +85°C

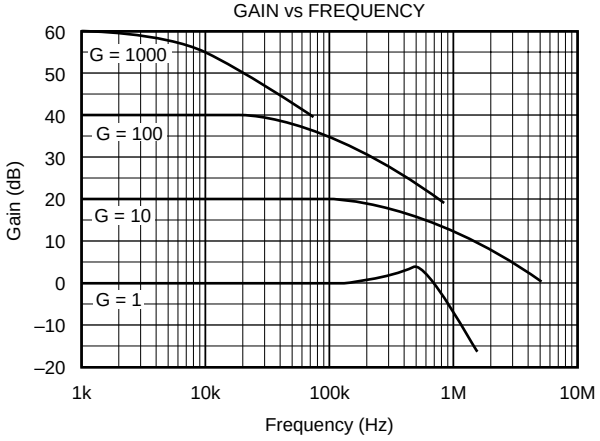
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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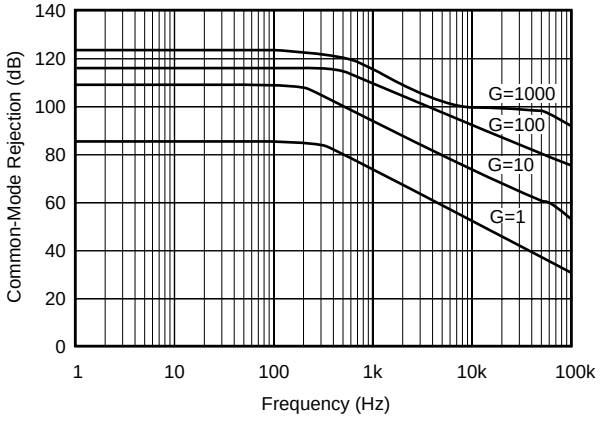
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

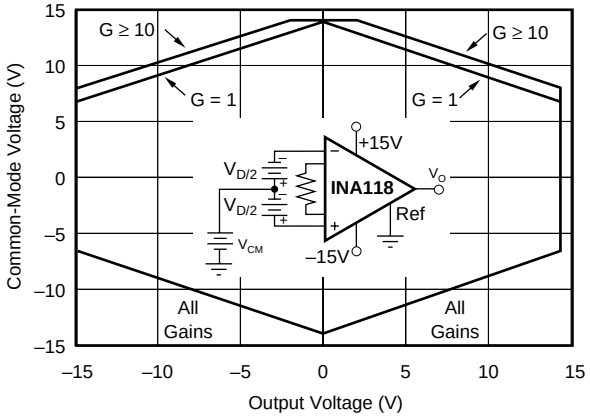
GAIN vs FREQUENCY



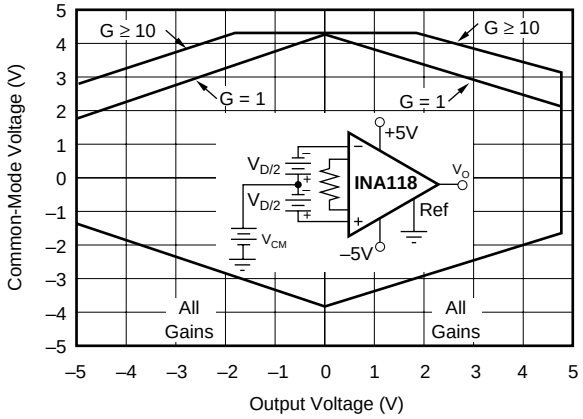
COMMON-MODE REJECTION vs FREQUENCY



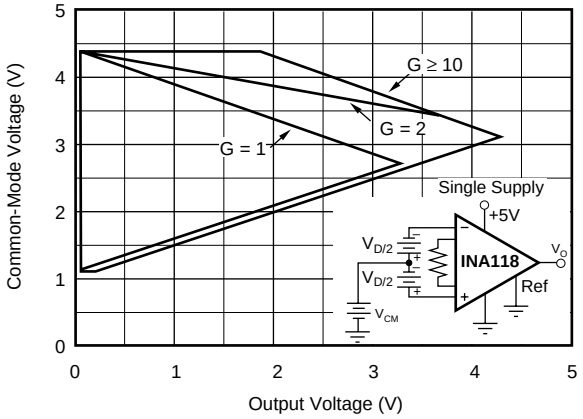
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



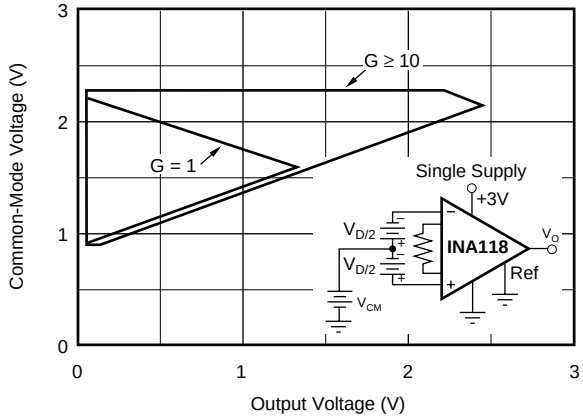
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



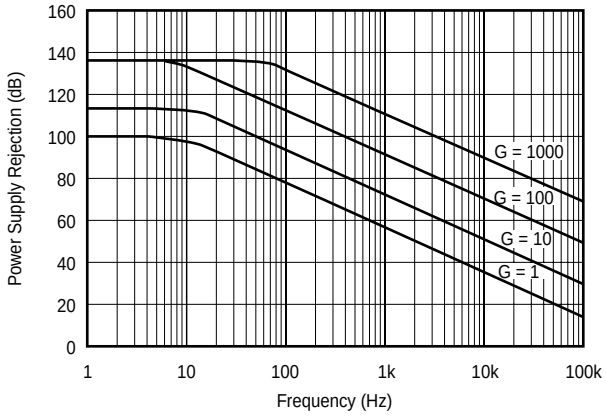
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



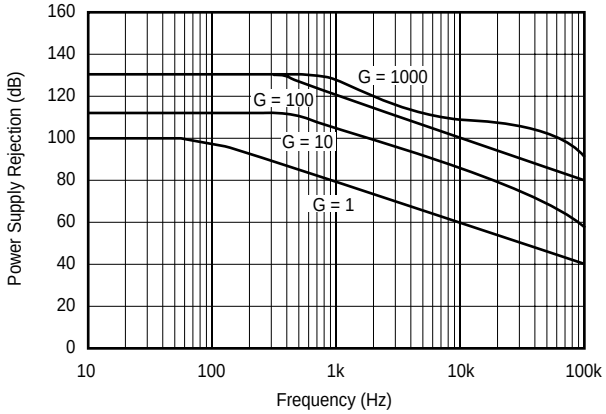
TYPICAL PERFORMANCE CURVES (CONT)

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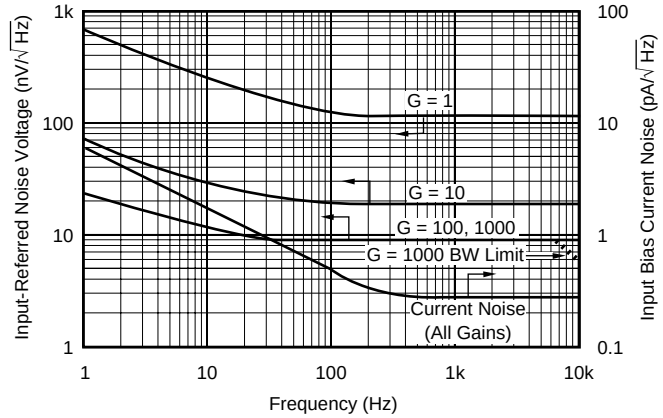
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



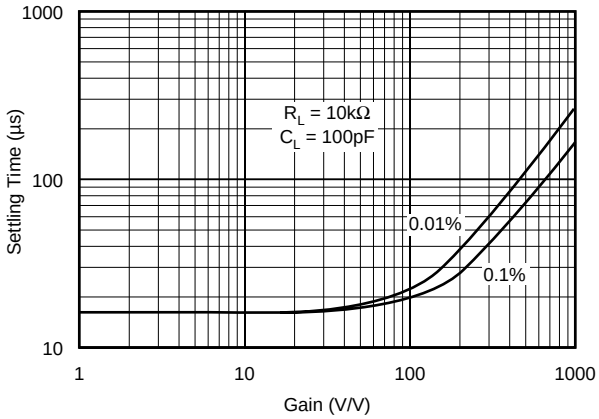
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



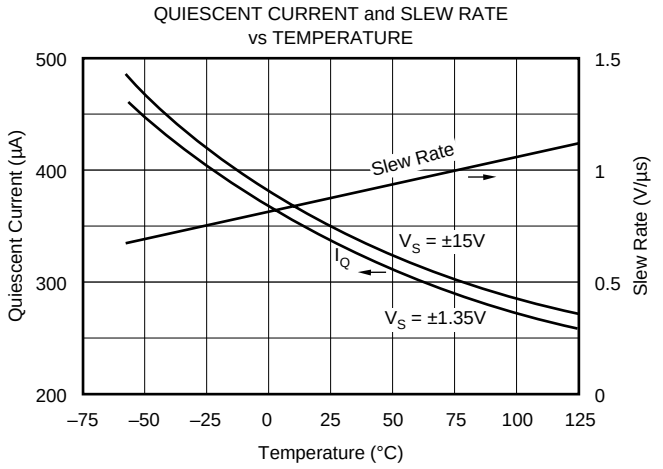
INPUT- REFERRED NOISE VOLTAGE vs FREQUENCY



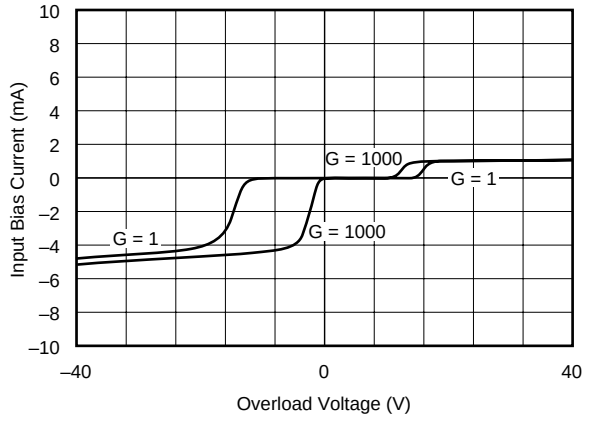
SETTLING TIME vs GAIN



QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



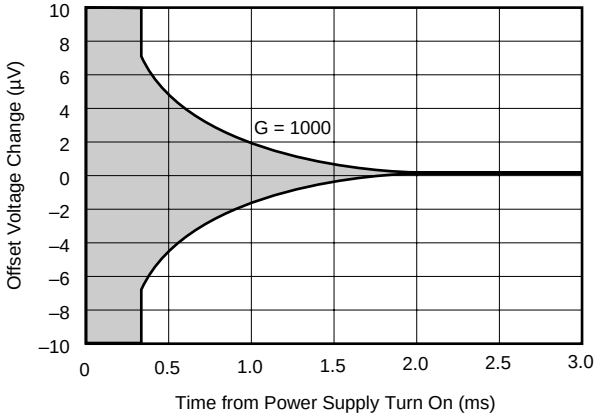
INPUT BIAS CURRENT vs INPUT OVERLOAD VOLTAGE



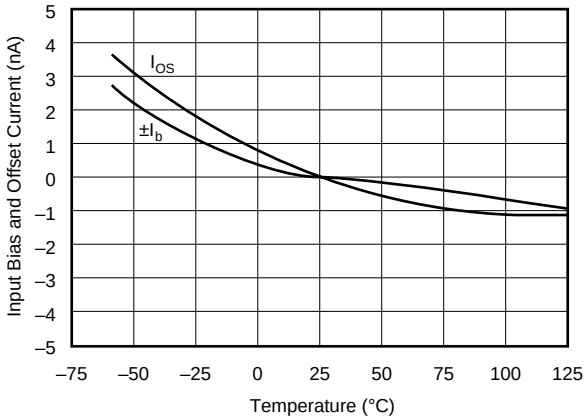
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

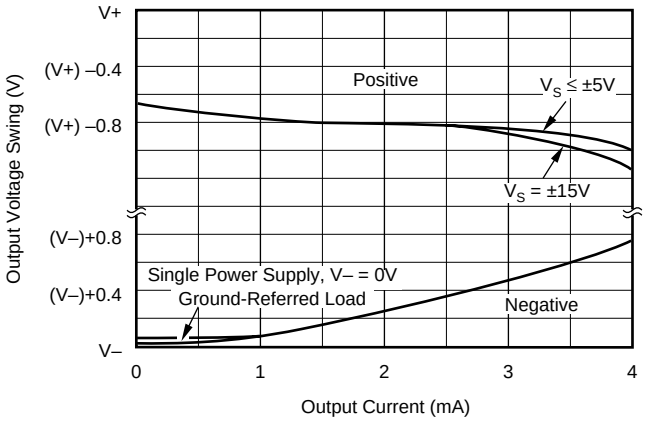
OFFSET VOLTAGE vs WARM-UP TIME



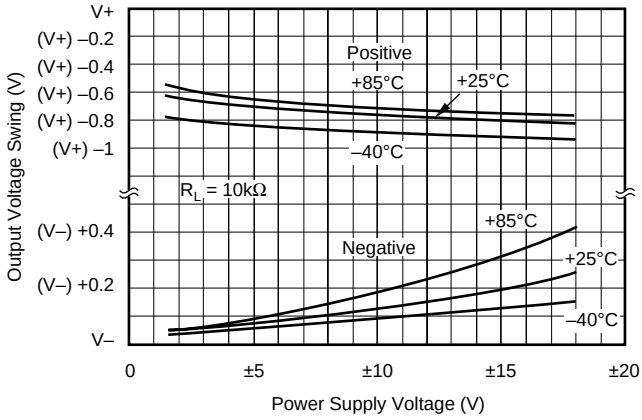
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



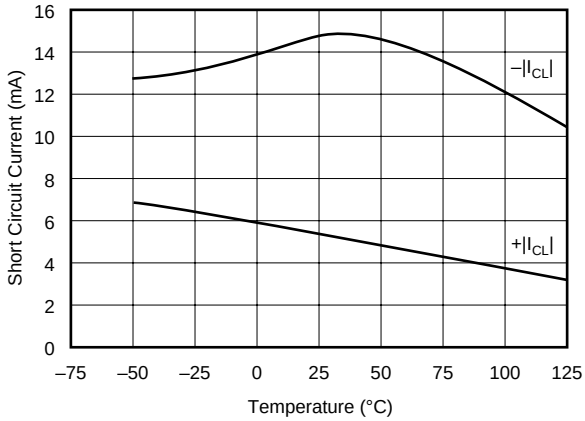
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



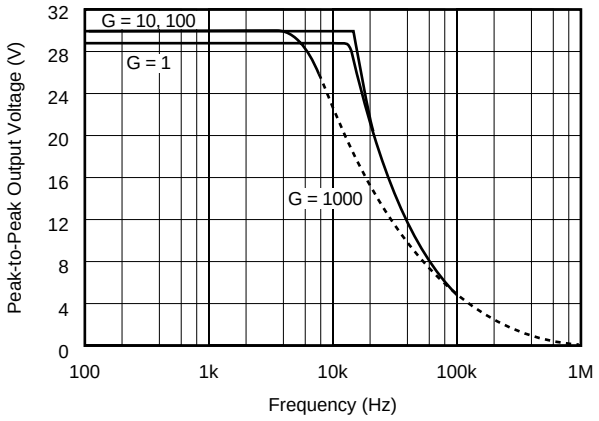
OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE



OUTPUT CURRENT LIMIT vs TEMPERATURE



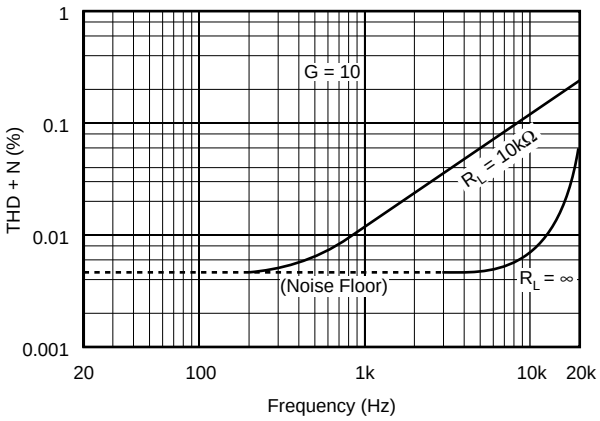
MAXIMUM OUTPUT SWING vs FREQUENCY



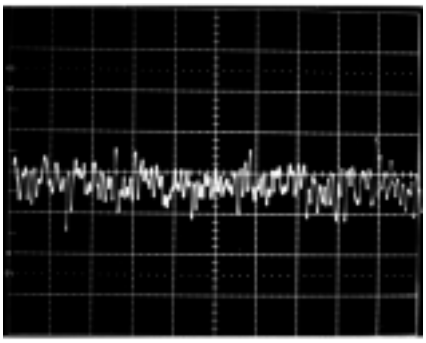
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

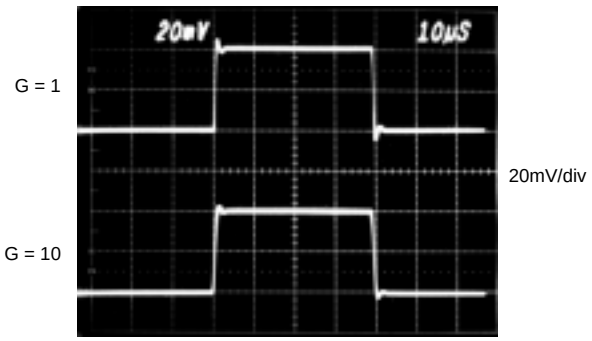
THD + N vs FREQUENCY



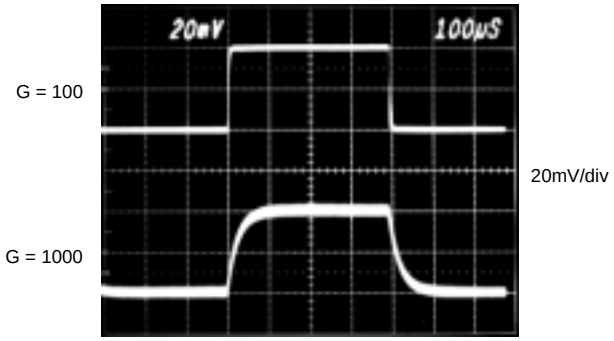
INPUT-REFERRED NOISE, 0.1Hz to 10Hz



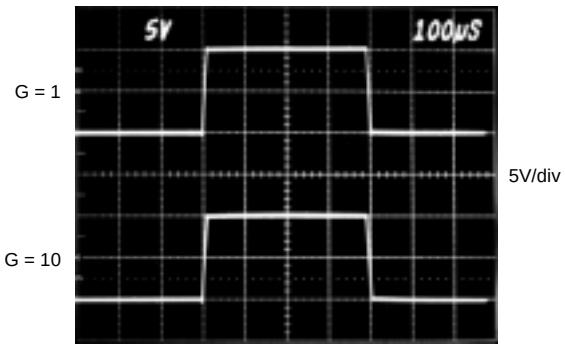
SMALL-SIGNAL RESPONSE



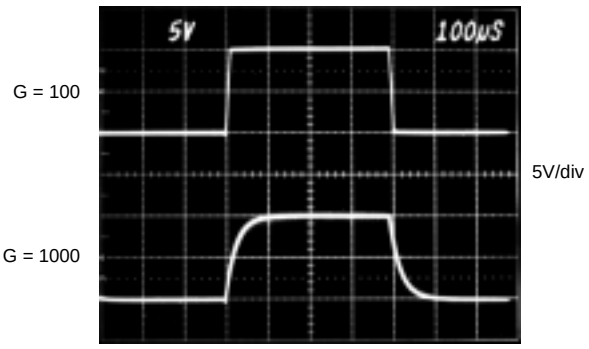
SMALL-SIGNAL RESPONSE



LARGE-SIGNAL RESPONSE



LARGE-SIGNAL RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 12Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA118 is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

$$G = 1 + \frac{50\text{k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3dB peaking at 500kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 300kHz or lower will produce a flat passband unity gain response.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

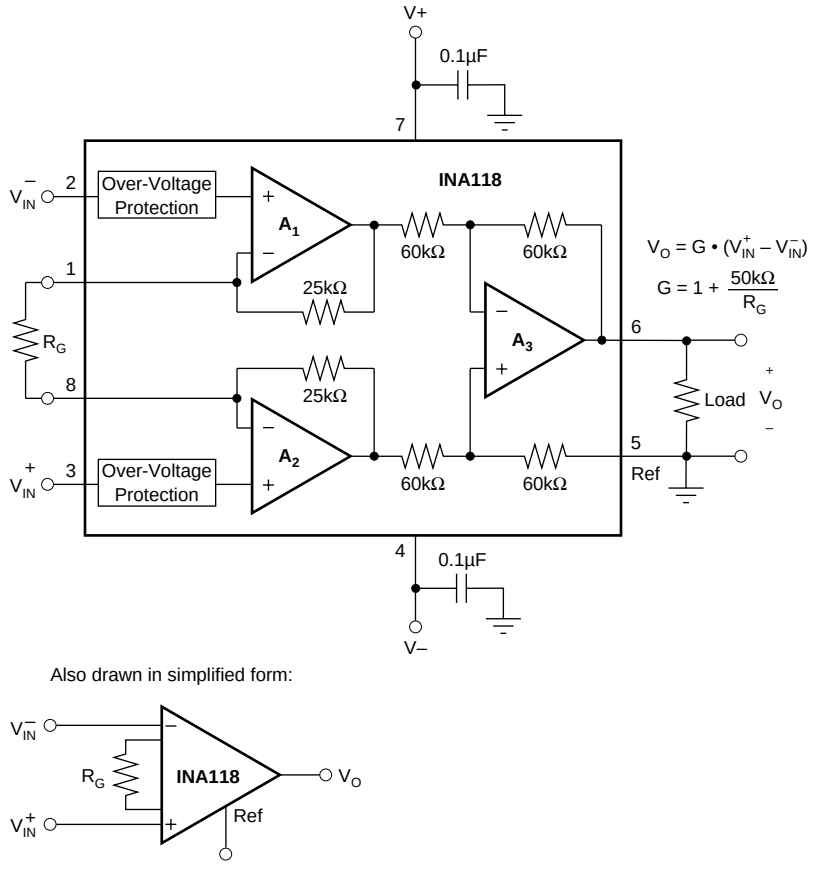


FIGURE 1. Basic Connections.

NOISE PERFORMANCE

The INA118 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA118 is approximately 0.28μVp-p measured from 0.1 to 10Hz (G≥100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

OFFSET TRIMMING

The INA118 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

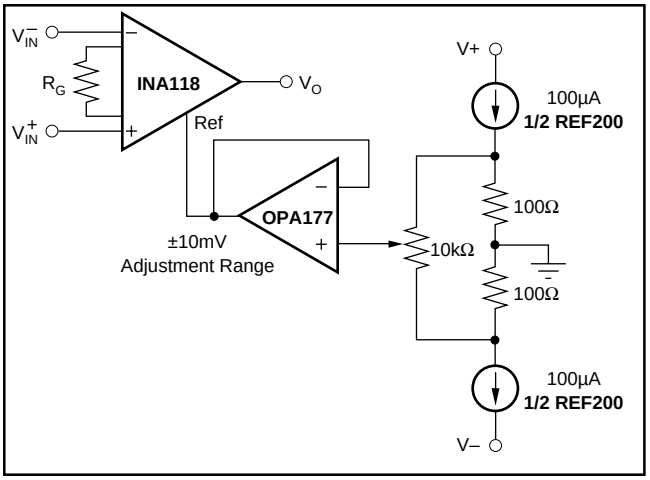


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA118 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±5nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA118 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

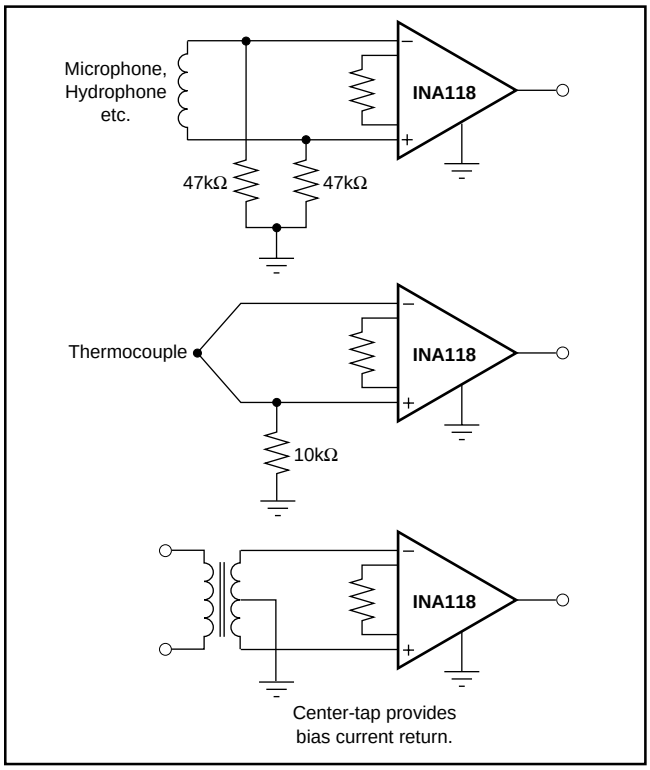


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6V below the positive supply voltage to 1V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA118 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA118 can be operated on power supplies as low as ±1.35V. Performance of the INA118 remains excellent with power supplies ranging from ±1.35V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for a various supply voltages and gains.

SINGLE SUPPLY OPERATION

The INA118 can be used on single power supplies of +2.7V to +36V. Figure 5 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage will demand an output voltage of 0V (ground). Actual output voltage swing is limited to approximately 35mV above ground, when the load is referred to ground as shown. The typical performance curve "Output Voltage vs Output Current" shows how the output voltage swing varies with output current.

With single supply operation, V_{IN}^+ and V_{IN}^- must both be 0.98V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 5. It shows the INA118, operating from a single 3V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier's inputs. Refer to the typical performance curve "Input Common-Mode Range vs Output Voltage" for 3V single supply operation.

INPUT PROTECTION

The inputs of the INA118 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

INSIDE THE INA118

Figure 1 shows a simplified representation of the INA118. The more detailed diagram shown here provides additional insight into its operation.

Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G, causing a signal current to flow through R_G, R_1 and R_2. The output difference amp, A_3, removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

Equations in the figure describe the output voltages of A_1 and A_2. The V_{BE} and IR drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 1V lower than the input voltages.

A_1 Out = $V_{CM} – V_{BE} – (10\mu A \bullet 25k\Omega) – V_O/2$
A_2 Out = $V_{CM} – V_{BE} – (10\mu A \bullet 25k\Omega) + V_O/2$
Output Swing Range A_1, A_2; (V+) – 0.65V to (V–) + 0.06V
Amplifier Linear Input Range: (V+) – 0.65V to (V–) + 0.98V

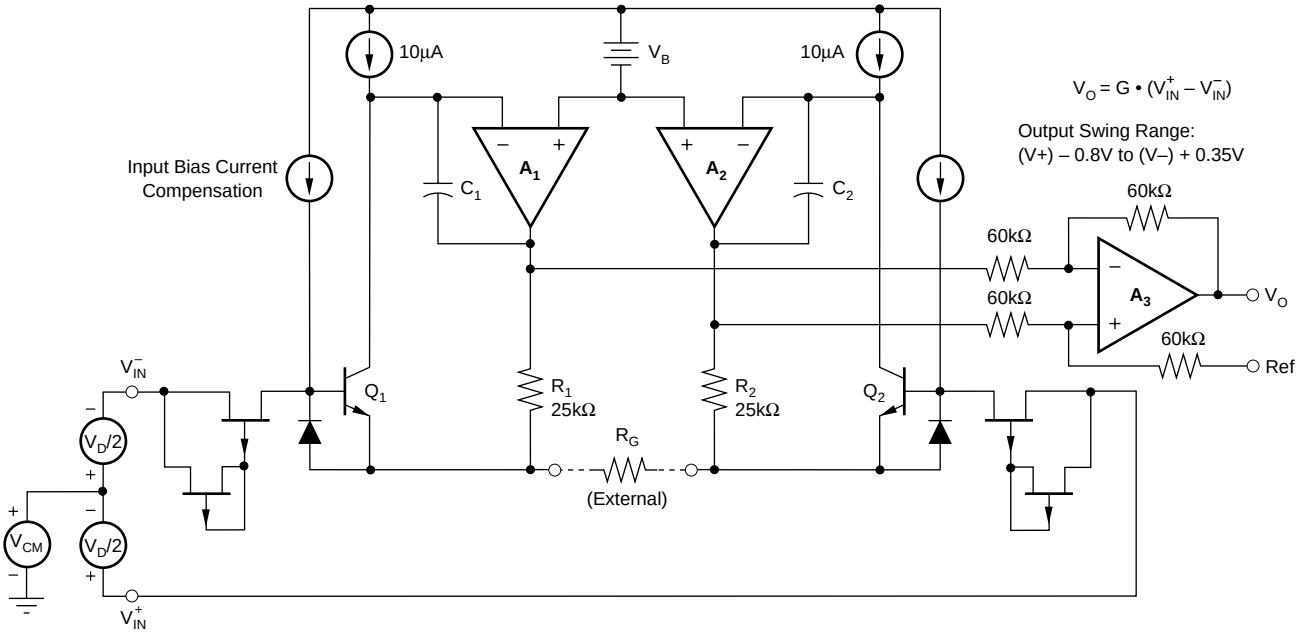


FIGURE 4. INA118 Simplified Circuit Diagram.

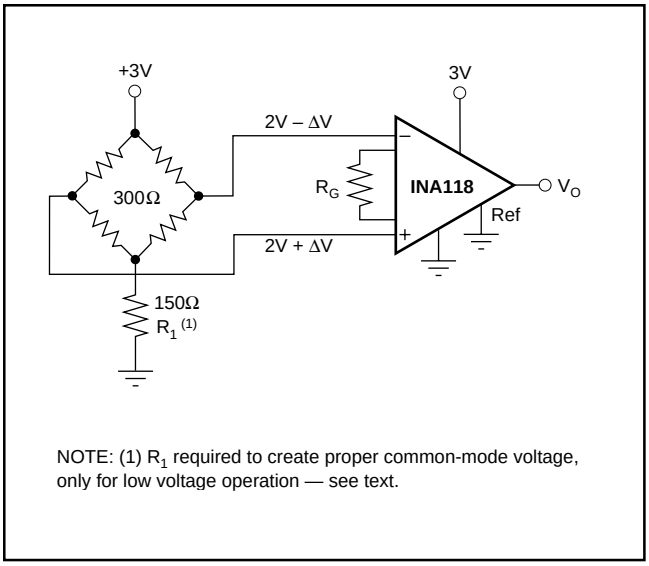


FIGURE 5. Single-Supply Bridge Amplifier.

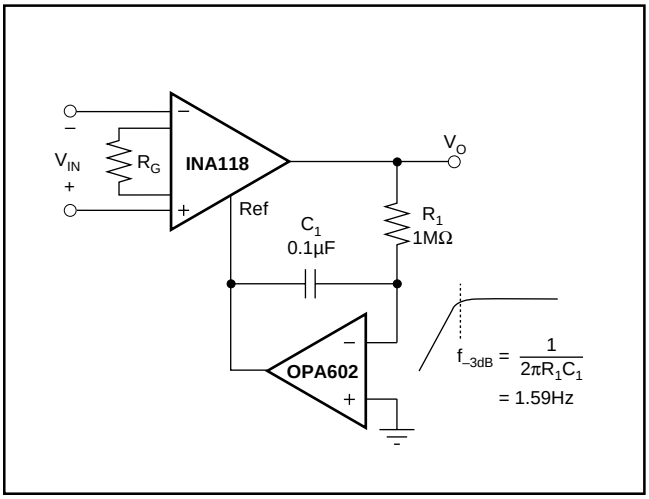
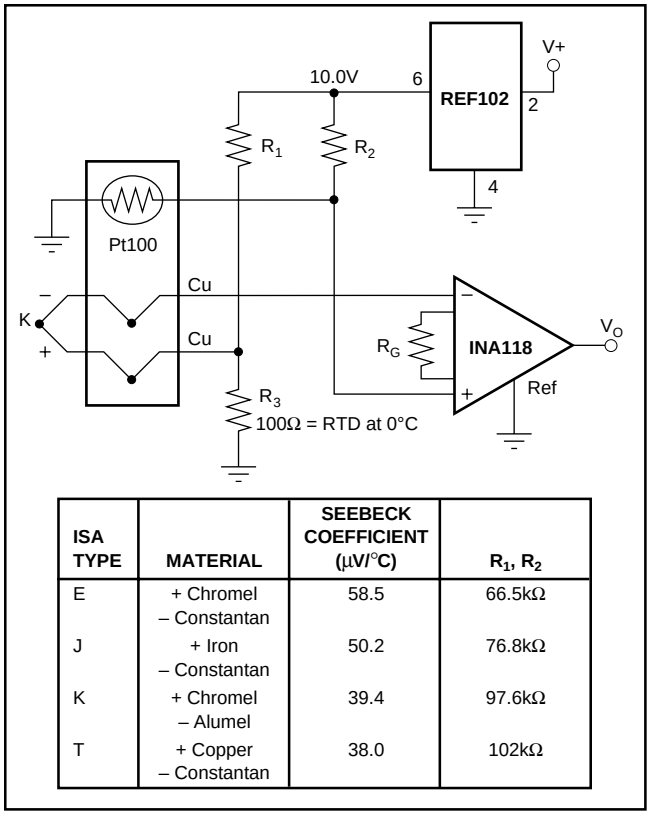
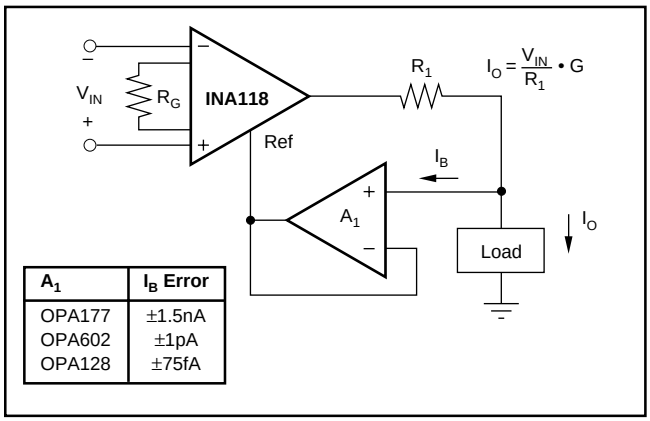


FIGURE 6. AC-Coupled Instrumentation Amplifier.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.



A_1	I_B Error
OPA177	±1.5nA
OPA602	±1pA
OPA128	±75fA

FIGURE 8. Differential Voltage to Current Converter.

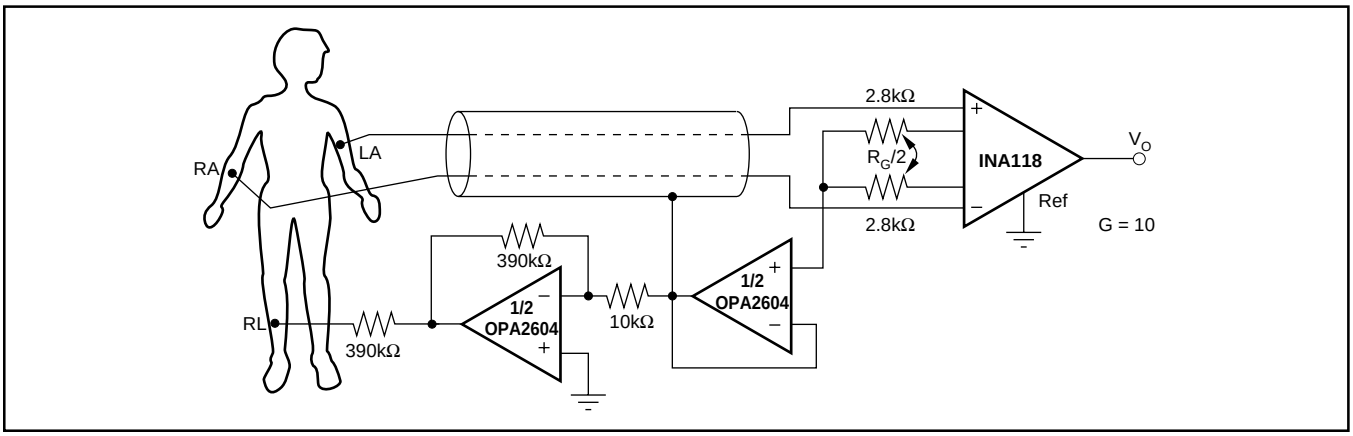


FIGURE 9. ECG Amplifier With Right-Leg Drive.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA118P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA118PB	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA118PBG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA118PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA118U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118UB/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA118UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

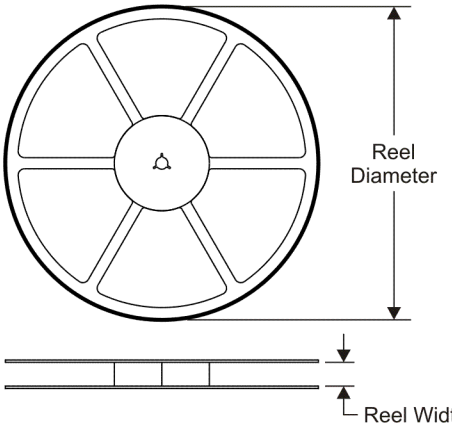
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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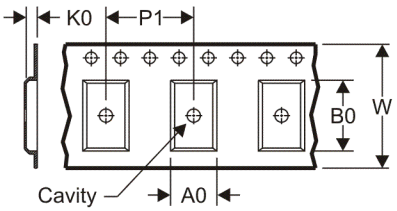
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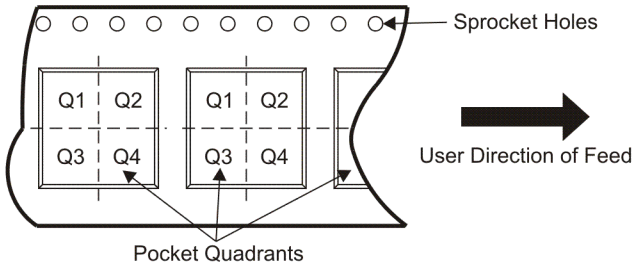


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

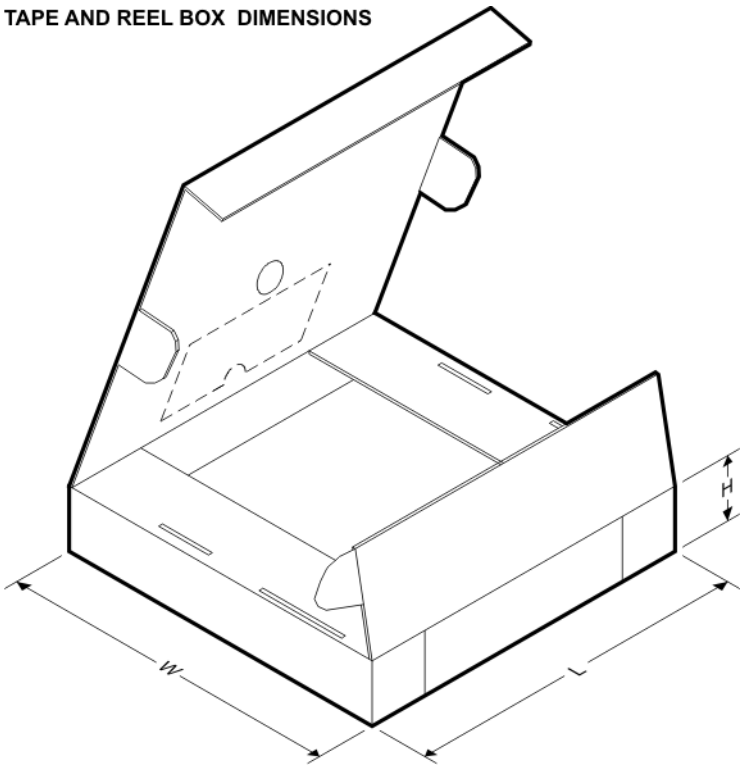
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA118U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
INA118UB/2K5	SOIC	D	8	2500	346.0	346.0	29.0

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