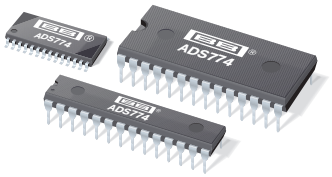
BURR - BROWN®



ADS774

Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- REPLACES ADC574, ADC674 AND ADC774 FOR NEW DESIGNS
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 8.5µs max OVER TEMPERATURE
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 120mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

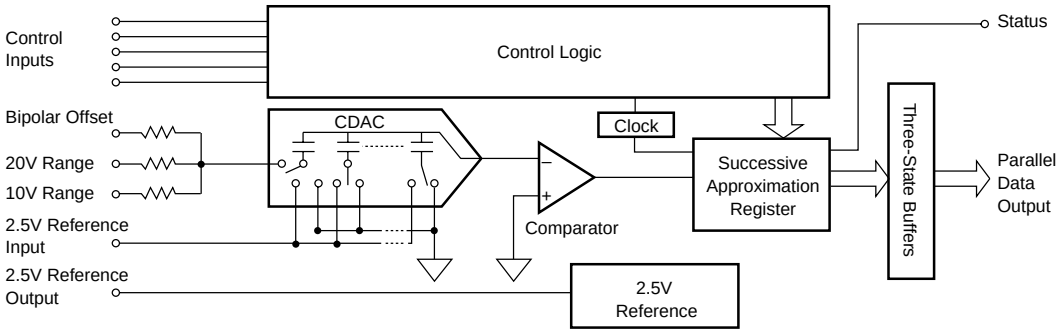
DESCRIPTION

The ADS774 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574, ADC674, and ADC774 models in most applications, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774 requires +5V, with –15V optional. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIP and 28-pin SOICs.



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SPECIFICATIONS

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX} , V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS774JE, JP, JU			ADS774KE, KP, KU			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	8.5	12		*	*		kΩ
±10V, 0V to +20V	35	50		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1] (adjustable to zero)			±0.25			*	% of FS [2]
No Missing Codes Resolution	12			12			Bits
T_{MIN} to T_{MAX} [3]							
Linearity Error			±1			±1/2	LSB
Full-Scale Calibration Error			±0.47			±0.37	% of FS
Unipolar Offset			±4			±3	LSB
Bipolar Offset			±12			±5	LSB
No Missing Codes Resolution	12			12			Bits
AC ACCURACY [4]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		–77	–72		*	–75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion (F_{IN1} = 20kHz, F_{IN2} = 23kHz)		–75			*		
TEMPERATURE COEFFICIENTS [5]							
Unipolar Offset		±1			*		ppm/°C
Bipolar Offset		±2			*		ppm/°C
Full-Scale Calibration		±12			*		ppm/°C
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration[6]							
+4.75V < V_{DD} < +5.25V							
Max Change			±1/2			*	LSB
CONVERSION TIME (Including Acquisition Time)							
t_{AQ} + t_C at 25°C:							
8-Bit Cycle		5.5	5.9		*	*	µs
12-Bit Cycle		7.5	8		*	*	µs
12-Bit Cycle, T_{MIN} to T_{MAX}:		8	8.5		*	*	µs
SAMPLING DYNAMICS							
Sampling Rate at 25°C	125			*			kHz
T_{MIN} to T_{MAX}	117			*			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			*		ns
With V_{EE} = 0V to –15V		1.6			*		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			*		ps, rms
With V_{EE} = 0V to –15V		10			*		ns, rms
Settling time to 0.01% for Full-Scale Input Change		1.4			*		µs

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS774JE, JP, JU			ADS774KE, KP, KU			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} (7)	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} (7) (V_{EE} = –15V)		–1			*		mA
I_{DD}		+15	+24		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		75	120		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating:	–40		+85	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

* Same specification as ADS774JE, JP, JU.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at T_{MIN} and T_{MAX}. (4) Based on using V_{EE} = +5V, which is the Control Mode. See the section "S/H Control Mode and ADC774 Emulation Mode." (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common	$+V_{DD}$ to –16.5V
V_{DD} to Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	–0.5V to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{DD}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Plastic DIPs	100°C/W
SOIC	100°C/W

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

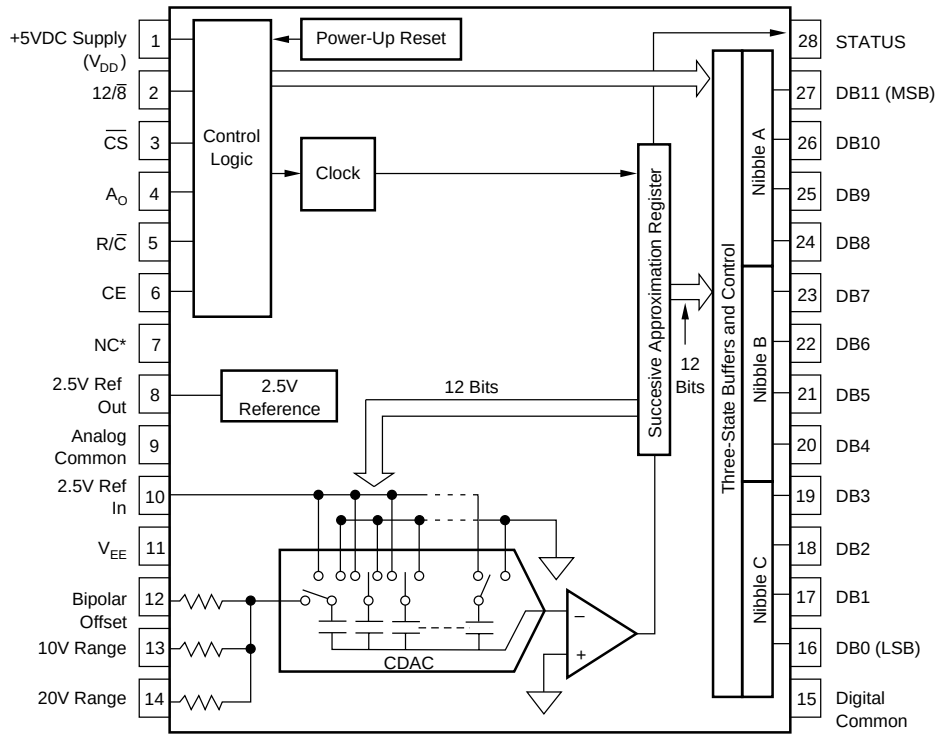
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR	PACKAGE	PACKAGE DRAWING NUMBER[2]
ADS774JE	68dB	0°C to +70°C	±1LSB	28-Pin 0.3" Plastic DIP	246
ADS774KE	70dB	0°C to +70°C	±1/2LSB	28-Pin 0.3" Plastic DIP	246
ADS774JP	68dB	0°C to +70°C	±1LSB	28-Pin 0.6" Plastic DIP	215
ADS774KP	70dB	0°C to +70°C	±1/2LSB	28-Pin 0.6" Plastic DIP	215
ADS774JU	68dB	0°C to +70°C	±1LSB	28-Lead SOIC	217
ADS774KU	70dB	0°C to +70°C	±1/2LSB	28-Lead SOIC	217

NOTES: (1) SINAD is Signal-to-(Noise + Distortion) expressed in dB. (2) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

CONNECTION DIAGRAM

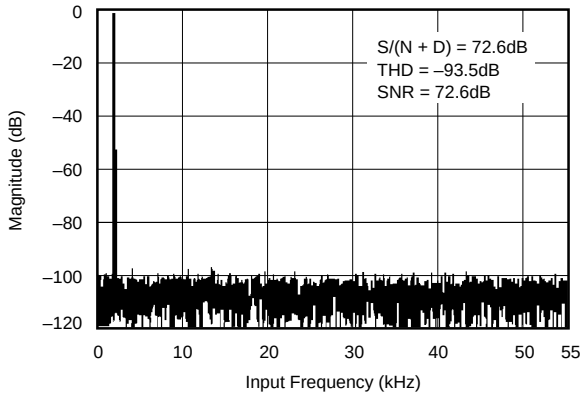


*Not Internally Connected

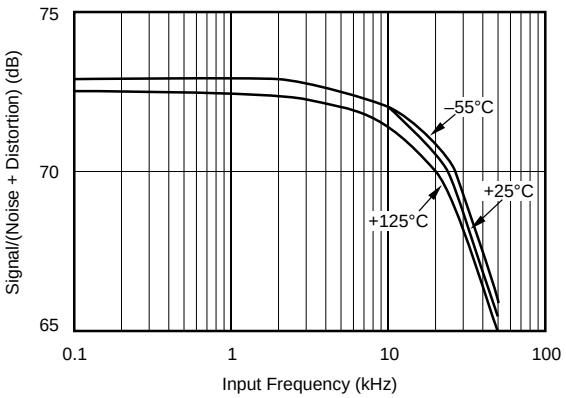
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 110kHz; unless otherwise specified. All plots use 4096 point FFTs.

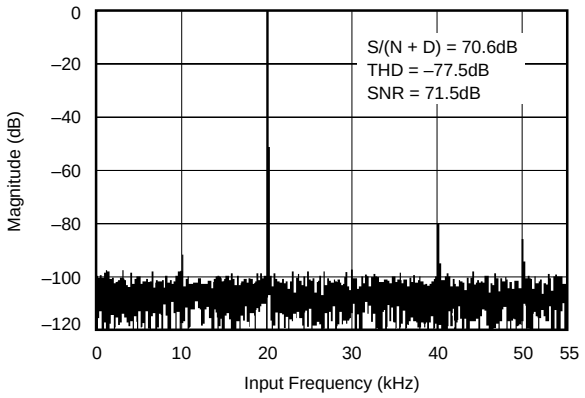
FREQUENCY SPECTRUM (±10V, 2kHz Input)



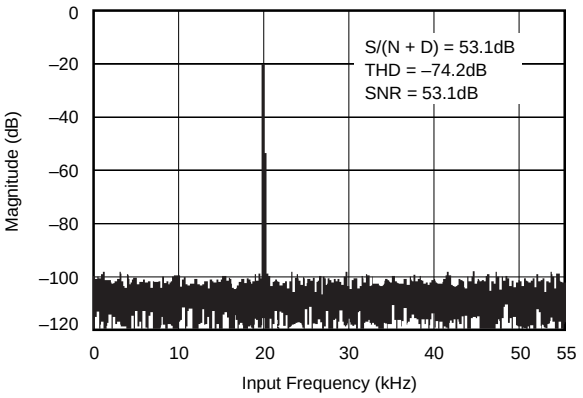
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



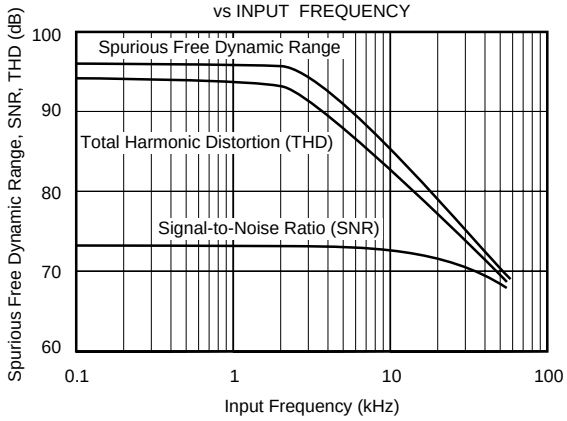
FREQUENCY SPECTRUM (±10V, 20kHz Input)



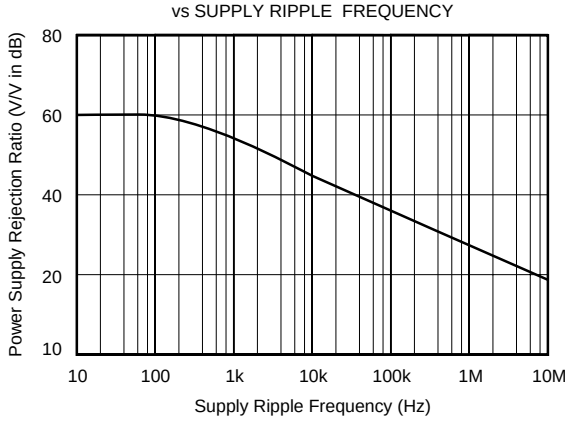
FREQUENCY SPECTRUM (±1V, 20kHz Input)



SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY



POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY



THEORY OF OPERATION

In the ADS774, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

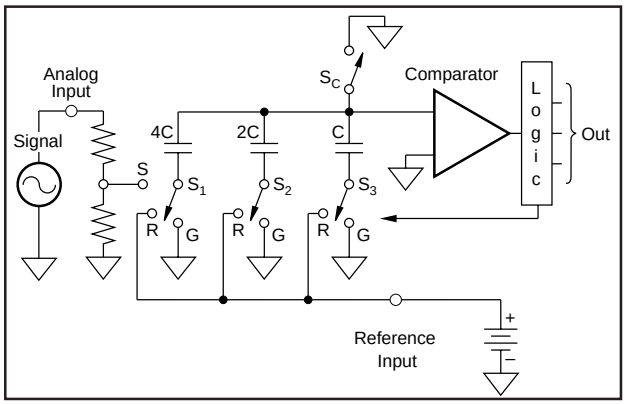


FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_C is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_C is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the ADS774 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS774 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS774.

The ADS774 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS774 is designed to complete a conversion and accurately acquire a new signal in 8.5µs max over the full operating temperature range, so that conversions can take place at a full 117kHz.

CONTROLLING THE ADS774

The Burr-Brown ADS774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are

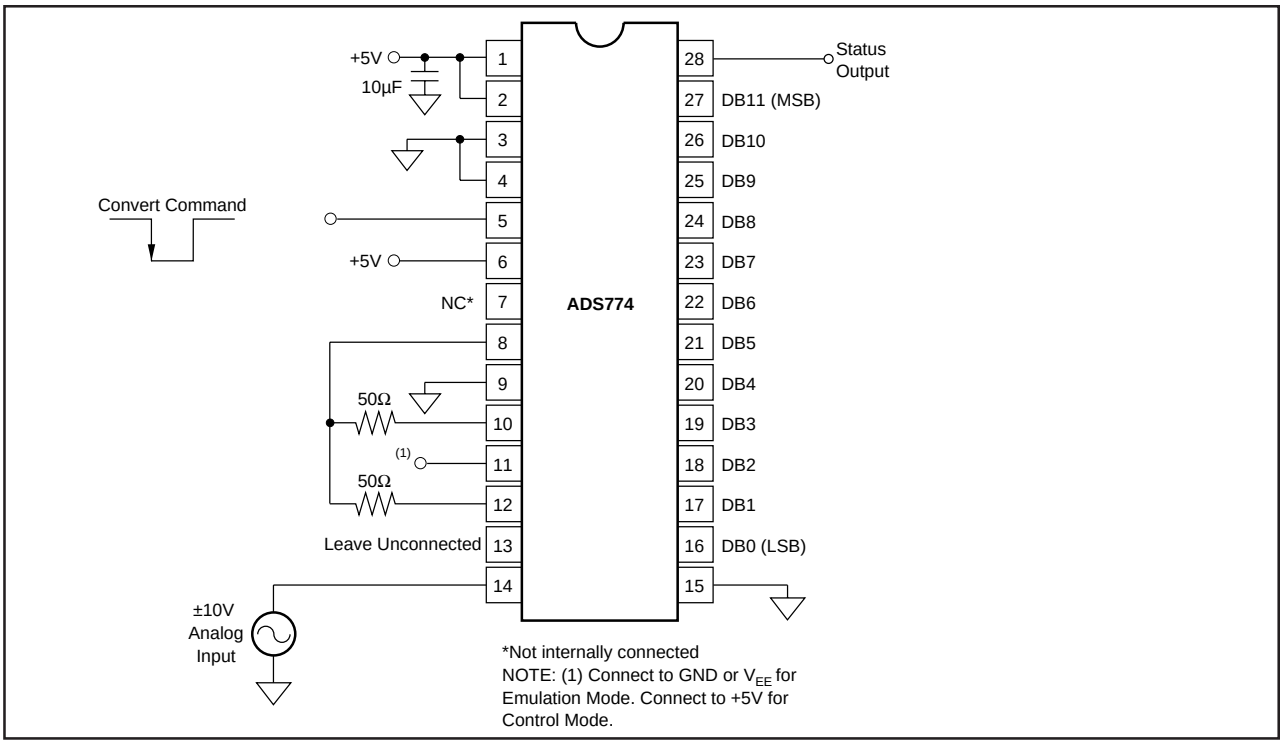


FIGURE 2. Basic ±10V Operation.

presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs ($\overline{CE}$, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	±5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB) n = 8 n = 12	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	 + Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (– Full-Scale Calibration)	 +10V – 3/2LSB 0V – 1/2LSB –10V + 1/2LSB	 +5V – 3/2LSB 0V – 1/2LSB –5V + 1/2LSB	 +10V – 3/2LSB +5V – 1/2LSB 0V +1/2LSB	 +20V – 3/2LSB +10V – 1/2LSB 0V +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH (“1”) to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW (“0”) to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert (“1” = read) (“0” = convert)	Must be LOW (“0”) to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH (“1”) to read output data. 0-1 edge may be used to initiate a read operation.
A_O (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_O selects 8-bit (A_O = “1”) or 12-bit (A_O = “0”) conversion mode. When reading output data in two 8-bit bytes, A_O = “0” accesses 8 MSBs (high byte) and A_O = “1” accesses 4 LSBs and trailing “0s” (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select (“1” = 12 bits) (“0” = 8 bits)	When reading output data, 12/$\overline{8}$ = “1” enables all 12 output bits simultaneously. 12/$\overline{8}$ = “0” will enable the MSBs or LSBs as determined by the A_O line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the HIGH or LOW condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS774 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

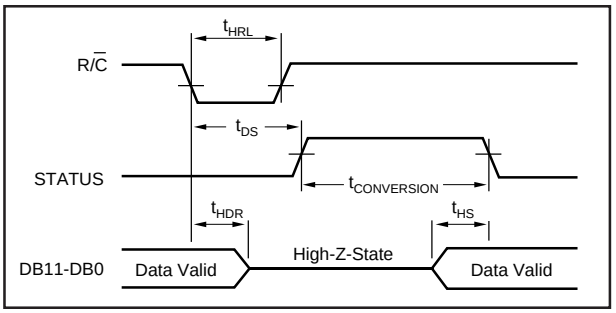


FIGURE 3. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

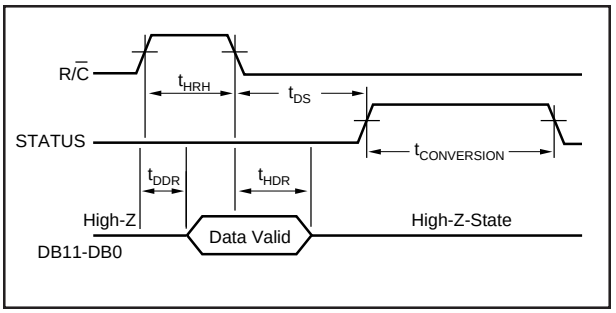


FIGURE 4. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	$\overline{CE}$ Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_O to CE setup	0			ns
t_{HAC}	A_O valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_O to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_O valid after CE low	50			ns
t_{HS}	STATUS delay after data valid	75	150	375	ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

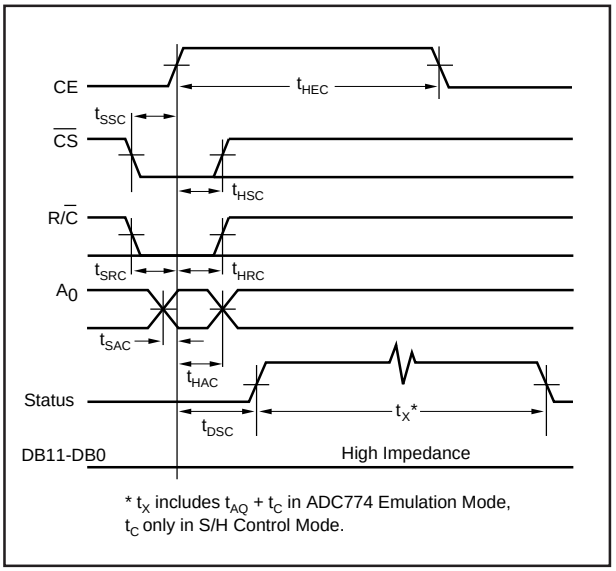


FIGURE 5. Conversion Cycle Timing.

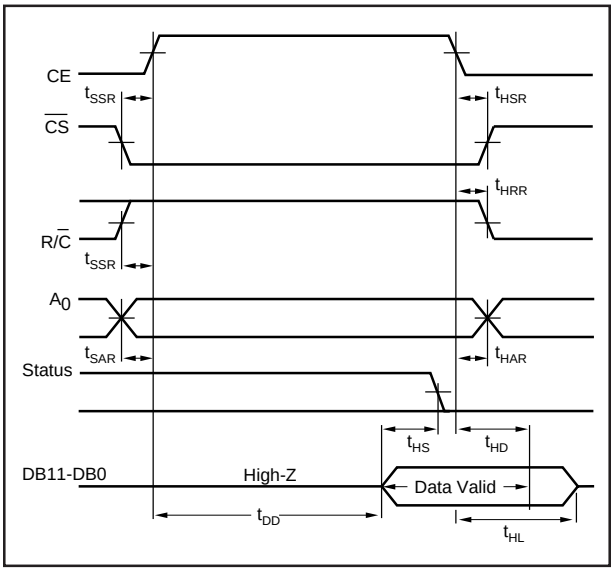


FIGURE 6. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

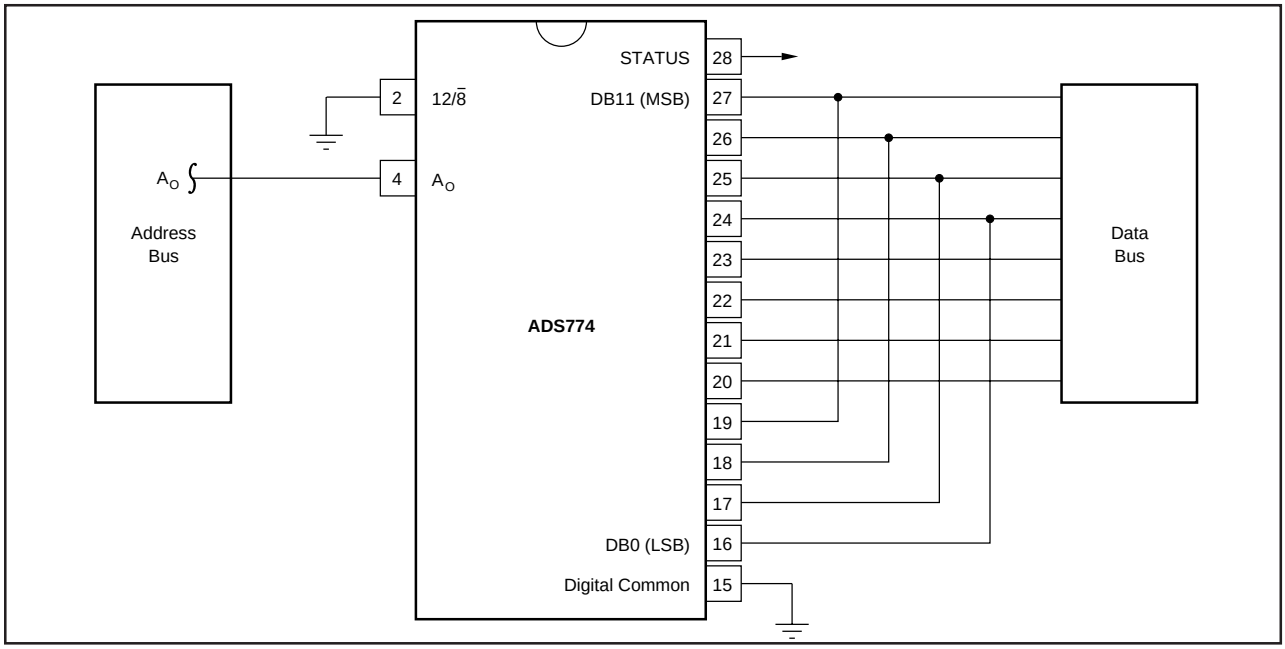


FIGURE 8. Connection to an 8-Bit Bus.

S/H CONTROL MODE AND ADC774 EMULATION MODE

The Emulation Mode allows the ADS774 to be dropped into most existing ADC774 sockets without changes to other system hardware or software. In existing sockets, the analog input is held stable during the conversion period so that accurate conversions can proceed, but the input can change rapidly at any time before the conversion starts. The Emulation Mode uses the stability of the analog input during the conversion period to both acquire and convert in a maximum of 8µs (8.5µs over temperature.) In fact, system throughput can be increased, since the input to the ADS774 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC774s.

The Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS774 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode, it is assumed that during the required 1.4µs acquisition time the signal is not changing faster than the ADS774 can track. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command. This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized in the Control Mode, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, a delay time is introduced between the convert command and the start of conversion to allow the ADS774 enough time to acquire the input signal before converting. This increases the effective aperture delay time from 0.02µs to 1.6µs, but allows the ADS774 to replace the ADC774 in most circuits without additional changes. In designs where the input to the ADS774 is changing rapidly in the 200ns prior to a convert command, system performance may be enhanced by delaying the convert command by 200ns.

When using the ADS774 in the Emulation Mode to replace existing converters in current designs, a sample/hold amplifier often precedes the converter. In these cases, no additional delay in the convert command will be needed. The existing sample/hold will not be slewing excessively when going from the sample mode to the hold mode prior to a conversion.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

The speed of the ADS774 requires special caution regarding whichever input pin is unused. For 10V input ranges, pin 14 (20V Range) must be unconnected, and for 20V input ranges, pin 13 (10V Range) must be unconnected. In both cases, the unconnected input should be shielded with ground plane to reduce noise pickup.

In particular, the unused input pin should not be connected to any capacitive load, including high impedance switches. Even a few pF on the unused pin can degrade acquisition time.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS774.

POWER SUPPLY DECOUPLING

On the ADS774, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC774 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC774 socket, the –15V on pin 11 selects the ADC774 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V) MIN	TYP	MAX	ADC774 EMULATION MODE (Pin 11 Connected to 0V to –15V) MIN	TYP	MAX	UNITS
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		8	8.5		8	8.5	µs
	8-bit Conversions		6	6.3		6	6.3	µs
t_C	Conversion Time:							
	12-bit Conversions		6.4			6.4		µs
	8-bit Conversions		4.4			4.4		µs
t_{AQ}	Acquisition Time		1.4			1.4		µs
t_{AP}	Aperture Delay		20			1600		ns
t_J	Aperture Uncertainty		0.3			10		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.

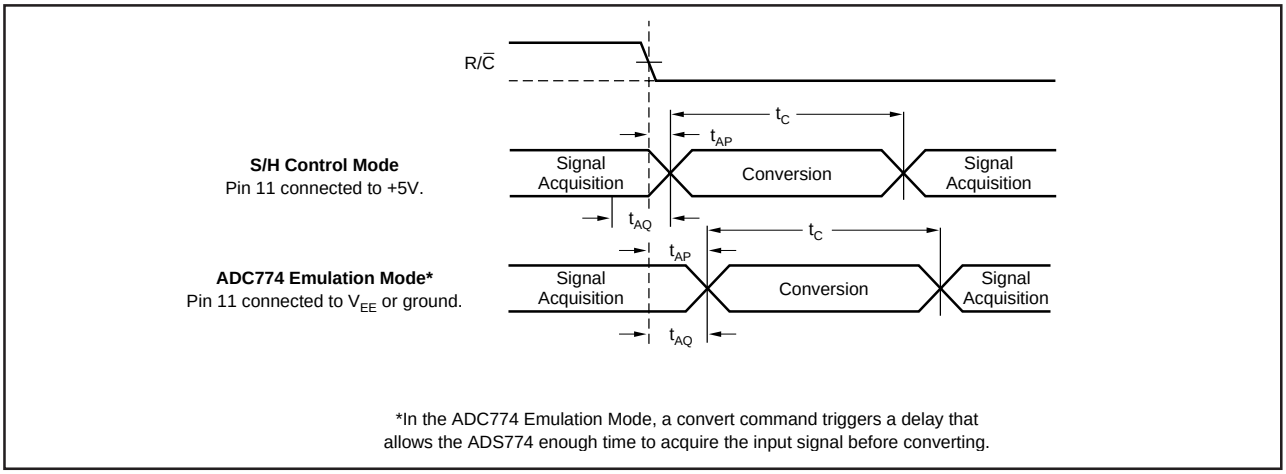


FIGURE 9. Signal Acquisition and Conversion Timing.

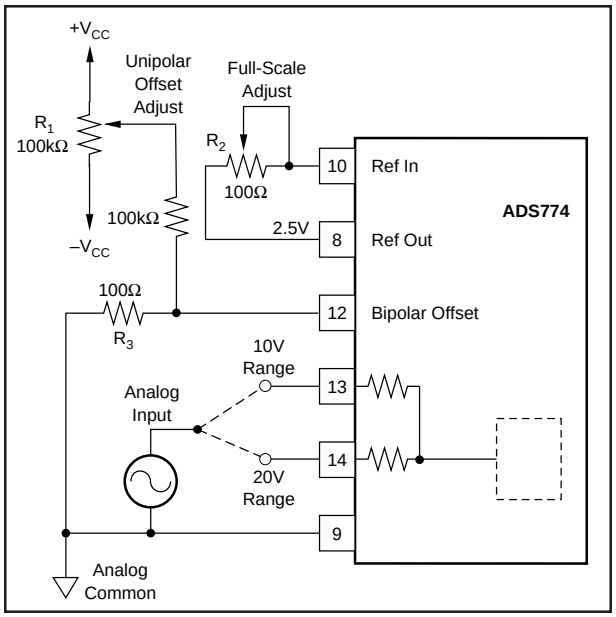


FIGURE 10. Unipolar Configuration.

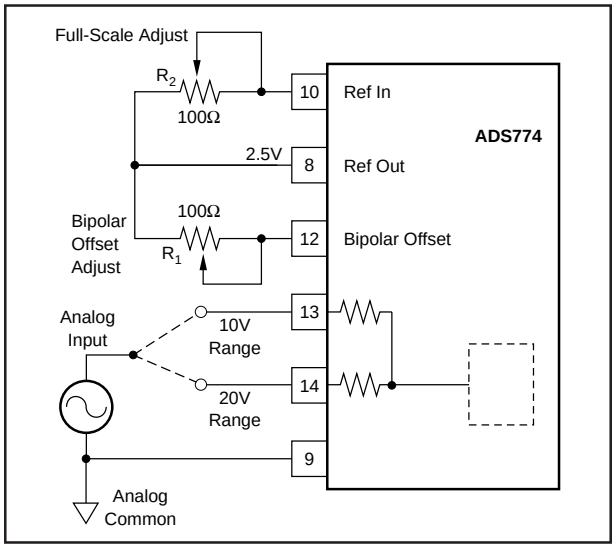


FIGURE 11. Bipolar Configuration.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS774 is typically 50kΩ in the 20V ranges and 12kΩ in the 10V ranges. This is significantly higher than that of traditional ADC774 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS774. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high impedance node as compared with traditional ADC774 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS774 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to pin 9, analog common. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (42kΩ + 42kΩ || 10.5kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide the same offset adjust response as that of traditional ADC774 architectures without changing the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS774 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is

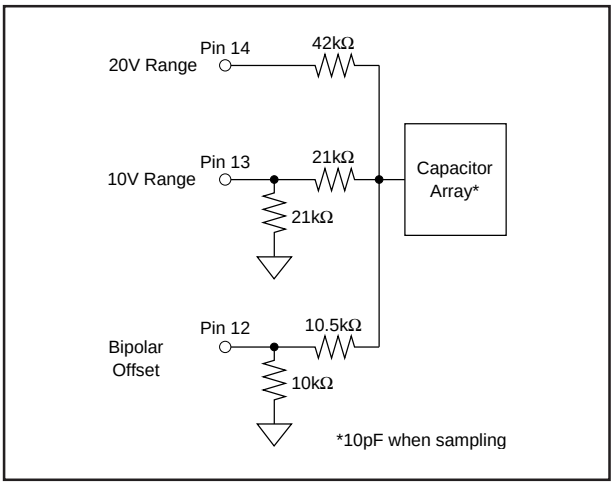


FIGURE 12. ADS774 Input Structure.

where +12V or +15V is supplied on traditional ADC774s. Pin 11, the –12V or –15V supply input on traditional ADC774s, is used only as a logic input on the ADS774. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS774, and this resistor will add 10mW to 15mW to the power consumption of the ADS774 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS774 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS774 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω 1% metal film resistor and connect pin 12 to pin 9, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 11 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS774JE	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774JEG4	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774JP	ACTIVE	PDIP	NTD	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774JPG4	ACTIVE	PDIP	NTD	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774JU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HRS	
ADS774JU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS774JU/1KE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS774JUE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HRS	
ADS774KE	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774KEG4	ACTIVE	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774KP	ACTIVE	PDIP	NTD	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774KPG4	ACTIVE	PDIP	NTD	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
ADS774KU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HRS	
ADS774KU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS774KU/1KE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS774KUE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HRS	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

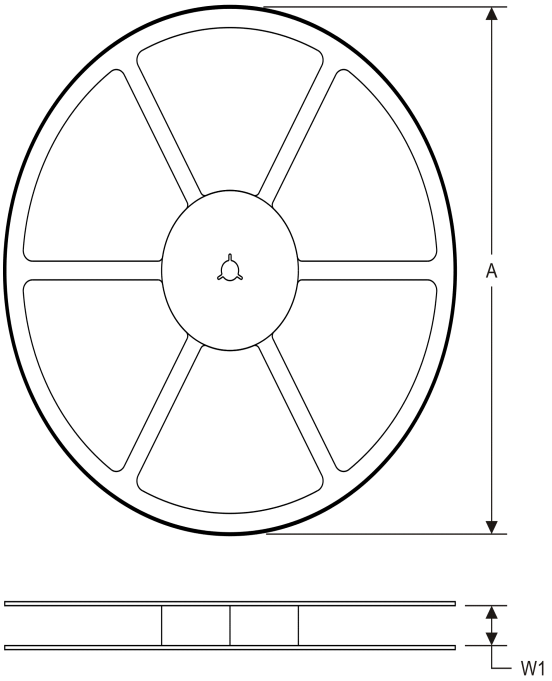
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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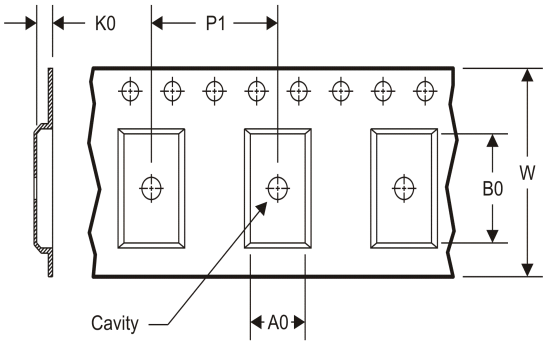
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



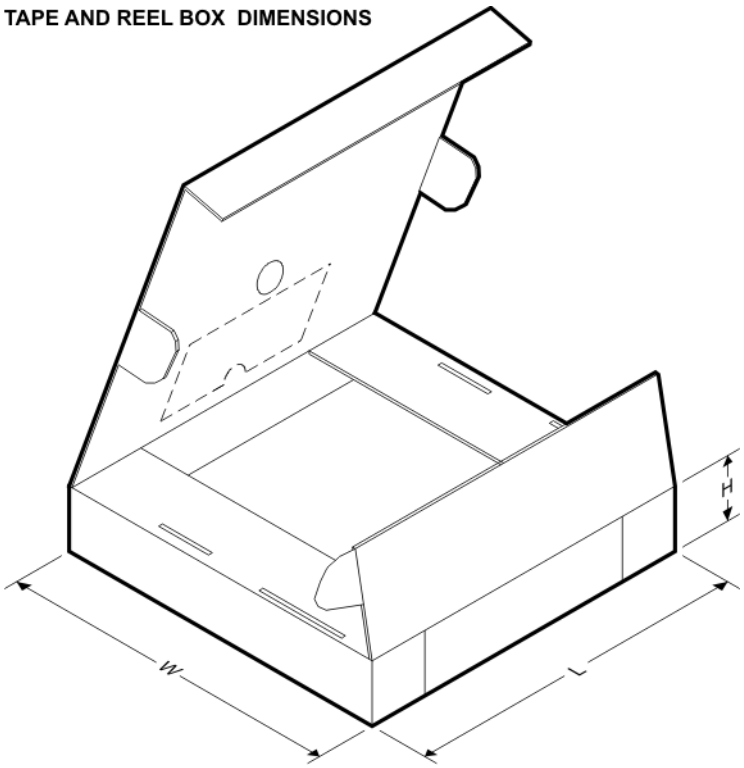
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS774JU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
ADS774KU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

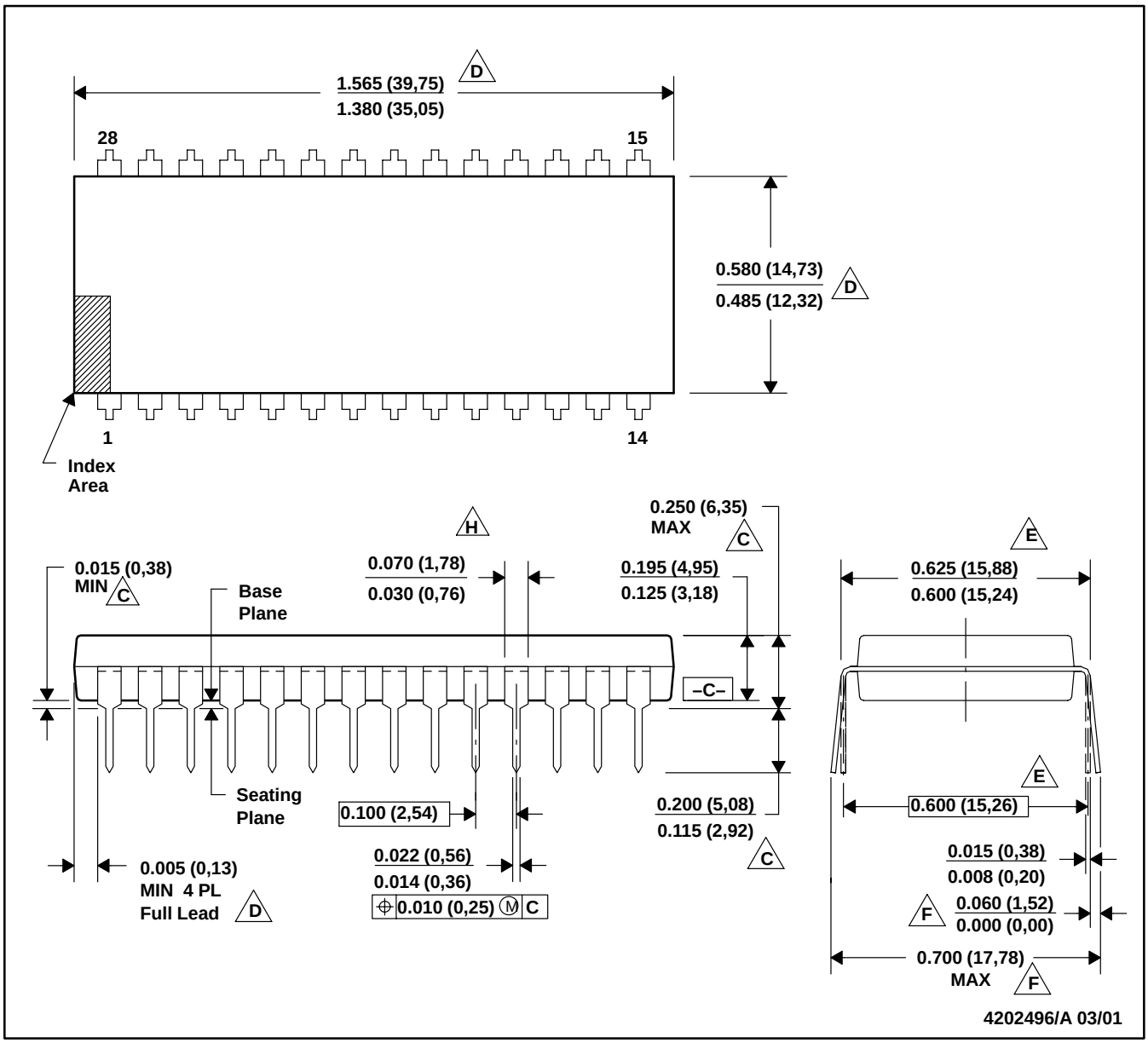


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS774JU/1K	SOIC	DW	28	1000	367.0	367.0	55.0
ADS774KU/1K	SOIC	DW	28	1000	367.0	367.0	55.0

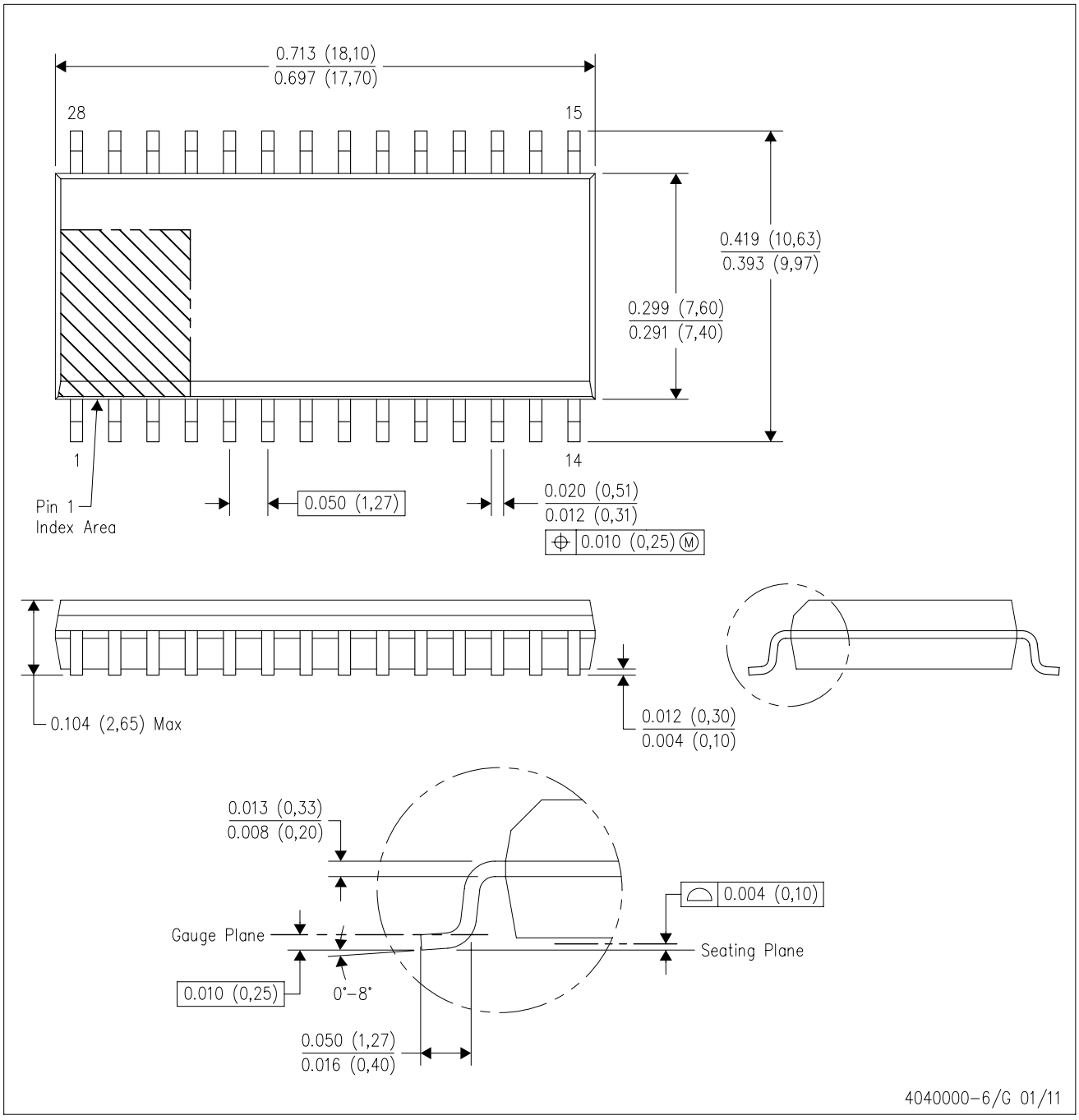
MPDI056 – APRIL 2001

NTD (R-PDIP-T28) **PLASTIC DUAL-IN-LINE**



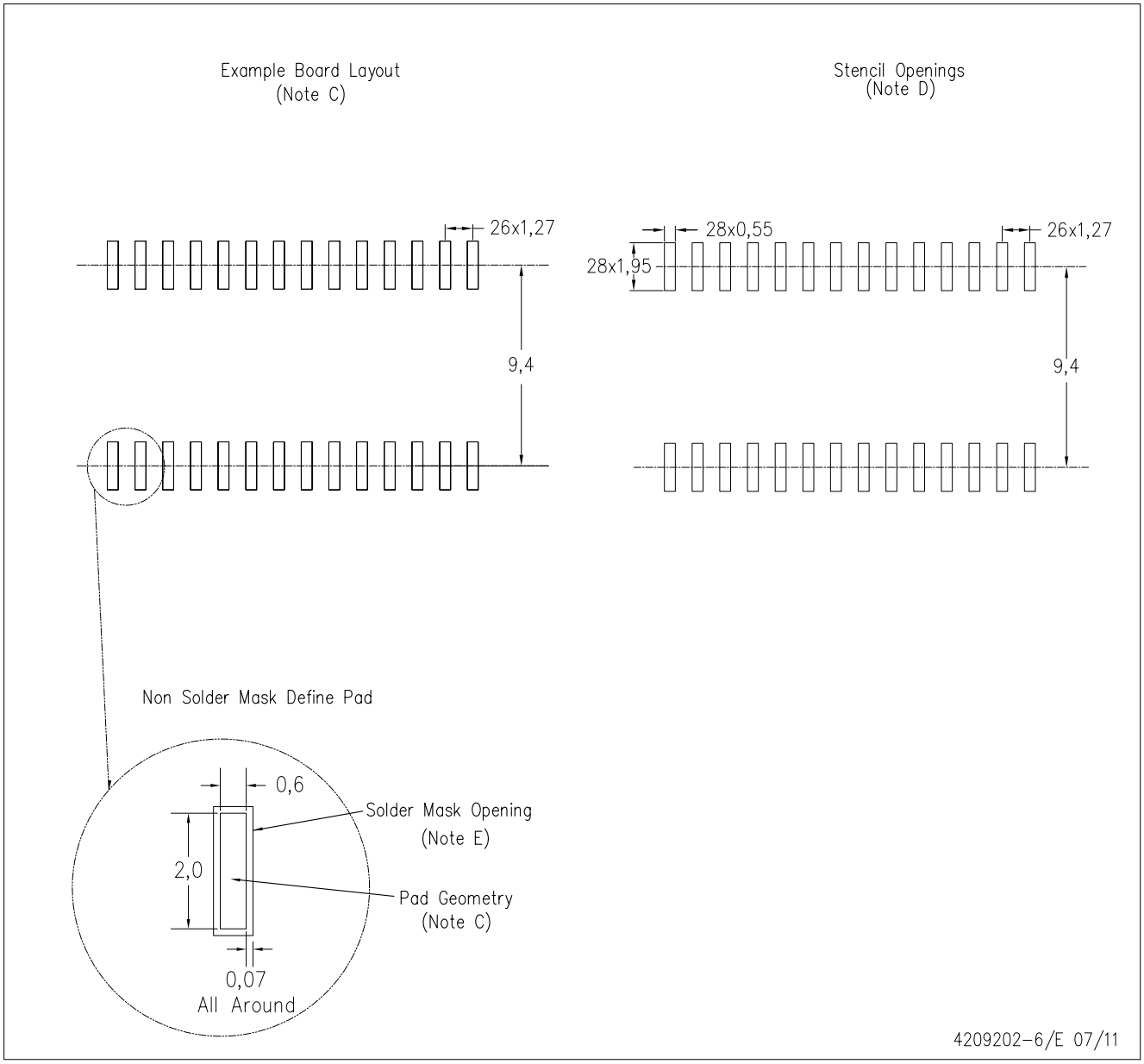
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. Pointed or rounded lead tips are preferred to ease insertion.
H. Maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
I. Distance between leads including dambar protrusions to be 0.005 (0,13) minumum.
J. A visual index feature must be located within the cross-hatched area.
K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
L. Controlling dimension in inches.
M. Falls within JEDEC MS-011-AB.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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