UCC5680
9-LINE LVD ONLY SCSI TERMINATOR WITH INTEGRATED SPI-3 DELAYS

SLUS313D − MARCH 1999 - REVISED NOVEMBER 2003

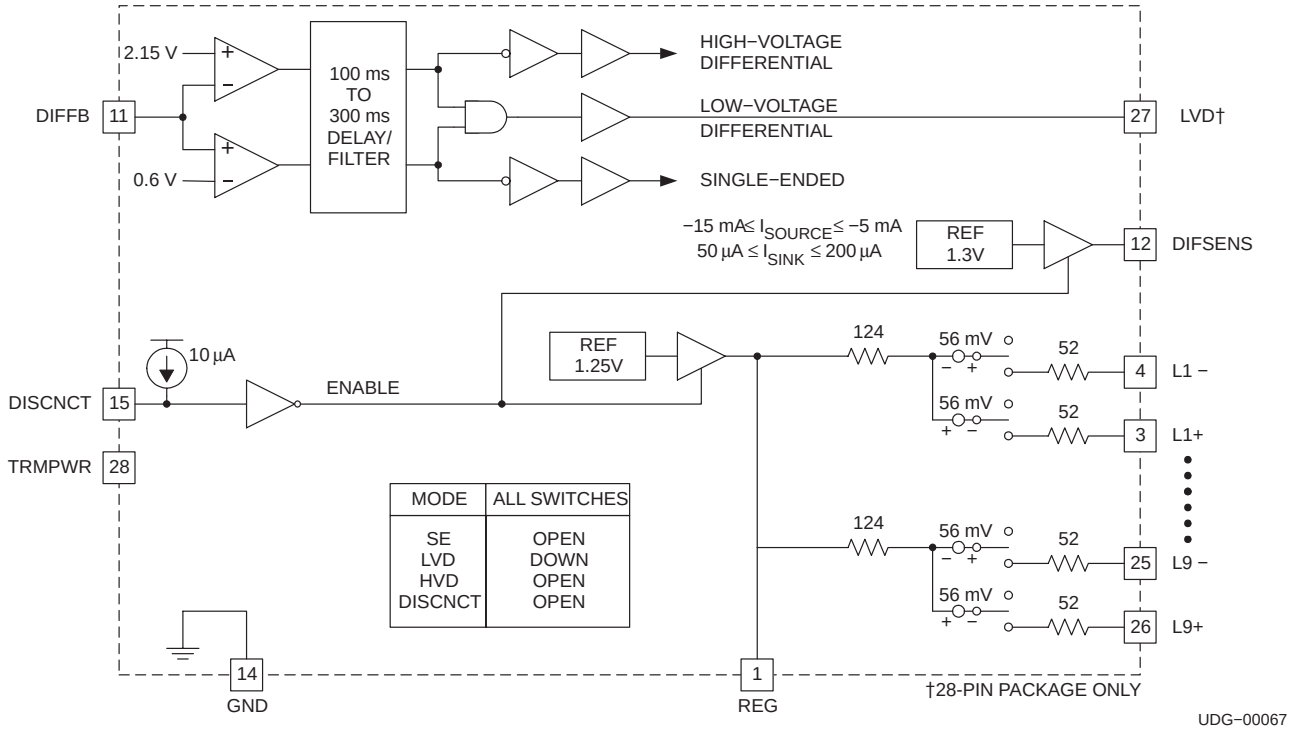
- **LVD-Only Active Termination**
- **2.7 V to 5.25 V Operation**
- **Differential Failsafe Bias**
- **Built-In SPI-3 Mode Change Filter/Delay**
- **Standards Supported: SPI-2, SPI-3, SPI-4, Ultra2 (Fast 40), Ultra3/Ultra160 (Fast 80) and Ultra320 (Fast 160)**

description

The UCC5680 is an LVD-only Small Computer System Interface (SCSI) terminator that integrates the mode change delay function required by the SPI-3 specification. The device senses what types of SCSI drivers are present on the bus via the voltage on the DIFFSENS SCSI control line. Single-ended (SE) and high-voltage differential (HVD) SCSI drivers (EIA485) are not supported. If the chip detects the presence of an SE or HVD SCSI driver, it disconnects itself by switching all terminating resistors off the bus and enters a high-impedance state. The terminator can also be commanded to disconnect the terminating resistors with the DISCNCT input. Impedance is trimmed for accuracy and maximum effectiveness. Bus lines are biased to a failsafe state to ensure signal integrity.

The UCC5680 is offered in both 24-pin and 28-pin TSSOP (PW) packages for a temperature range of 0°C to 70°C.

functional block diagram



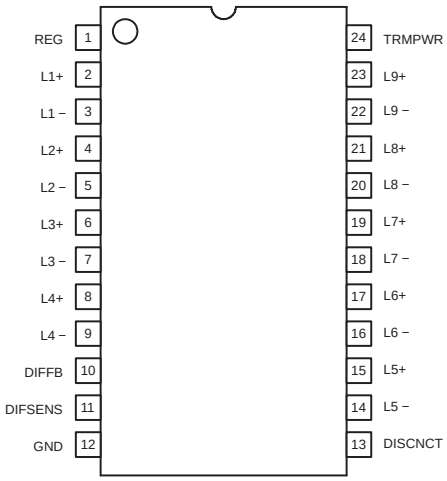
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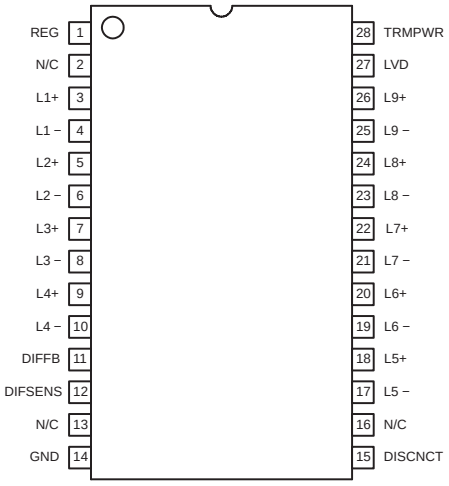
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TSSOP PACKAGE (TOP VIEW)

PW PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



ordering information

$T_A = T_J$	PACKAGED DEVICE†	
	TSSOP-24 (PW)	TSSOP-28 (PW)
0°C to 70°C	UCC5680PW24	UCC5680PW28

‡ The PW package is available taped and reeled in quanities of 2,000. Add TR suffix to device type (e.g. UCC5680PWTR) to order quantities of 2,000 devices per reel.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

TERMPWR Voltage . . . . . 6 V
Signal Line Voltage . . . . . 0 V to 5 V
Package Dissipation . . . . . 0.5 W
Storage Temperature . . . . . −65°C to 150°C
Junction Temperature . . . . . −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

TERMPWR Voltage . . . . . 2.7 V to 5.25 V
Operating Temperature Range . . . . . 0°C to 70°C

electrical characteristics over recommended operating free-air temperature range, $T_A = T_J = 0°C$ to $70°C$, TRMPWR = 2.7 V to 5.25 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRMPWR Supply Current Section					
TRMPWR supply current	LVD Mode (No Load)			35	mA
	Disabled Mode			500	µA
Regulator Section					
Regulator output voltage	$0.5\ V \le V_{CM} \le 2.0$, See Note 1	1.15	1.25	1.35	V
Regulator short-circuit source current	$V_{REG} = 0$ V		-100	-80	mA
Regulator short-circuit sink current	$V_{REG} = 3.0$ V	80	100		mA
DIFSENS Output Section					
Output voltage	$-5\ mA \le I_{DIFSENS} \le 50\ \mu A$	1.2	1.3	1.4	V
Short-circuit source current	$V_{DIFSENS} = 0$ V	-15		-5	mA
Short-circuit sink current	$V_{DIFSENS} = 2.75$ V	50		200	µA
Differential Termination Section (Applies to each line pair , 1-9, in LVD mode)					
Differential impedance		100	105	110	Ω
Common-mode impedance	L+ and L- shorted together, See Note 2	110	150	165	Ω
Differential bias voltage		100		125	mV
Common-mode bias voltage	L+ and L- shorted together	1.15	1.25	1.35	V
Disconnected Termination Section (Applies to each line pair , 1-9, in DISCNCT, SE or HVD mode)					
Output leakage				400	nA
Output capacitance	Single-ended measurement to ground, See Note 3			3	pF
DISCNCT and DIFFB Input Section					
DISCNCT threshold		0.8		2.0	V
DISCNCT input current	$V_{DISCNCT} = 0$ V and 2.0 V	-30	-10		µA
DIFFB SE to LVD threshold		0.5		0.7	V
DIFFB LVD to HVD threshold		1.9		2.4	V
DIFFB input current	$0\ V \le V_{DIFFB} \le 2.75$ V	-10		10	µA
Low Voltage Differential (LVD) Status Bit Section (See Note 4)					
I_{SOURCE}	$V_{LOAD} = 2.4$ V		-6	-4	mA
I_{SINK}	$V_{LOAD} = 0.4$ V	2	5		mA
Time Delay/Filter Section					
Mode change delay	A new mode change can start any time after a previous mode change has been detected	100	190	300	ms
Thermal Shutdown Section					
Themal shutdown threshold	For increasing temperature	140	155	170	°C
Themal shutdown hysteresis			10		°C

NOTES: 1. V_{CM} is applied to all L+ and L- lines simultaneously.

2. $$Z_{CM} = \frac{(2.0V - 0.5V)}{\left[I_{VCM(max)} - I_{VCM(min)}\right]} \text{ @ } V_{CM(max)} = 2.0,\ V_{CM(min)} = 0.5\ V$$

3. Ensured by design, not production tested.
4. This applies to the 28-pin package only.

pin descriptions

DIFFB: DIFFSENS input pin. Connect through a 20-kΩ resistor to DIFSENS and through a 0.1-µF capacitor to ground. Input to comparators that detect what types of drivers are connected to the SCSI bus.

DIFSENS: SCSI bus DIFSENS line driver.

DISCNCT: Disconnect pin. Shuts down the terminator (switches terminating resistors off the bus) when open or active (high). The disconnect pin low enables the terminator.

GND: Power supply return.

LINE*n*-: Line termination pins. Negative line in differential pair.

LINE*n*+: Line termination pins. Positive line in differential pair.

LVD: (28-pin package only) Indicates that the bus is in LVD mode.

REG: Regulator bypass pin. Bypass near the terminator with a 4.7-µF and a high-frequency, low-ESR 0.01-µF capacitor to ground.

TRMPWR: V_{IN} 2.75 V to 5.25 V supply. Bypass near the terminator with a 4.7-µF and a high-frequency, low-ESR 0.01-µF capacitor to ground.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI driver devices are present on the bus. The UCC5680 is a low-voltage differential (LVD)-only device. It senses which types of drivers are present on the bus. If it detects the presence of a single-ended (SE) or high-voltage differential (HVD) driver, the UCC5680 will place itself in a high-impedance input state, effectively disconnecting the chip from the bus.

The UCC5680 senses what kinds of drivers are present on the bus by the voltage on SCSI bus control line DIFFSENS, which is monitored by the DIFFB input pin. The DIFSENS output pin on the UCC5680 attempts to drive a DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFFSENS line will be successfully driven to that voltage. If HVD drivers are present, they will pull the DIFFSENS line high. If any single-ended drivers are present, they pull the DIFSENS line to ground (even if HVD drivers are also present on the bus). If the voltage on the DIFFB is below 0.5 V or above 2.4 V, the UCC5680 enters the high-impedance SE/HVD state. If it is between 0.7 V and 1.9 V, the UCC5680 enters the LVD mode. These thresholds accommodate differences in ground potential that can occur between the ends of long bus lines.

Three UCC5680 ICs are required at each end of the SCSI bus to terminate 27 lines (18 data, 9 control). Every UCC5680 contains a DIFSENS driver, but only one should be used to drive the line at each end. The DIFSENS pin on the other devices should be left unconnected.

On power up (the voltage on the TRMPWR pin rising above 2.7 V), the UCC5680 assumes the SE/HVD mode. If the voltage on the DIFFB input indicates LVD mode, the chip waits 100 ms to 300 ms before changing the mode of the bus. If the voltage at the DIFFB input later crosses one of the thresholds, the UCC5680 again waits 100 ms to 300 ms before changing the mode of the bus. The magnitude of the delay is the same when changing in or out of either bus mode. A new mode change can start anytime after a previous mode change has been detected.

The DIFFB inputs on all three chips at each end of the bus should be connected together. Properly filtered, noise on DIFFB will not cause a false mode change. There should be a shared 50-Hz noise filter implemented on DIFFB at each end of the bus as close as possible to the DIFFB pins. This is implemented with a 20-kΩ resistor between the DIFFB and DIFSENS pins, and a 0.1-µF capacitor from DIFFB to ground. See the *Typical Application* diagram at the end of this datasheet.

APPLICATION INFORMATION (continued)

In LVD mode, the regulated voltage is switched to 1.25 V and a resistor network is presented to each line pair that provides common-mode impedance of 150 Ω and differential impedance of 105 Ω. The lines in each differential pair are biased so that when not driven, Line(n)+ and Line(n)− are driven 56 mV below and above the common-mode bias voltage (1.25 V) respectively.

In SE/HVD mode, all the terminating resistors are switched off the bus. The 1.25-V and 1.3-V (DIFSENS) regulators are left on.

When the disconnect input (DISCNCT) is active (high), the terminating resistors are switched off the bus and both voltage regulators are turned off to save power. The mode change filter/delay function is still active and the LVD pin (in the 28-pin package) continues to indicate the correct bus mode.

The UCC5680 operates down to a TRMPWR voltage of 2.7 V. This accommodates a 3.3-V system with allowance for supply tolerance (±10%), a unidirectional fusing device, and cable drop. The UCC3916 is recommended in place of a fuse and diode implementation, as its lower voltage drop provides additional voltage margin for the system.

Layout is important in all SCSI implementations and critical in SPI-3 systems, which have stringent requirements on both the absolute value of capacitance on differential signal lines and the balancing of capacitance between paired lines and from pair to pair.

Feedthroughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multilayer power and ground plane spacing adds about 1 pF to each plane. Each feed-through will add 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes reduces capacitance. Opening up the power and ground planes under a through-hole connector reduces added capacitance in those applications. Capacitance is also affected by components in close proximity on both sides of the board.

maximum capacitance

SCSI Class	Trace to GND: REQ, ACK, DATA, Parity, P_CRCA	Trace to Trace: REQ, ACK, DATA, Parity, P_CRCA	Trace to GND: Other signals	Trace to Trace: Other Signals
Ultra1	25 pF	N/A	25 pF	N/A
Ultra2	20 pF	10 pF	25 pF	13 pF
Ultra3/Ultra160	15 pF	8 pF	25 pF	13 pF
Ultra320	13 pF	6.5 pF	21 pF (est.)	10 pF (est.)

TI terminators are designed with very tightly controlled capacitance on their signal lines. Between the positive and negative lines in a differential pair the difference is typically no more than 0.1 pF, and only 0.3 pF between pairs.

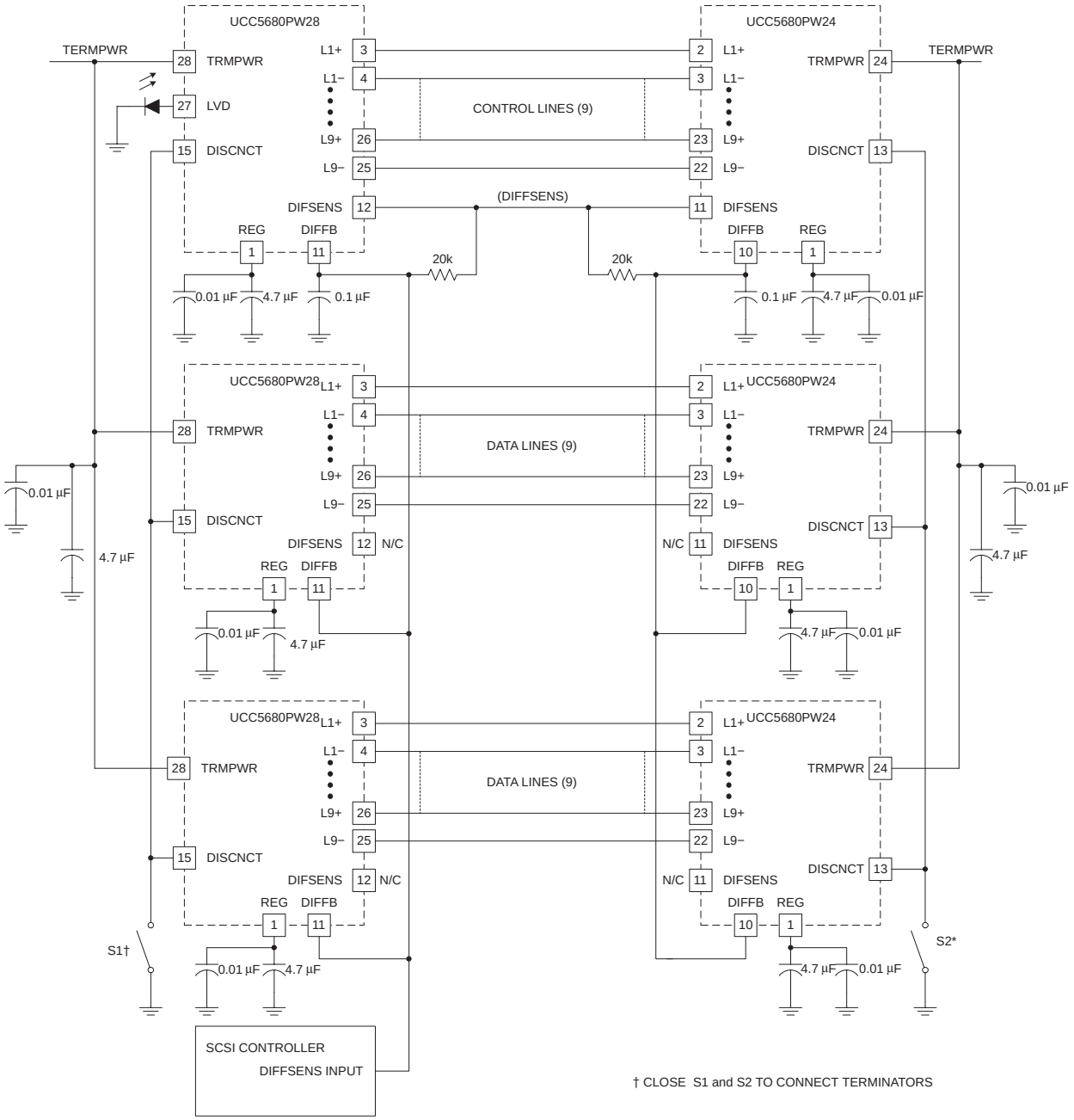
Multi-layer boards need to adhere to the 120-Ω impedance standard, including the connector and feedthroughs. Bus traces are normally run on the outer layers of the board with 4-mil etch and 4-mil spacing between the two lines in each differential pair, and a minimum of 8-mil spacing to adjacent pairs to minimize crosstalk. Microstrip technology is too low in impedance and should not be used—it is designed for 50 Ω rather than 120-Ω differential systems.

Decoupling capacitors should be installed as close as possible to the following input pins of the UCC5680:

TRMPWR: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

REG: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

TYPICAL APPLICATION



UDG-00005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC5680PW24	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -24	Samples
UCC5680PW24G4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -24	Samples
UCC5680PW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -28	Samples
UCC5680PW28G4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -28	Samples
UCC5680PW28TR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -28	Samples
UCC5680PW28TRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5680PW -28	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

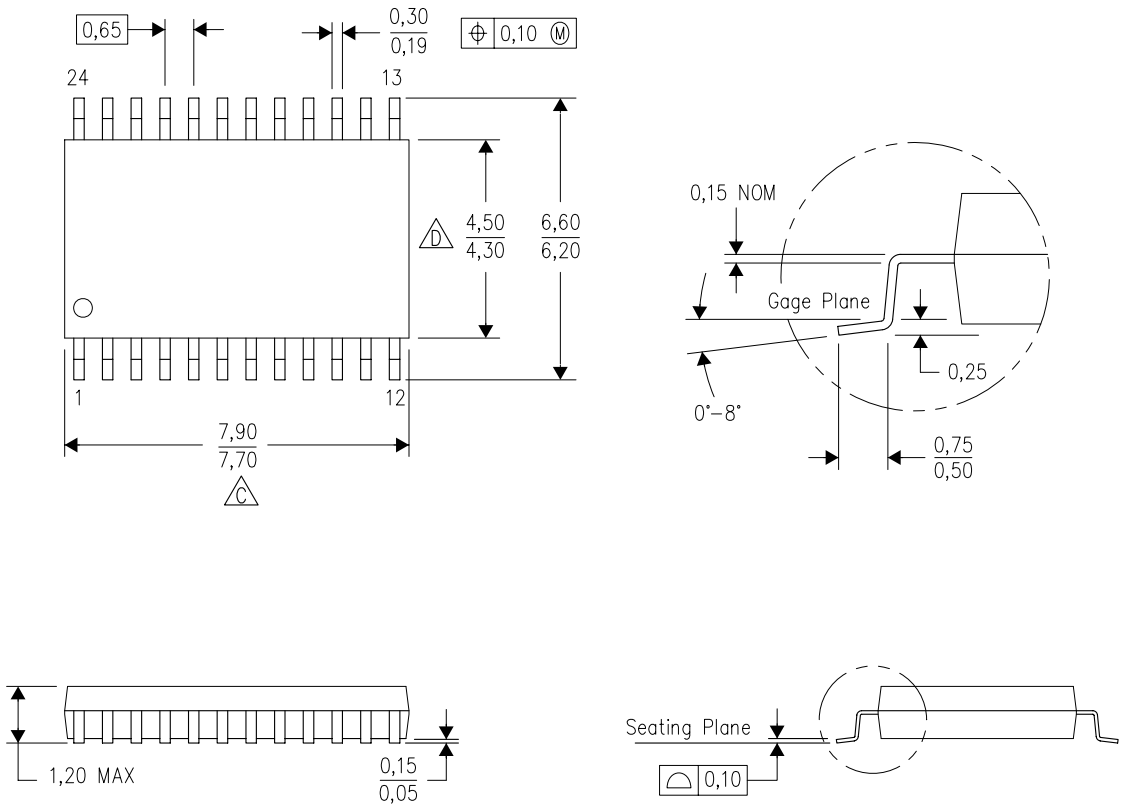
(4) Only one of markings shown within the brackets will appear on the physical device.

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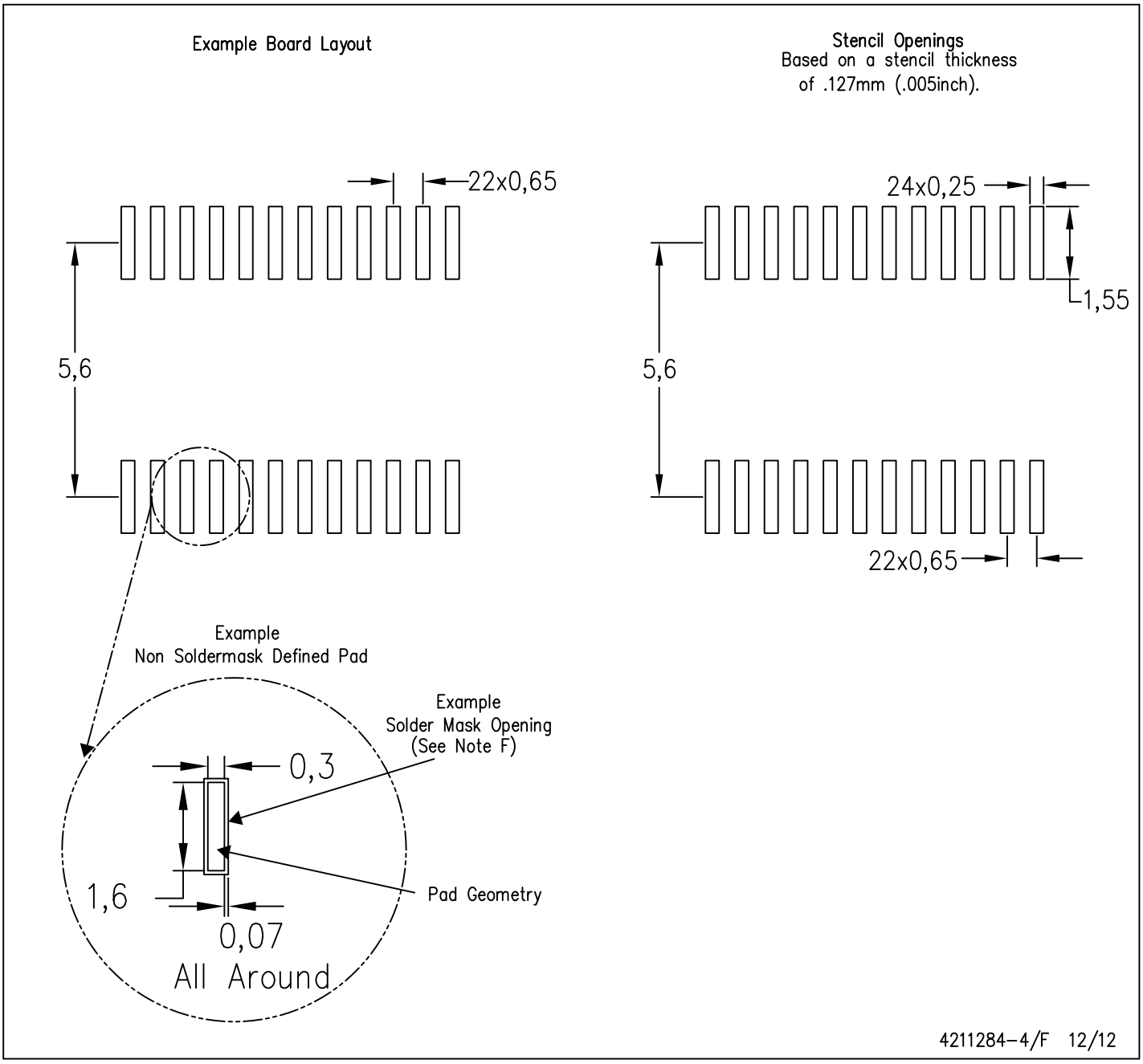
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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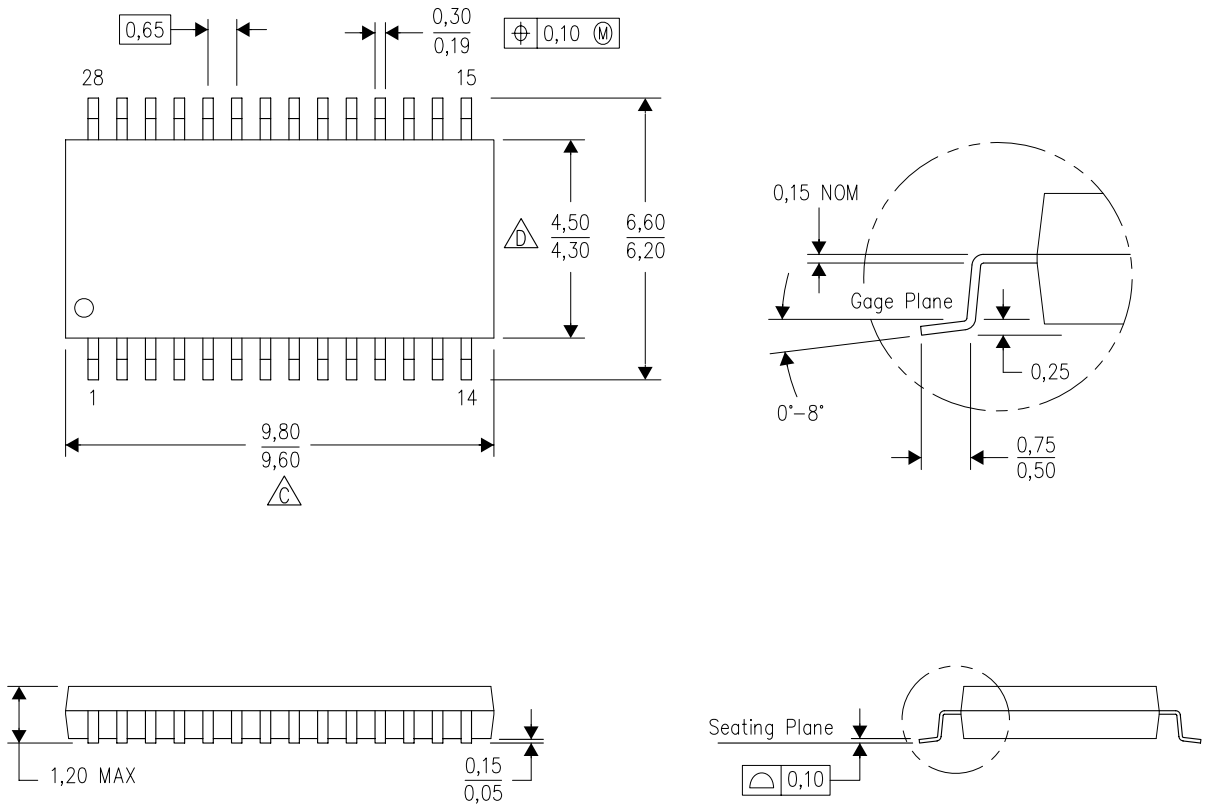
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

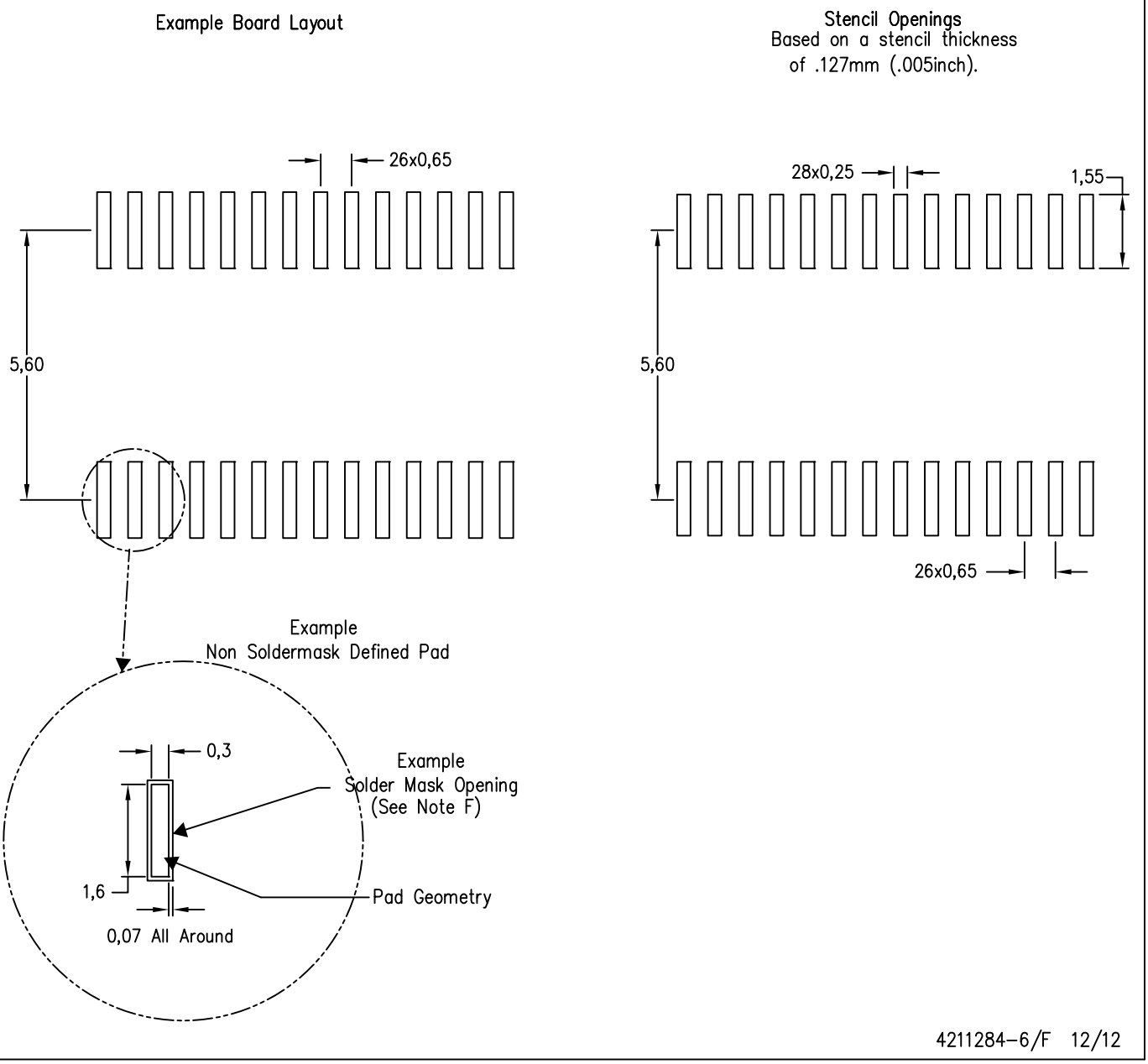
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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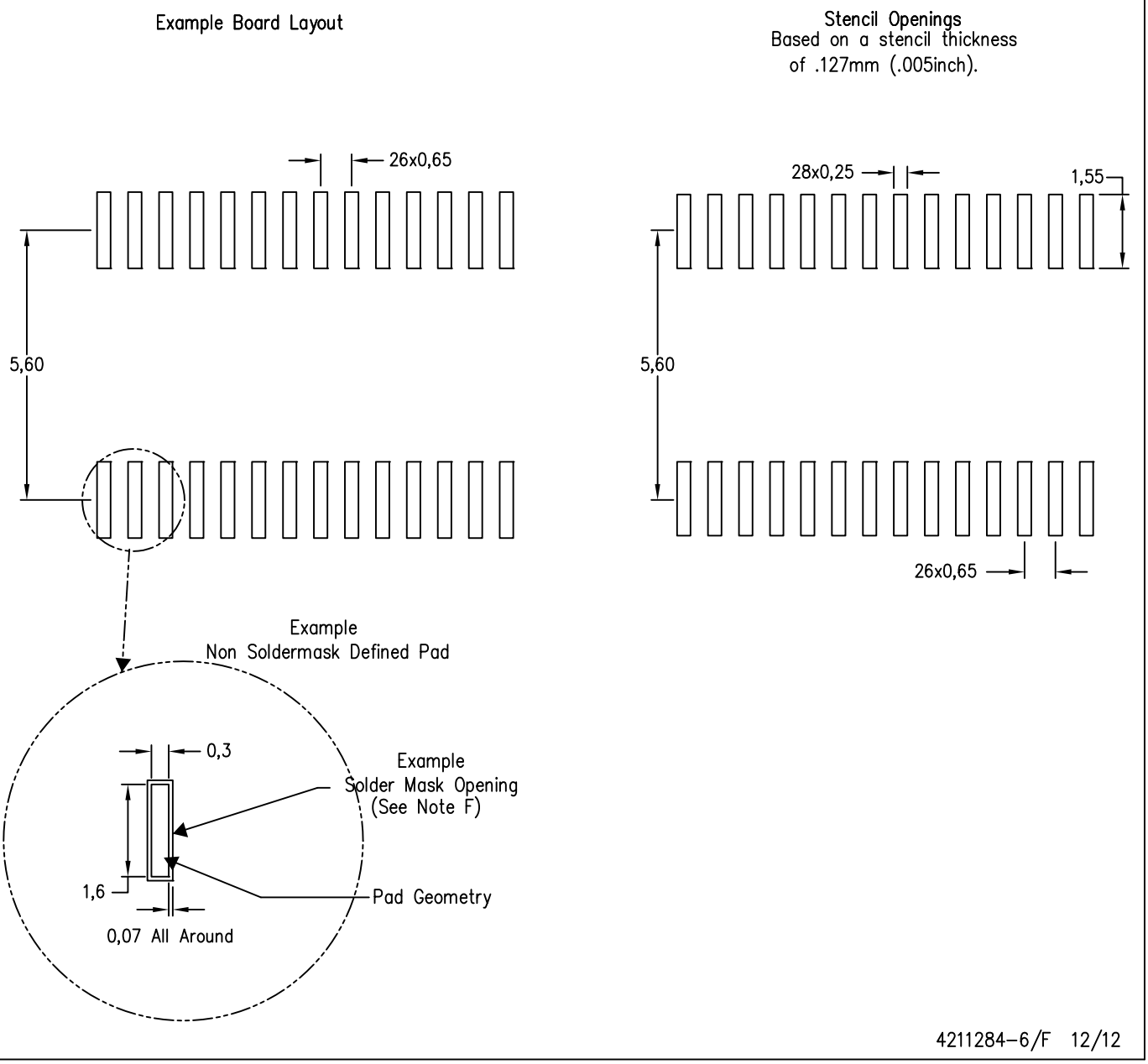
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D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Наличие собственной эффективной системы логистики обеспечивает надежную поставку продукции по конкурентным ценам в точно указанные сроки.

Срок поставки со стоков в **Европе и Америке – от 3 до 14 дней.**

Срок поставки из **Азии – от 10 дней.**

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

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Перечень производителей, продукцию которых мы поставляем на российский рынок



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С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

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