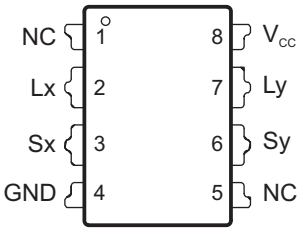
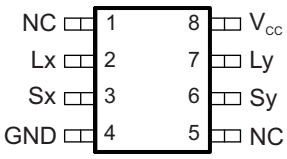
FEATURES

- **Operating Power-Supply Voltage Range of 3 V to 12 V**
- **Supports Bidirectional Data Transfer of I²C Bus Signals**
- **Allows Bus Capacitance of 400 pF on Main I²C Bus (Sx/Sy Side) and 3000 pF on Transmission Side (Lx/Ly Side)**
- **Dual Bidirectional Unity-Voltage-Gain Buffer With No External Directional Control Required**
- **Drives 10× Lower-Impedance Bus Wiring for Improved Noise Immunity**
- **Multi-Drop Distribution of I²C Signals Using Low-Cost Twisted-Pair Cables**
- **I²C Bus Operation Over 50 Meters of Twisted-Pair Wire**
- **Latch-up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2500-V Human-Body Model (A114-A)**
  - **400-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

P PACKAGE
(TOP VIEW)



D PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The P82B715 is a bipolar device intended for I²C bus systems applications and supports bidirectional data transfer via the I²C bus. The P82B715 buffers both the serial data (SDA) and serial clock (SCL) signals on the I²C bus and allows for extension of the I²C bus, while retaining all the operating modes and features of the I²C system.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Tube of 50	P82B715P	P82B715P
	SOIC – D	Tube of 75	P82B715D	PG715
		Reel of 2500	P82B715DR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

In general, the I^2C bus capacitance limit of 400 pF restricts practical communication distances to a few meters. One of the advantages of the P82B715 is that it can isolate bus capacitance such that the total loading (devices, connectors, traces and wires) of the new bus or remote I^2C nodes are not apparent to other I^2C buses (or nodes). This is achieved by using one P82B715 device at each end of a long cable. The pin Lx of one P82B715 device has to be connected to Lx of the second P82B715 (similarly for Ly). This allows the total system capacitance load to be around 3000 pF. The P82B715 uses unidirectional analog current amplification to increase the current sink capability of I^2C chips by a factor of ten and to change the 400-pF I^2C bus specification limit into a 4-nF bus wiring capacitance limit. That means longer cables or lower-cost general-purpose wiring may be used to connect two separate I^2C-based systems, without worrying about the special voltage levels associated with other I^2C bus buffers.

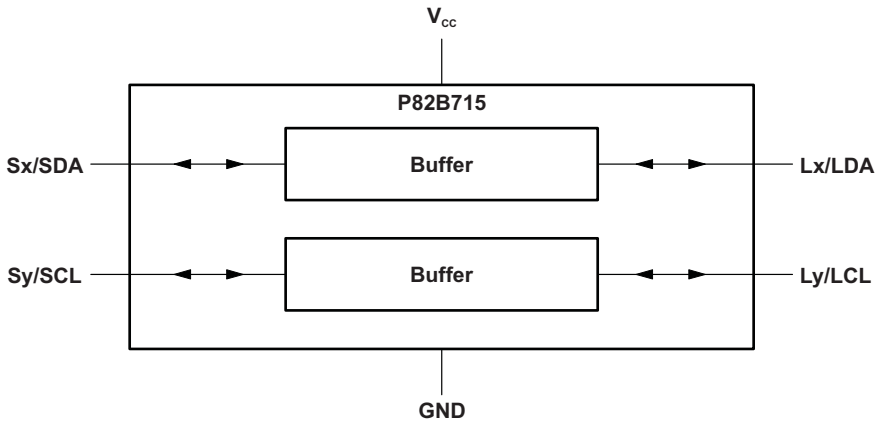
Multiple P82B715s can be connected together in a star or multipoint architecture by their Lx/Ly ports, without limit, as long as the total capacitance of the system remains less than about 3000 pF (400 pF or less when referenced to any Sx/Sy connection). In that arrangement, the master and/or slave devices are attached to the Sx/Sy port of each P82B715. The P82B715 alone does not support voltage-level translation, but it simplifies the application of low-cost transistors for this purpose. In normal use, the power-supply voltages at each end of the low-impedance buffered bus line should be the same. If these differ by a significant amount, noise margin is sacrificed.

Two or more Sx or Sy I/Os can be interconnected and are also fully compatible with bus buffers that use voltage-level offsets (such as the PCA9515A) because it duplicates and transmits the offset voltage.

TERMINAL FUNCTIONS

D OR P PACKAGE NO.	NAME	DESCRIPTION
1	NC	No connection
2	Lx	Buffered serial data bus or LDA
3	Sx	Serial data bus or SDA. Connect to V_{CC} of I^2C master through a pullup resistor.
4	GND	Ground
5	NC	No connection
6	Sy	Serial clock bus or SCL. Connect to V_{CC} of I^2C master through a pullup resistor.
7	Ly	Buffered serial clock bus or LCL
8	V_{CC}	Supply voltage

FUNCTIONAL BLOCK DIAGRAM



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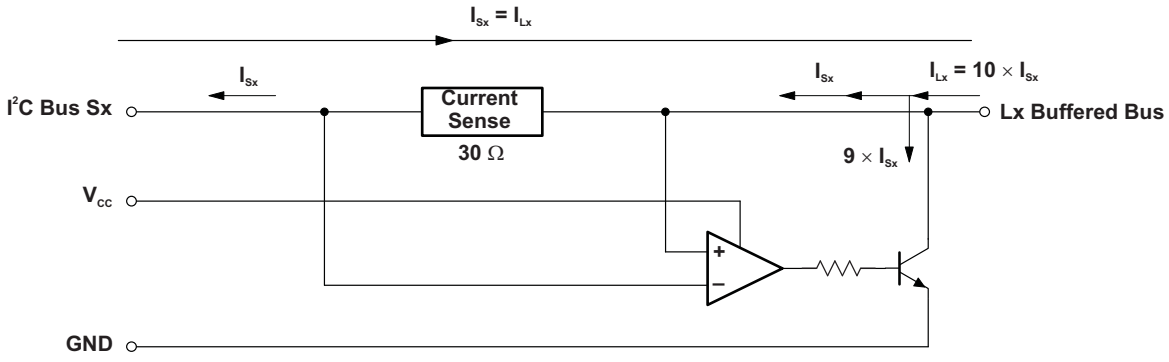


Figure 1. Equivalent Circuit (One-Half of P82B715)

Functional Description

Sx and Sy

The I^2C pins (Sx and Sy) are designed to interface with a normal I^2C bus. The maximum I^2C bus supply voltage is 12 V. The Sx and Sy pins contain identical circuitry and can be used interchangeably as SCL or SDA.

Lx and Ly

On the special low-impedance or buffered-line side, the corresponding output becomes the LDA data line or LCL clock line. The P82B715 provides current amplification from its I^2C bus to its low impedance or buffered bus. Whenever current is flowing out of Sx into an I^2C chip driving the I^2C bus low, its amplifier sinks ten times that current into Lx, to drive the buffered bus low (see Figure 1). To minimize interference and ensure stability, the current rise and fall times of the Lx drive amplifier are internally controlled. The P82B715 does not amplify signal currents flowing into Sx on the I^2C bus driven by currents flowing out of Lx on the buffered side. A buffered bus logic low signal at Lx passes via the internal 30-Ω resistor to drive the I^2C bus low. This signal current amplification, dependent on its direction, preserves the multimaster bidirectional open-collector/open-drain characteristic of any connected I^2C bus lines and the new low-impedance bus. Bus logic-signal voltage levels are clamped at (V_{CC} + 0.7 V) but, otherwise, are independent of the supply voltage, V_{CC}.

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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	12	V
V_b	I^2C bus voltage range	Sx or Sy	0	V_{CC}	V
	Buffered bus voltage range	Lx or Ly	0	V_{CC}	
I_O	Continuous output current	Sx or Sy		60	mA
		Lx or Ly		60	
I_{CC}	Continuous current through V_{CC} or GND			60	mA
θ_{JA}	Package thermal impedance(2)	D package		97	°C/W
		P package		85	
T_{stg}	Storage temperature range		–55	125	°C
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage(1)	4.5	12	V
T_A	Operating free-air temperature	–40	85	°C

(1) Operation with reduced performance is possible down to 3 V. Typical static sinking performance is not degraded at 3 V, but the dynamic sink currents while the output is being driven through $V_{CC}/2$ are reduced and can increase fall times. Timing-critical designs should accommodate the specified minimums.

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Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C, voltages are specified with respect to GND (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Quiescent supply current	Sx = Sy = V_{CC}			14		mA
		V_{CC} = 12 V			15		
		Both I^2C inputs low, Both buffered outputs sinking 30 mA			22		
I_{IOS}	Output sink current on I^2C bus	Sx, Sy	V_{CC} > 3 V, V_{Sx}, V_{Sy} (low) = 0.4 V, V_{Lx}, V_{Ly} (low) on buffered bus = 0.3 V, I_{Lx}, I_{Ly} = –3 mA(1)	2.6			mA
I_{IOL}	Output sink current on buffered bus	Lx, Ly	V_{Lx}, V_{Ly} (low) = 0.4 V, V_{Sx}, V_{Sy} (low) on I^2C bus = 0.3 V	30			mA
			3 V < V_{CC} < 4.5 V, V_{Lx}, V_{Ly} (low) = 0.4 V to 1.5 V, I_{Sx}, I_{Sy} sinking on I^2C bus < –4 mA	24			
			3 V < V_{CC} < 4.5 V, V_{Lx}, V_{Ly} (low) = 1.5 V to V_{CC}, I_{Sx}, I_{Sy} sinking on I^2C bus = –7 mA	24			
I_I	Input current from I^2C bus	Sx, Sy	I_{Lx}, I_{Ly} sink on buffered bus = 30 mA			–3.2	mA
	Input current from buffered bus(1)	Lx, Ly	V_{CC} > 3 V, I_{Sx}, I_{Sy} sink on I^2C bus = 3 mA(1)			–3	
	Leakage current on buffered bus		V_{CC} = 3 V to 12 V, V_{Lx}, V_{Ly} = V_{CC}, V_{Sx}, V_{Sy} = V_{CC}			200	µA
Z_{in}/Z_{out}	Input/output impedance	V_{Sx} < V_{Lx}, Buffer is active		8	10	13	

(1) Buffer is passive in this test. The Sx/Sy sink current flows via an internal resistor to the driver connected at the Lx/Ly I/O.

Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, no capacitive loads, voltages are specified with respect to GND (unless otherwise specified)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYP	UNIT
Buffer Delay Times						
$t_{rise/fall}$	Delay time to V_{Lx} voltage crossing V_{CC}/2 for input drive current step I_{Sx} at Sx(1) (see Figure 2)	I_{Sx} I_{Sy}	V_{Lx} V_{Ly}	R_{Lx} pullup = 270 Ω	250	ns
	Buffer delay time, switching edges between V_{Lx} input and V_{Sx} output(2)	V_{Lx} V_{Ly}	V_{Sx} V_{Sy}	R_{Lx} pullup = 4700 Ω	0	ns

(1) A conventional input-output delay is not observed in the Sx/Lx voltage waveforms, because the input and output pins are internally tied with a 30-Ω resistor so they show equal logic voltage levels to within 100 mV. When connected in an I^2C system, an Sx/Sy input pin cannot rise/fall until the buffered bus load at the output pin has been driven by the internal amplifier. This test measures the bus propagation delay caused to falling or rising voltages at the Lx/Ly output (as well as the Sx/Sy input) by the amplifier's response time. The figure given is measured with a drive current as shown in Figure 2. Because this is a dynamic bus test in which a corresponding bus driving IC has an output voltage well above 0.4 V, 6 mA is used instead of the static 3 mA.

(2) The signal path Lx to Sx and Ly to Sy is passive via the internal 30-Ω resistor. There is no amplifier involved and essentially no signal propagation delay.

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PARAMETER MEASUREMENT INFORMATION

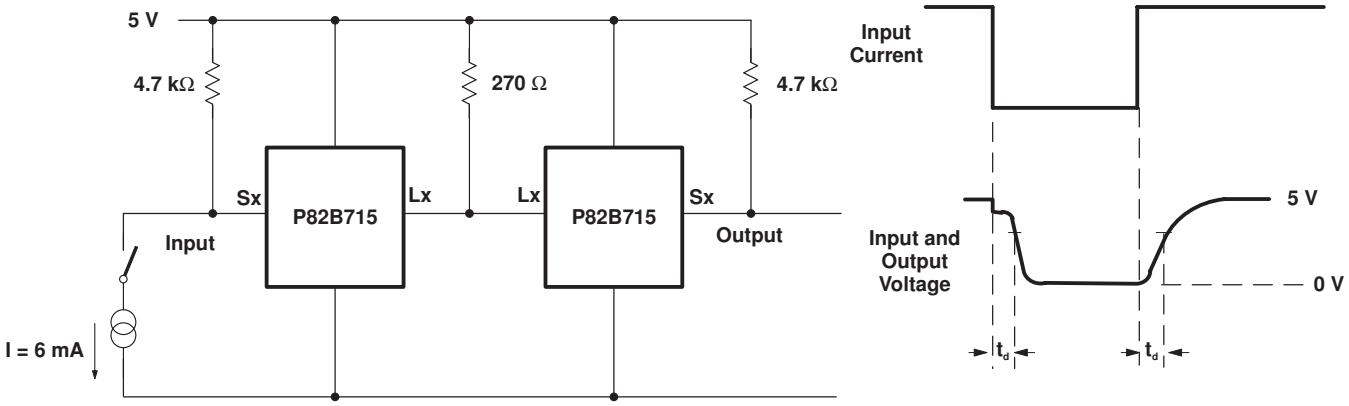


Figure 2. Test Circuit for Delay Times

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APPLICATION INFORMATION

By using two (or more) P82B715 devices, a subsystem can be built that retains the interface characteristics of a normal I²C device so that the subsystem may be included in, or added to, any I²C or related system.

The subsystem features a low-impedance or buffered bus capable of driving large wiring capacitance (see Figure 3).

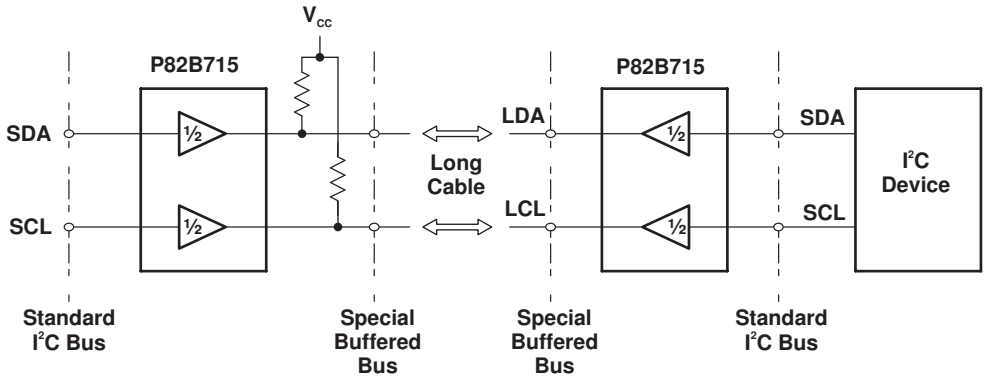


Figure 3. Minimum Subsystem Diagram

The P82B715 can operate with a supply voltage from 3 V to 12.5 V, but the logic-signal levels at Sx/Lx are independent of the supply voltage. They remain at the levels presented to the chip by the attached devices. The maximum static I²C bus sink current, 3 mA, flowing in either direction in the internal current sense resistor, causes a difference less than 100 mV in the bus logic low levels at Sx and Lx. This makes P82B715 fully compatible with all logic signal drivers, including TTL. The P82B715 cannot modify the bus logic signal voltage levels, but it contains internal diodes connected between Lx/Sx and V_{CC} that conduct and limit the logic signal swing if the applied logic levels would have exceeded the supply voltage by more than 0.7 V.

In normal applications, external pullup resistors pull the connected buses up to the desired voltage high level. Usually this is the supply voltage, V_{CC}, but for very low logic voltages, it is necessary to use a V_{CC} of at least 3.3 V and preferably higher. Note that full performance over temperature is ensured only from 4.5 V. Specification deratings apply when its supply voltage is reduced below 4.5 V. The absolute minimum V_{CC} is 3 V.

I²C Systems

As in standard I²C systems, pullup resistors are required to provide the logic high levels on the buffered bus, as the standard open-collector configuration is retained. The size and number of pullup resistors depends on the system.

If P82B715 devices are to be permanently connected into a system, the circuit may be configured with only one pullup resistor on the buffered bus and none on the I²C buses, but the system design is simplified, and performance is improved by fitting separate pullups on each section of the bus. When a subsystem using P82B715 may be optionally connected to an existing I²C system that already has a pullup, the effects of the subsystem pullups acting in parallel with the existing I²C bus pullup must be considered.

Pullup Resistance Calculation

When calculating the pullup resistance values, the gain of the buffer introduces scaling factors that must be applied to the system components. In practical systems, the pullup resistance value is calculated to meet the rise time limit for I²C systems. As an approximation, this limit is satisfied in a 100-kHz system if the time constant of the total system (product of the net resistance and net capacitance) is set to 1 µs or less.

In systems using the P82B715, it is convenient to set the total system time constant by considering each bus node separately (i.e., the I²C nodes and the buffered bus node) and selecting a separate pullup resistor for each node to provide time constants of less than 1 µs. If each node complies then the system requirement is also met.

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This arrangement, using multiple pullups as shown in Figure 4, provides the best system performance and allows stand-alone operation of individual I²C buses if parts of the extended system are disconnected or reconnected. For each bus section, the pullup resistor is calculated as:

$$R = 1\ \mu s/(C_{device} + C_{wiring})$$

Where:

C_{device} = Sum of any connected device capacitances

C_{wiring} = Total wiring and stray capacitance on the bus section

The 1 µs is an approximation with a safety factor to the theoretical time constant necessary to meet the specified 1-µs bus rise-time specification in a system with variable logic thresholds, where the CMOS limits of 30% and 70% of V_{CC} apply. The calculated value is 1.18 µs.

If these capacitances cannot be measured or calculated, an approximation can be made by assuming that each device presents 10 pF of load capacitance and 10 pF of trace capacitance, and that cables range from 50 pF to 100 pF per meter.

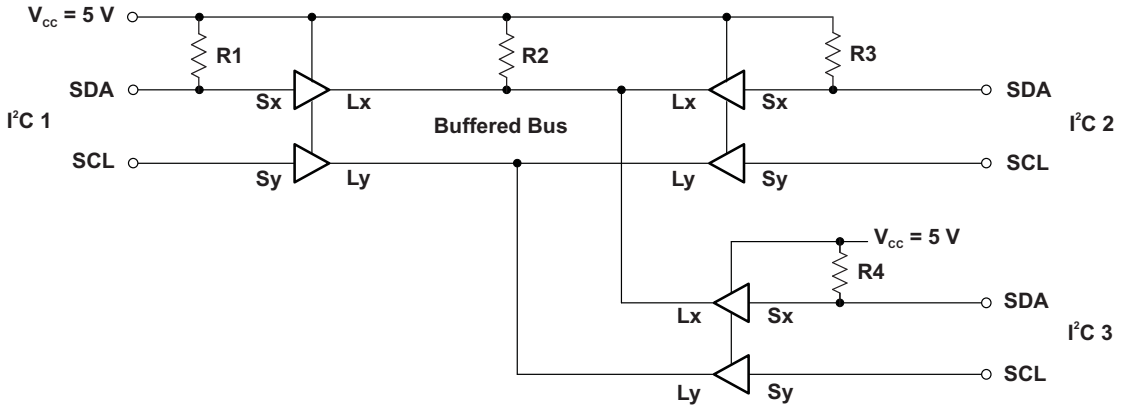


Figure 4. Single Pullup Buffered Bus

If only a single pullup is used, it must be placed on the buffered bus (as R2 in Figure 4,) and the associated total system capacitance calculated by combining the individual bus capacitances into an equivalent capacitive loading on the buffered bus.

This equivalent capacitance is the sum of the capacitance on the buffered bus plus ten times the sum of the capacitances on all the connected I²C nodes. The calculated value should not exceed 4 nF. The single buffered bus pullup resistor is then calculated to achieve the 1-µs rise time, and it provides the pullup for the buffered bus and for all other connected I²C bus nodes included in the calculation.

Calculating Bus Drive Currents

Figure 4 shows three P82B715 devices connected to a common buffered bus. The associated bus capacitances are omitted for clarity, but assume the resistors have been selected to give R-C products of less than 1 µs so the bus rise-time requirement is satisfied. An I²C device connected at I²C 1 and holding the SDA bus low must sink the current flowing in its local pullup R1, plus, with assistance from the P82B715, the currents in R2, R3, and R4. Because the resistors R3 and R4 act to pull the bus nodes I²C 2 and I²C 3 and their corresponding Sx pins to a voltage higher than the voltage at the Lx pins, their buffer amplifiers are inactive. The SDA at Sx of I²C 2 and I²C 3 is pulled low by the low at Lx via the internal 30-Ω resistor that links Lx to Sx. So the effective current that must be sunk by the P82B715 buffer on I²C 1 at its Lx pin is the sum of the currents in R2, R3, and R4. The Sx current that must be sunk by an I²C device at I²C 1 due to the buffer gain action is 1/10 of the Lx current. So the effective pullup determining the current to be sunk by an I²C device at I²C 1 is R1 in parallel with resistors ten times the values of R2, R3, and R4. If R1 = R3 = R4 = 10 kΩ, and R2 = 1 kΩ, the effective pullup load at I²C 1 is 10 kΩ||10 kΩ||100 kΩ||100 kΩ = 4.55 kΩ.

The same calculation applies for I²C 2 or I²C 3.

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To calculate the current sunk by the Lx pin of the buffer at I²C 1, note that the current in R1 is sunk directly by the device at I²C 1. The buffer, therefore, sinks only the currents flowing in R2, R3, and R4, so the effective pullup is R2 in parallel with R3 and R4.

In this example that is 1 kΩ||10 kΩ||10 kΩ = 833 Ω. For a 5.5-V supply and 0.4-V low, the buffer is sinking 16.3 mA.

The P82B715 has a static sink rating of 30 mA at Lx. The requirement is that the pullup on the buffered bus, in parallel with all other pullups that it is indirectly pulling low on Sx pins of other P82B715 devices, does not cause this 30-mA limit to be exceeded.

The minimum pullup resistance in a 5-V ± 10% system is 170 Ω.

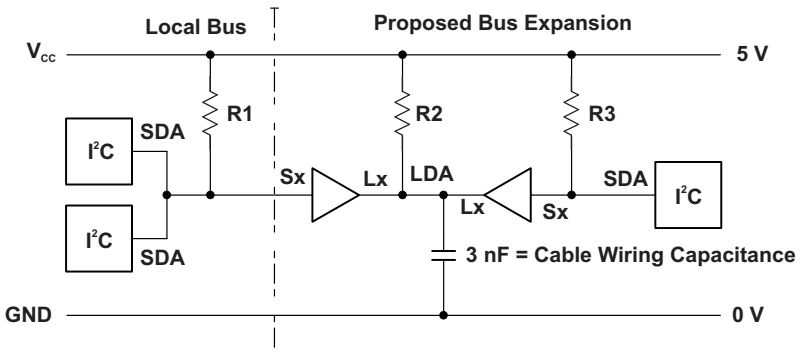
The general requirement is:

$(V_{CC}(max) – 0.4)/R_P < 30$ mA

Where:

R_p = Parallel combination of all pullup resistors driven by the Lx pin of the P82B715

Figure 5 shows calculations for an expanded I²C bus with 3 nF of cable capacitance.



Effective Capacitance Local Bus I²C Devices

2 × I²C Devices	20 pF
Strays	20 pF
P82B715	10 pF
Total	50 pF

Local I²C Pullup

$R1 = \frac{1\ \mu s}{50\ pF} = 20\ k\Omega$

Effective Capacitance Buffered Line

Wiring Capacitance	3000 pF
Total	3000 pF

Buffered Bus Pullup

$R2 = \frac{1\ \mu s}{3000\ pF} = 330\ \Omega$

Effective Capacitance Remote I²C Devices

1 × I²C Devices	10 pF
Strays	10 pF
P82B715	10 pF
Total	30 pF

Remote I²C Pullup

$R3 = \frac{1\ \mu s}{30\ pF} = 33\ k\Omega$

Figure 5. Typical Loading Calculations

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
P82B715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
P82B715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
P82B715DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
P82B715DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
P82B715P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
P82B715PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

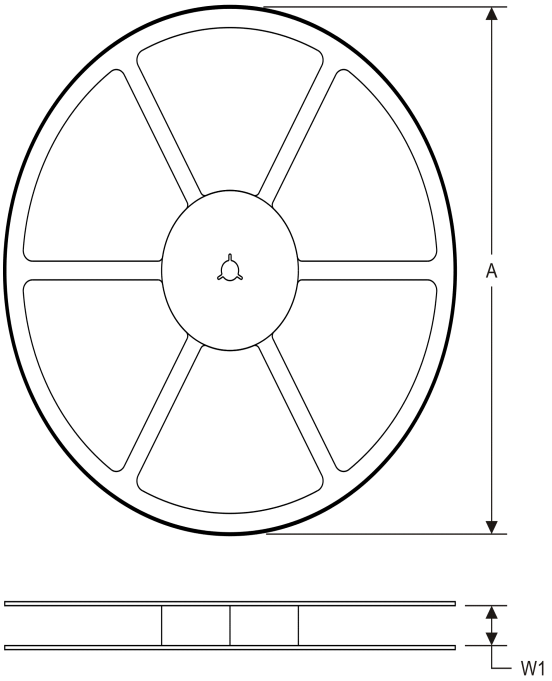
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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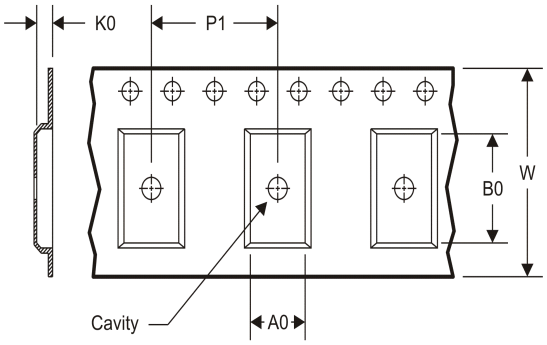
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



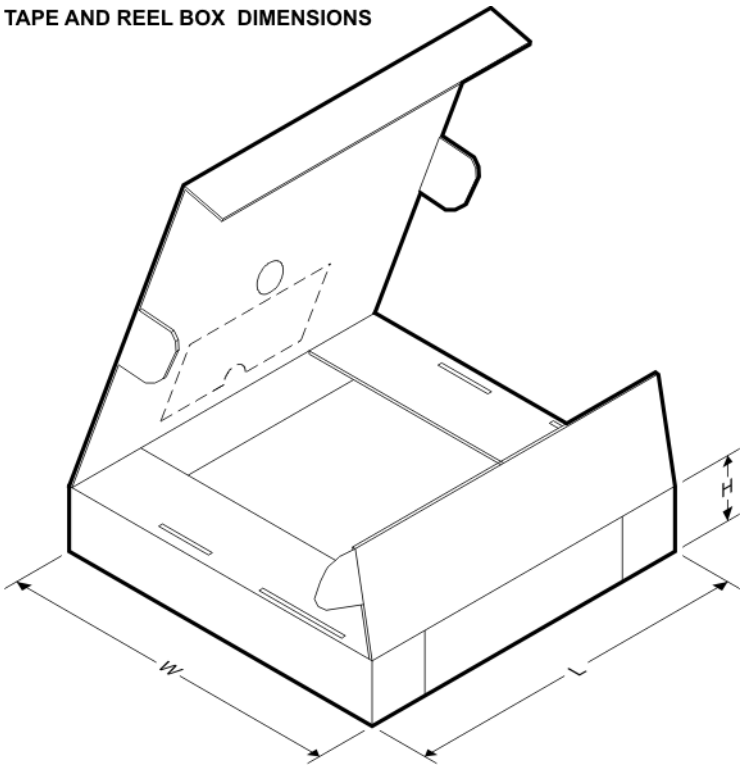
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P82B715DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

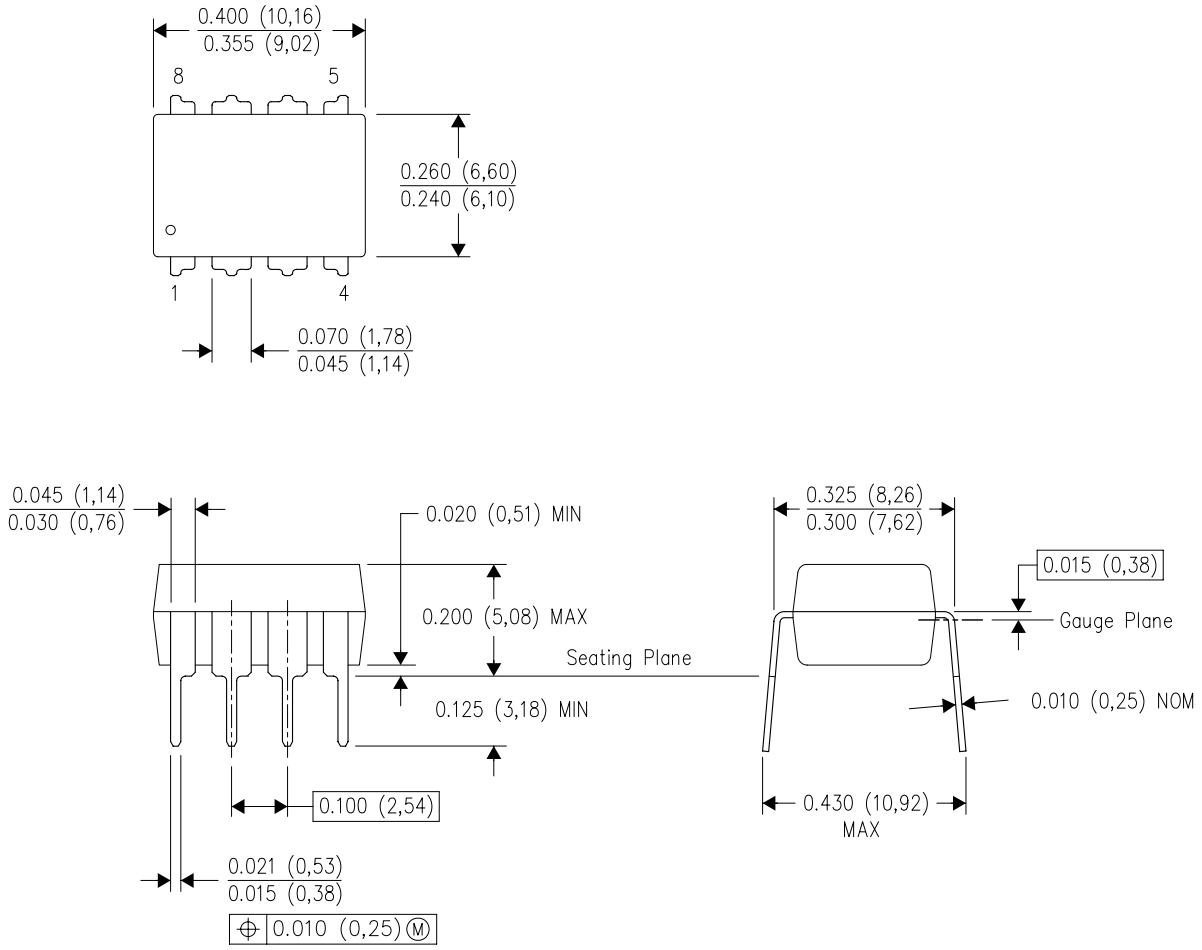
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

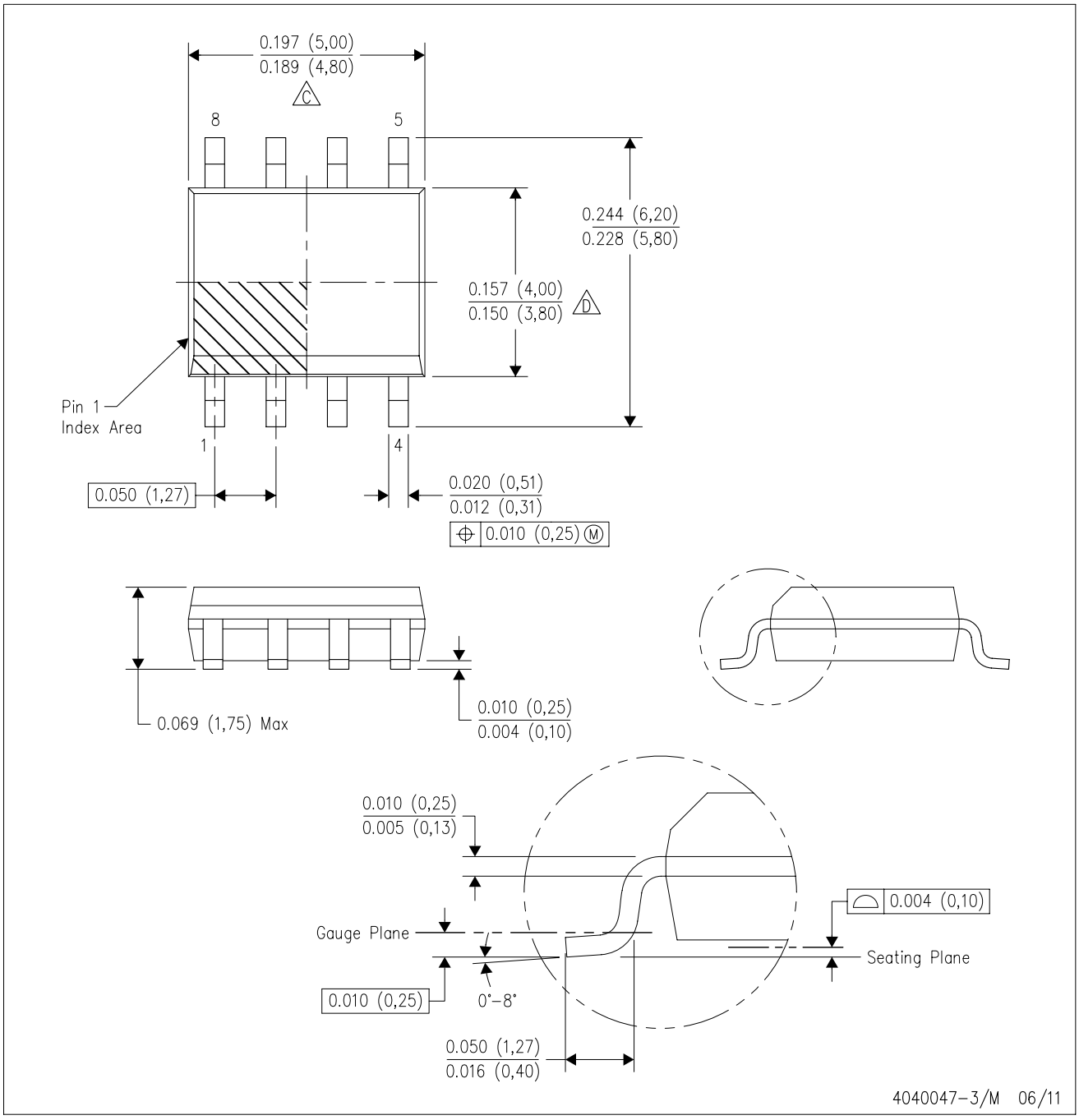
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P82B715DR	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



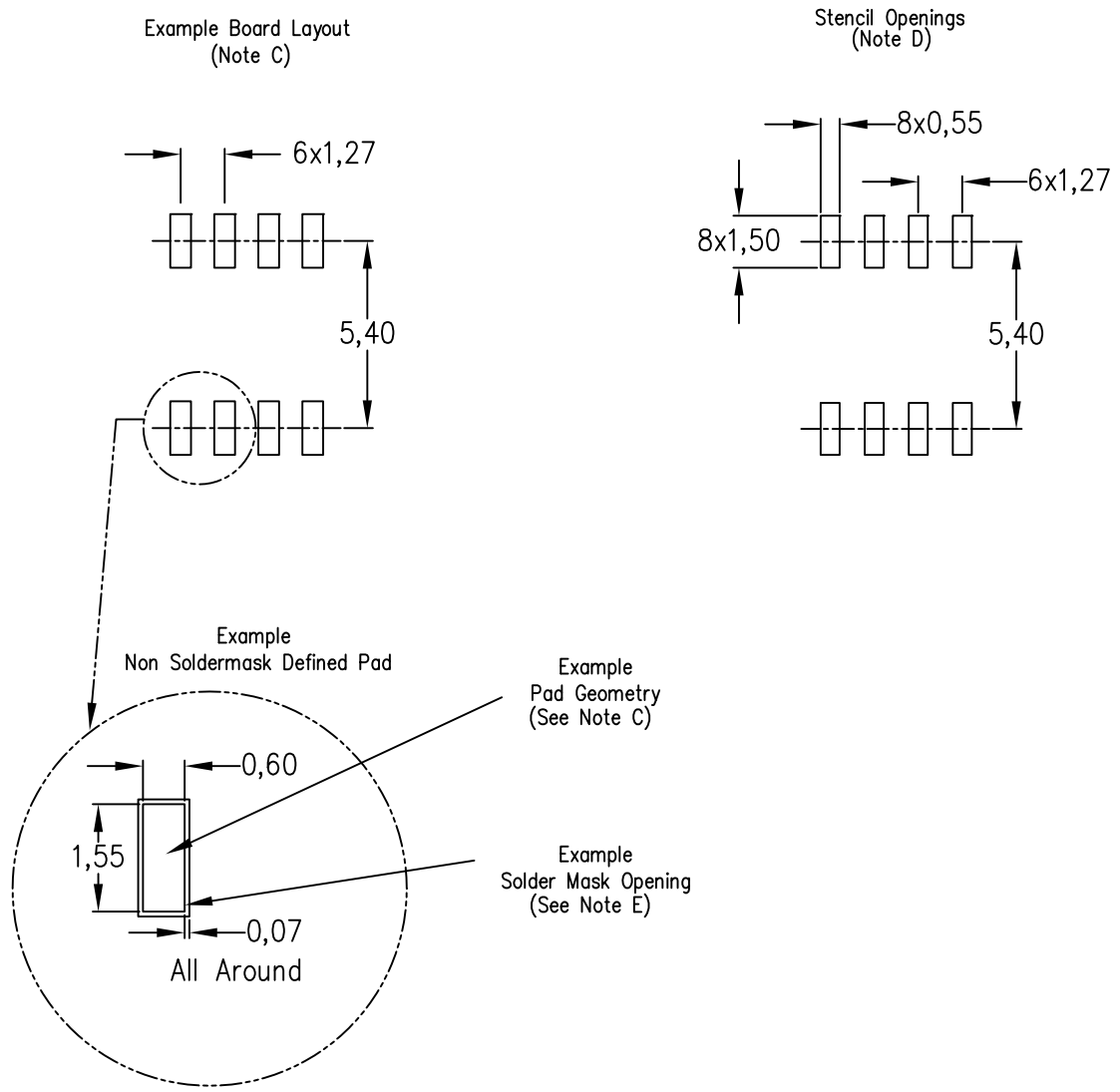
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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