Rev 0; 9/06

I²C Programmable-Gain Amplifier for Audio Applications

DS4420

General Description

The DS4420 is a fully differential, programmable-gain amplifier for audio applications. It features a -35dB to +25dB gain range controlled by an I²C interface and it is optimized to drive loads as low as 50Ω. The gain is adjustable in 3dB increments across the entire range. Three address inputs, used to select the I²C slave address, enable up to eight devices on a common bus.

The product operates from a single 5V supply over a -20°C to +70°C temperature range. It is offered in a 3mm x 3mm TDFN package.

Applications

Telephone Headsets

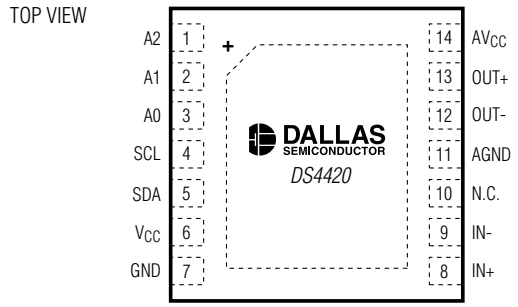
Audio Volume Control

Microphone Gain Control

Features

- **Differential Inputs and Outputs**
- **-35dB to +25dB Adjustable Gain**
- **Low Output Noise**
- **Low-Distortion Driving into a 50Ω Load**
- **3dB Gain Steps Programmed through I²C Interface**
- **5V Single Supply**
- **20kHz Bandwidth for All Gain Settings**
- **Small 3mm x 3mm x 0.8mm TDFN Package**
- **Up to Eight DS4420s can be Placed on the Same I²C Bus**

Pin Configuration



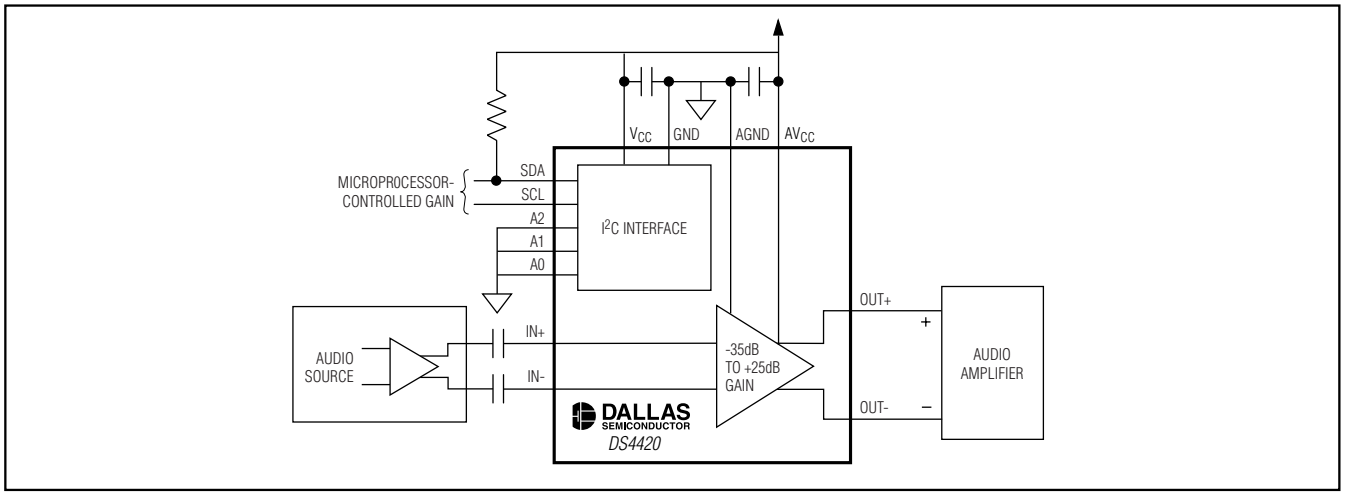
TDFN
(3mm x 3mm x 0.8mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4420+	-20°C to +70°C	14 TDFN-EP*

+Denotes lead-free package.
**EP = Exposed paddle.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC}, SDA, and SCL Relative to GND .....-0.5V to +6.0V
Voltage on A0, A1, and A2 Relative to GND .....-0.5V to (V_{CC} + 0.5V; not to exceed 6.0V)
Voltage on IN+, IN-, OUT-, and OUT+ Relative to AGND .....-0.5V to (AV_{CC} + 0.5V; not to exceed 6.0V)
Voltage on AV_{CC} Relative to V_{CC} .....-0.3V to +0.3V
Voltage on AGND Relative to GND .....-0.3V to +0.3V
Output Current 150mA
Operating Temperature Range .....-20°C to +70°C
Storage Temperature .....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{CC}	(Note 1)	+4.5		+5.5	V
Analog Supply Voltage	AV_{CC}			V_{CC}		V
Analog Ground	AGND	(See Figure 5)		GND		V
Input Logic 1 (SCL, SDA, A0, A1, A2)	V_{IH}		2.0		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1, A2)	V_{IL}		-0.3		+0.8	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	V_{CC} = 5.5V, R_L = ∞, V_{IN} = 0V differential (Note 9)		1.7	3	mA
Standby Current	I_{STBY}	V_{CC} = 5.5V (Notes 2, 9)			140	µA
Input Leakage (SDA, SCL, A2, A1, A0)	I_{IL}	V_{CC} = 5.5V			1	µA
Output Leakage (SDA)	I_L				1	µA
Output-Current Low (SDA)	I_{OL}	V_{OL} = 0.4V	3			mA
		V_{OL} = 0.6V	6			
Input Voltage Range	V_{IN}	Differential		-19	+1	dBV
Max Peak-to-Peak Input Level	V_{INP-P}	Differential			3.2	V
Input Resistance	R_{IN}	Differential, active mode (Note 3)	29	49	60	kΩ
Input Common-Mode Voltage	$V_{IN:CM}$		0.45 x V_{CC}		0.55 x V_{CC}	V
Output Voltage	V_O	R_L = 50Ω differential			6	dBV
Output Peak-to-Peak Signal Swing	V_{OP-P}	Differential			5.6	V
Output Common-Mode Voltage	$V_{O:CM}$		0.45 x V_{CC}	0.5 x V_{CC}	0.55 x V_{CC}	V
Output Offset Voltage	$V_{O:OS}$	A_V = +25dB	-20		+20	mV
Amplifier Output Current (Sourcing)	I_{OS1}	V_{OUT} = GND	95			mA
		V_{OUT} = V_{CC} - 0.75V	64			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Output Current (Sinking)	I_{OS2}	$V_{OUT} = V_{CC}$	89			mA
		V_{OUT} = 0.75V	64			
Resistive Load Range	R_L	Differential	50		50k	Ω
Capacitive Load	C_L	Cap to GND (Note 4)			100	pF
Closed-Loop Bandwidth		All gain settings (Note 5)	20		20k	Hz
Passband Flatness		20Hz to 20kHz (Notes 2, 5)	-1		+1	dB
Output Noise (Note 5)	N_O	A = -35dB, 300Hz to 3.4kHz		-123		dBV
		A = +25dB, 300Hz to 3.4kHz		-88		
Total Harmonic Distortion (Note 5)	THD	R_L = 50Ω, V_O ≤ +6dBV, f = 1kHz, A = ±16dB		0.03	1.0	%
		R_L = 1kΩ, V_O ≤ +6dBV, f = 1kHz, A = ±16dB		0.01		
Gain Range	A		-35		+25	dB
Gain Step Size	A_S		2.0	3.0	4.0	dB
Gain Accuracy	A_{ERR1}	(Note 10)	-2.5		+2.5	dB
Mute and Standby Mode Gain	A_{MUTE}	(Note 5)			-90	dB
Standby Mode Exit Time	t_{PU}	(Note 6)			10	µs

I²C AC ELECTRICAL CHARACTERISTICS (See Figure 3)

(V_{CC} = +4.5V to +5.5V, T_A = -20°C to +70°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 8)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 8)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 8)			400	pF

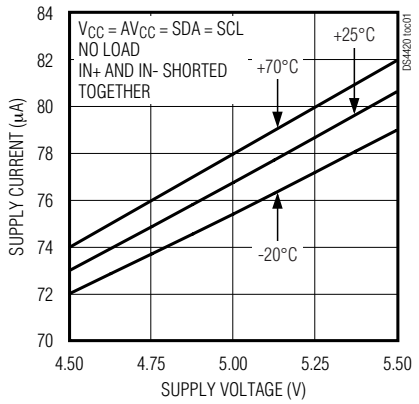
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Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive, and currents exiting the IC are negative.
Note 2: Standby supply current specified with SDA = SCL = V_{CC}, the output disconnected, and A0, A1, and A2 driven to within 100mV of V_{CC} or GND.
Note 3: Input resistance during mute and power-down is approximately one-half of the active-mode resistance.
Note 4: Each output is capable of driving a 100nF capacitive load to ground using an external 10Ω series resistor. However, output capacitance should be minimal for optimal distortion performance.
Note 5: Guaranteed by design.
Note 6: This is the time it takes for the output to become active after exiting standby mode.
Note 7: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard-mode timing.
Note 8: C_B = total capacitance of one bus line in picofarads.
Note 9: The current specified is the sum of V_{CC} and AV_{CC} supply currents.
Note 10: Gain accuracy specified assuming the output impedance of signal source driving of the DS4420 is ≤ 2.5kΩ.

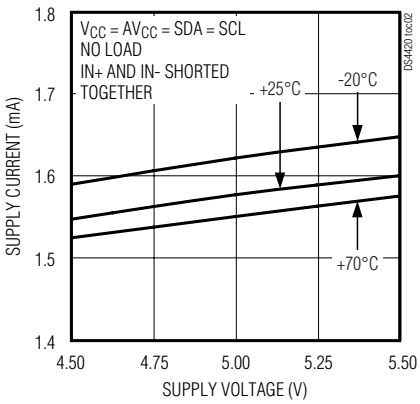
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = AV_{CC} = 5.0V, unless otherwise noted.)

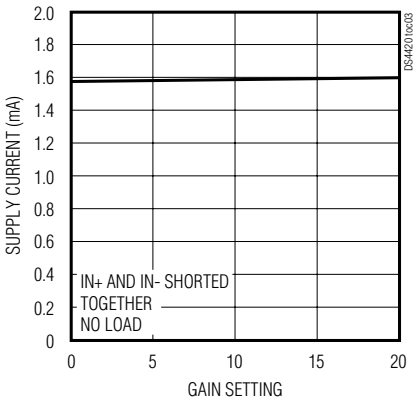
SUPPLY CURRENT vs. SUPPLY VOLTAGE (STANDBY MODE ENABLED)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (SETTING AT -11dB)



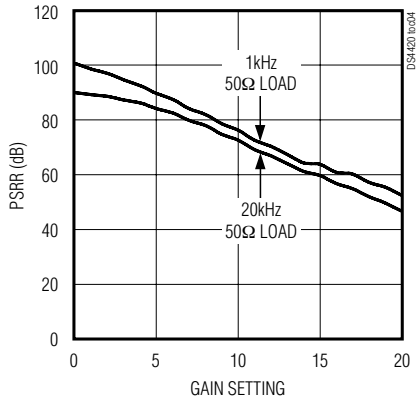
SUPPLY CURRENT vs. GAIN SETTING



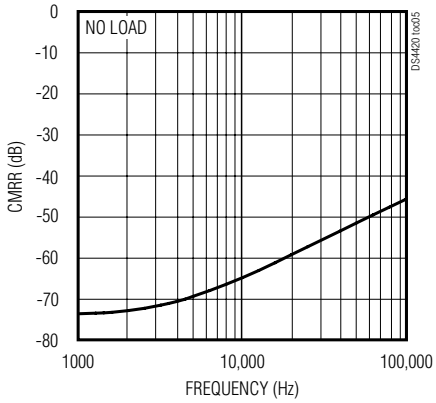
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = AV_{CC} = 5.0V, unless otherwise noted.)

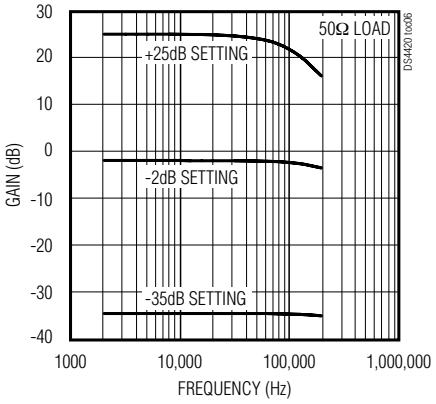
POWER-SUPPLY REJECTION RATIO vs. GAIN SETTING



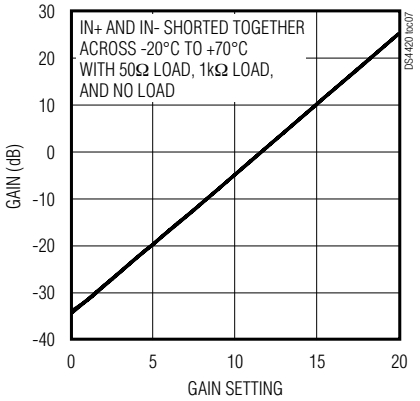
COMMON-MODE FREQUENCY RESPONSE SWEEP AT -11dB



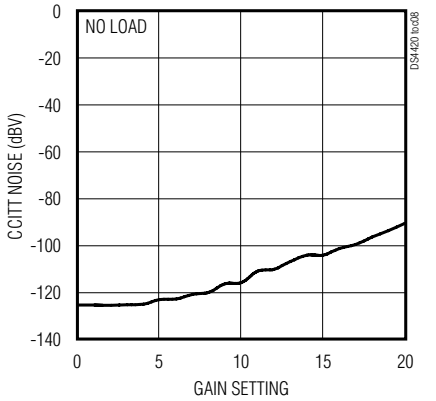
GAIN vs. FREQUENCY RESPONSE



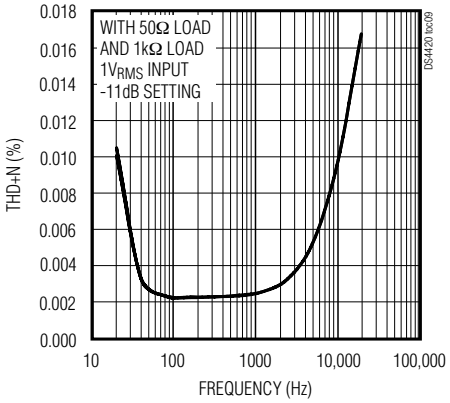
GAIN vs. SETTING



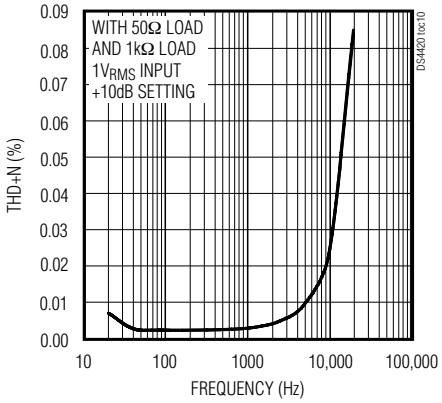
CCITT NOISE vs. GAIN SETTING



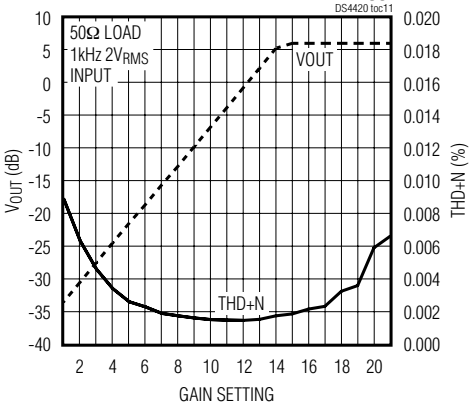
TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. V_{OUT}



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Pin Description

PIN	NAME	FUNCTION
1	A2	Address Select Inputs—Determine I²C Slave Address. Device address is $1010A_2A_1A_0$.
2	A1	
3	A0	
4	SCL	I²C Serial Clock—Input for I²C Clock
5	SDA	I²C Serial Data—Input/Output for I²C Data
6	V_{CC}	Digital Power-Supply Terminal
7	GND	Ground
8	IN+	Differential Audio Input Signal
9	IN-	
10	N.C.	No Connection
11	AGND	Analog Ground (Must be Connected to GND)
12	OUT-	Differential Audio Output Signal
13	OUT+	
14	AV_{CC}	Analog Power Supply (Must be Connected to V_{CC})
EP	EP	Exposed Paddle. Connect to GND and AGND.

Detailed Description

The key features of the DS4420 are illustrated in the *Block Diagram*.

Controlling the DS4420

The DS4420 is controlled through the I²C serial interface. Gain, mute, and standby settings all reside in one control register located at memory address F8h (see Figure 1). Writes to other memory addresses are invalid.

Programmable Gain

The gain is adjustable from -35dB to +25dB in 3dB increments. The gain is determined by the five LSBs of the control register as shown in Figure 1. Gain settings greater than 14h are invalid.

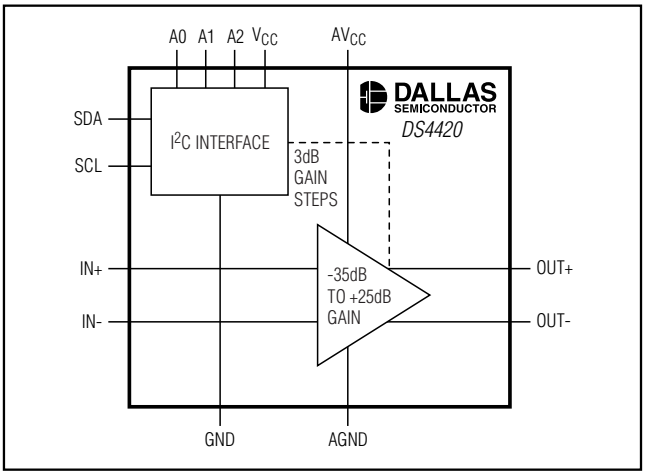
Mute Mode

The DS4420 is placed in mute mode by setting the mute bit located in the control register (see Figure 1). When in this mode, the output of the amplifier is muted and is independent of the gain setting. The input-to-output attenuation is specified in the *Electrical Characteristics* table as A_{MUTE}.

Standby Mode

Standby mode is entered by setting the standby control bit (see Figure 1). Setting the standby control bit mutes the output of the amplifier and places the DS4420 into a low-current (I_{STBY}) consumption state. Unlike mute mode, however, standby mode is intended for use when no input signal is present. While in standby mode, the DS4420 maintains input and output common-mode bias voltages. The device produces no audible clicks or pops when entering or exiting the standby state. The time required for the output to become active when exiting standby mode is specified as t_{PU}.

Block Diagram



Control Register (F8h)

Power-Up Default: 1000 0000 b

	bit 7						bit 0
F8h	Standby	x	Mute	Gain Setting[4:0]			

bit 7	**Standby:** Places the DS4420 in standby mode. 0 = Normal operation. 1 = Places the DS4420 in standby mode. (Power-up default.)
bit 6	**Don't care.**
bit 5	**Mute:** Mutes the amplifier output, regardless of the current gain setting. 0 = Normal operation. (Power-up default.) 1 = Mutes the amplifier output.
bit 4:0	**Gain Setting:** Five-bit gain setting. The power-up default is setting 00h.

GAIN SETTING (hex)	GAIN (dB)	GAIN SETTING (hex)	GAIN (dB)
00h	-35	0Bh	-2
01h	-32	0Ch	+1
02h	-29	0Dh	+4
03h	-26	0Eh	+7
04h	-23	0Fh	+10
05h	-20	10h	+13
06h	-17	11h	+16
07h	-14	12h	+19
08h	-11	13h	+22
09h	-8	14h	+25
0Ah	-5	15h to 1Fh	Illegal

Figure 1. Control Register Description

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 2). The DS4420's slave address is determined by the state of the A0, A1, and A2 address pins. These pins allow up to eight DS4420s to reside on the same I²C bus. Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions. For example, the DS4420's slave address byte is A0h when A0, A1, and A2 pins are grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

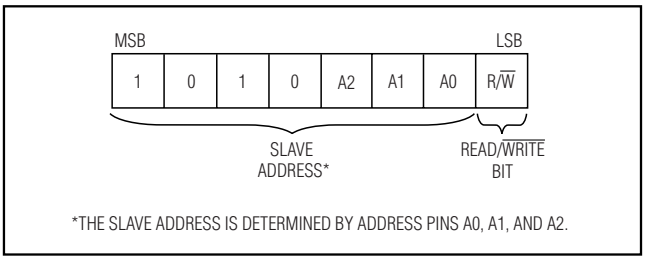


Figure 2. DS4420 Slave Address Byte

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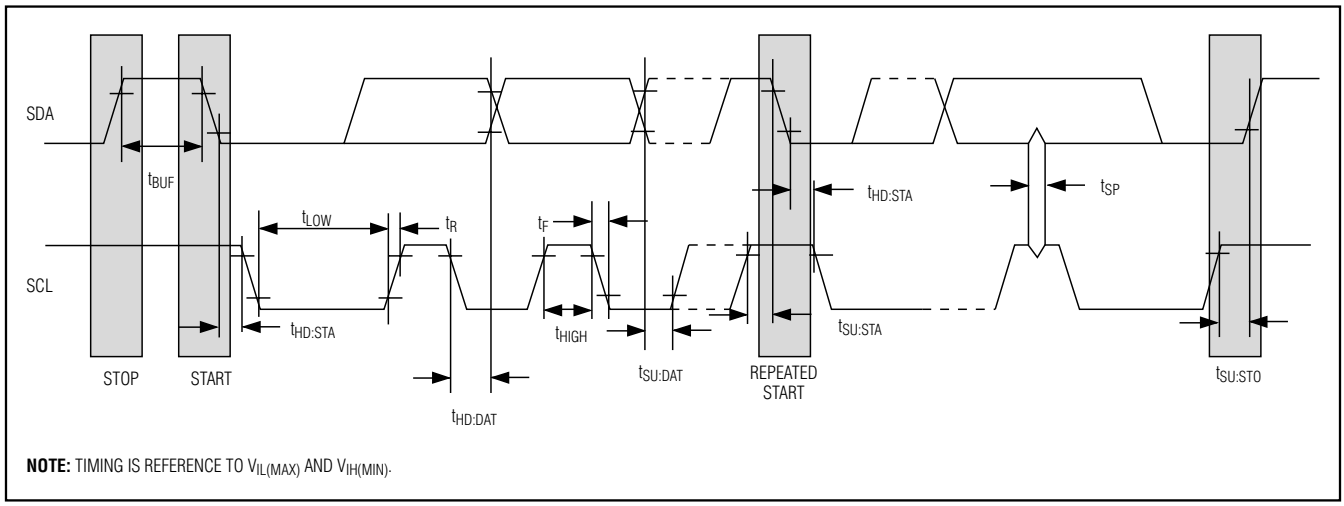


Figure 3. I²C Timing Diagram

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. See the timing diagram (Figure 3) and the *I²C AC Electrical Characteristics* table for additional information.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, start and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one (done by releasing SDA) during the 9th bit. Timing (Figure 3) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a start condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS4420's slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 2. Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ is set to a 1, (A1h in this case), the master is indicating it wants to read from the slave.

If an incorrect (nonmatching) slave address is written, the DS4420 will assume the master is communicating with another I²C device and ignore the communication until the next start condition is sent.

Memory Address: During an I²C write operation to the DS4420, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a stop condition. The master must read the slave's acknowledgement during all byte write operations.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. A dummy write cycle can be used to force the address pointer to a desired location. To do this, the master generates a start condition, writes the slave address byte (R/$\overline{W}$ =0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address byte (R/$\overline{W}$ = 1), reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition.

See Figure 4 for I²C communication examples.

Applications Information

Power-Supply Decoupling

The DS4420 has separate supply voltages for its analog and digital circuitry. For best noise and distortion performance, place a 0.1µF or 0.01µF capacitor from V_{CC} to GND and from AV_{CC} to AGND. These capacitors should be placed as close as possible to the supply and ground pins of the device.

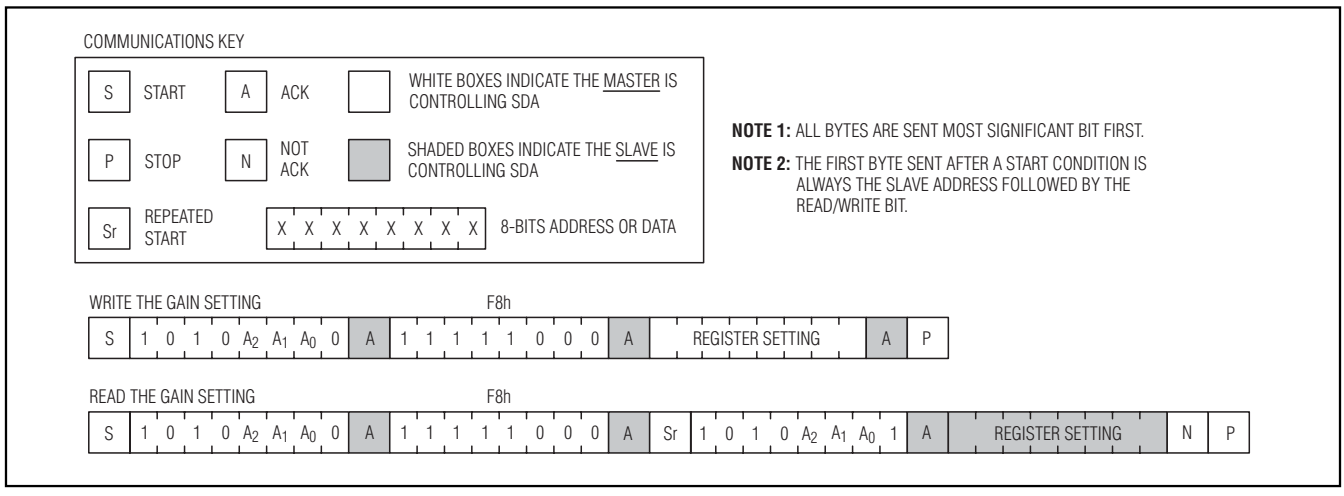


Figure 4. I²C Communication Examples

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Exposed Paddle

The DS4420 exposed paddle is not electrically isolated. It must be soldered to ground for proper operation.

Input-Coupling Capacitors

The DS4420 is designed to be operated with an AC-coupled input signal. The input resistance, R_{IN}, is sufficiently large to allow the use of small and inexpensive external capacitors. The input resistance combined with the AC-coupling capacitor will create a highpass filter. The -3dB cutoff frequency of the highpass, f_C, is given by:

$$f_C = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

where C_{IN} is the external coupling capacitor and R_{IN} is the internal input resistance.

At the cutoff frequency, the input signal will be attenuated 3dB, with less attenuation as the signal's frequency increases beyond the cutoff frequency. To guarantee passband flatness, the cutoff frequency of the filter should be designed using the specified minimum input resistance, and placed well below the desired flat band of the circuit. The typical input resistance should only be used to estimate typical performance.

Internal Ground Connections

The DS4420's ground pins, GND and AGND, must be connected together externally. Internally, they are connected as shown in Figure 5.

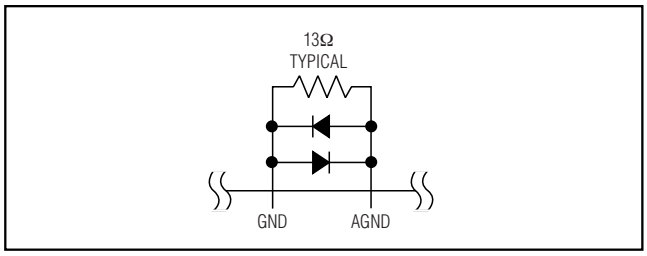


Figure 5. Internal Ground Connections

Chip Topology

TRANSISTOR COUNT: 5347

SUBSTRATE CONNECTED TO: Ground

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

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