19-2547; Rev 0; 7/02

MAXIM

Smallest 1A, 1.4MHz Step-Down Regulators

General Description

The MAX1973/MAX1974 are constant-frequency 1.4MHz pulse-width-modulated (PWM) current-mode step-down regulators. The output voltage can be set as low as 0.75V using an external voltage-divider, or it can be set to preset outputs of 1V, 1.5V (MAX1974), 1.8V, or 2.5V (MAX1973) without requiring external resistors. The MAX1973 also includes a voltage-margining feature that offsets the output voltage up or down 4% to facilitate board-level production testing.

A fixed 1.4MHz operating frequency ensures operation outside the DSL frequency band, provides fast transient response, and allows the use of small external components. Only 4.7µF input and output ceramic capacitors are needed for 1A applications. Forced PWM operation ensures a constant switching frequency over all load conditions.

Output voltage accuracy is ±1% over load, line, and temperature operating ranges. The MAX1973 features voltage margining; the MAX1974 provides a POK output to indicate when the output has reached 90% of its nominal regulation voltage. Both devices are available in small 10-pin µMAX packages.

Applications

Network Equipment

Cellular Base Stations

DSL and Wireless Modems/Routers

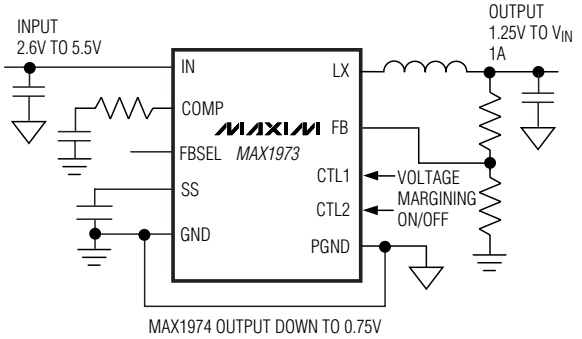
Optical Modules

Central-Office DSL and Telecom

DSP/ASIC Core and IO supplies

Selector Guide appears at end of data sheet.

Typical Operating Circuit



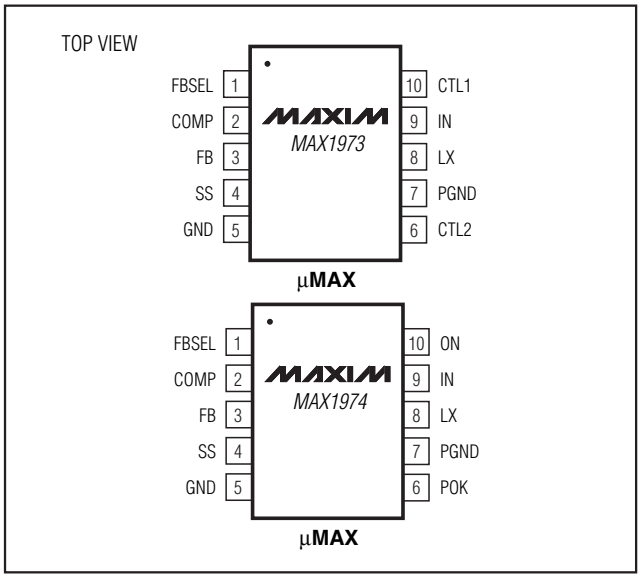
Features

- **Tiny Circuit Footprint of 0.19in²**
- **Ultra-Low Circuit Height of 1.8mm**
- **4.7µF Ceramic Input and Output Capacitors**
- **2.6V to 5.5V Input Voltage**
- **1A Output Current**
- **1% Accurate**
- **Built-In ±4% Logic-Controlled Voltage Margining (MAX1973)**
- **Preset 1V, 1.5V, 1.8V, 2.5V, or 0.75V to V_{IN} Adjustable Output**
- **Fixed-Frequency PWM Current-Mode Operation**
- **1.4MHz Switching Frequency, Operate Outside DSL Band**
- **100% Duty-Cycle Dropout Capability**
- **Small External Components**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1973EUB	-40°C to +85°C	10 µMAX
MAX1974EUB	-40°C to +85°C	10 µMAX

Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

IN, POK, CTL1, CTL2, FBSEL, ON to GND .....-0.3V to +6V
COMP, FB, SS to GND .....-0.3V to (V_{IN} + 0.3V)
PGND to GND .....-0.3V to +0.3V
LX Current (Note 1).....-2.4A to +2.4A

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to IN and PGND. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{CTL_}$ = 3.3V, FB = OUT, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN						
IN Voltage Range			2.6		5.5	V
IN Undervoltage Lockout Threshold	Rising and falling, hysteresis is 25mV (typ)		2.2	2.35	2.5	V
Supply Current	Switching with no load			4.0	7.5	mA
Supply Current in Dropout	V_{OUT} set for 3.6V			3	5	mA
Shutdown Supply Current	V_{IN} = 5.5V			0.1	10	µA
FB						
Output Voltage Range	MAX1973		1.25		V_{IN}	V
	MAX1974		0.75		V_{IN}	
FB Regulation Voltage	MAX1973	FBSEL not connected	1.2375	1.25	1.2625	V
		FBSEL = GND	1.7820	1.8	1.8180	
		FBSEL = IN	2.4750	2.5	2.5250	
	MAX1974	FBSEL not connected	0.7425	0.75	0.7575	
		FBSEL = GND	0.99	1.00	1.01	
		FBSEL = IN	1.485	1.500	1.515	
FB Regulation Voltage Positive Voltage Margining	MAX1973, CTL1 = GND, CTL2 = IN		+3	+4	+5	%
FB Regulation Voltage Negative Voltage Margining	MAX1973, CTL1 = IN, CTL2 = GND		-3	-4	-5	%
FB Input Resistance to GND in Preset Output Modes			10	30	70	kΩ
FB Input Bias Current	FBSEL not connected		-0.1	0.01	+0.1	µA
SS (REFERENCE OUTPUT)						
SS Voltage	MAX1974			0.75		V
	MAX1973			1.25		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{CTL_}$ = 3.3V, FB = OUT, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SS Source Current			-25	-20	-15	µA
SS Sink Current			10	20	35	µA
SS to GND Resistance in Shutdown			5	40	100	Ω
FBSEL						
Low Input Threshold			0.3			V
High Input Threshold					V_{IN} - 0.3	V
Input Bias Current	FBSEL = GND or IN, V_{IN} = 5.5V		-20	10	+20	µA
COMP						
Transconductance from FB to COMP			40	60	80	µS
COMP to GND Resistance in Shutdown			5	40	100	Ω
Clamp Voltage Low			0.6	0.9	1.2	V
Clamp Voltage High			1.35	1.75	2.15	V
LX						
On-Resistance High	V_{IN} = 3.3V			0.23	0.46	Ω
On-Resistance Low	V_{IN} = 3.3V			0.16	0.32	Ω
Current-Sense Transresistance			0.275	0.335	0.425	V/A
Positive Current-Limit Threshold			1.1	1.6	1.75	A
Negative Current-Limit Threshold			-1.2	-0.8	-0.4	A
LX Shutdown Leakage Current		V_{LX} = V_{IN} = 5.5V			20	µA
		LX = GND, V_{IN} = 5.5V	-20			
Switching Frequency			1.2	1.4	1.6	MHz
CTL1, CTL2 (MAX1973), ON (MAX1974)						
Logic-Low Input Threshold			0.6			V
Logic-High Input Threshold					1.6	V
Logic Input Current			-1		+1	µA
POK (MAX1974 only)						
Output Low Voltage	POK sinking 1mA			10	100	mV
Output Valid Threshold for POK	Percentage of nominal regulation voltage	Rising	90	92.5	95	%
		Falling	88	90	92	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{CTL_}$ = 3.3V, FB = OUT, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN					
Thermal-Shutdown Threshold			+170		°C
Thermal-Shutdown Hysteresis			20		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{FB} = $V_{CTL_}$ = 3.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN						
IN Voltage Range			2.6		5.5	V
IN Undervoltage Lockout Threshold	Rising and falling, hysteresis is 25mV (typ)		2.2		2.5	V
Supply Current	Switching with no load				7.5	mA
Supply Current in Dropout	V_{OUT} set for 3.6V				5	mA
Shutdown Supply Current	V_{IN} = 5.5V				10	µA
FB						
Output Voltage Range	MAX1973		1.25		V_{IN}	V
	MAX1974		0.75		V_{IN}	
FB Regulation Voltage	MAX1973	FBSEL not connected	1.2375		1.2625	V
		FBSEL = GND	1.7820		1.8180	
		FBSEL = IN	2.4750		2.5250	
	MAX1974	FBSEL not connected	0.7425		0.7575	
		FBSEL = GND	0.99		1.01	
		FBSEL = IN	1.485		1.515	
FB Regulation Voltage Positive Voltage Margining	MAX1973, CTL1 = GND, CTL2 = IN		3		5	%
FB Regulation Voltage Negative Voltage Margining	MAX1973, CTL1 = IN, CTL2 = GND		-3		-5	%
FB Input Resistance to GND in Preset Output Modes			10		70	kΩ
FB Input Bias Current	FBSEL not connected		-0.15		+0.15	µA
SS (REFERENCE OUTPUT)						
SS Source Current			-25		-15	µA
SS Sink Current			10		35	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{CTL_}$ = 3.3V, FB = OUT, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SS to GND Resistance in Shutdown			5	40	100	Ω
FBSEL						
Low Input Threshold			0.3			V
High Input Threshold					V_{IN} - 0.4	V
Input Bias Current	FBSEL = GND or IN, V_{IN} = 5.5V		-20		+20	µA
COMP						
Transconductance from FB to COMP			40		80	µS
COMP to GND Resistance in Shutdown			5		100	Ω
Clamp Voltage Low			0.6		1.2	V
Clamp Voltage High			1.3		2.2	V
LX						
On-Resistance High	V_{IN} = 3.3V				0.46	Ω
On-Resistance Low	V_{IN} = 3.3V				0.32	Ω
Current-Sense Transresistance			0.275		0.425	V/A
Positive Current-Limit Threshold			1.10		1.85	A
Negative Current-Limit Threshold			-1.20		-0.35	A
LX Shutdown Leakage Current		V_{LX} = V_{IN} = 5.5V			20	µA
		LX = GND, V_{IN} = 5.5V	-20			
Switching Frequency			1.2		1.6	MHz
CTL1, CTL2 (MAX1973), ON (MAX1974)						
Logic-Low Input Threshold			0.6			V
Logic-High Input Threshold					1.6	V
Logic Input Current			-1		1	µA
POK (MAX1974 only)						
Output Low Voltage	POK sinking 1mA				100	mV
Output Valid Threshold for POK	Percentage of nominal regulation voltage	Rising	90		95	%
		Falling	88		92	

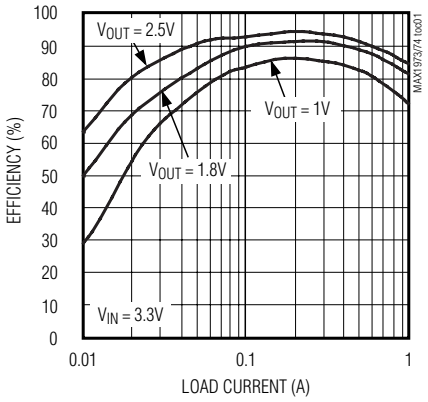
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

Smallest 1A, 1.4MHz Step-Down Regulators

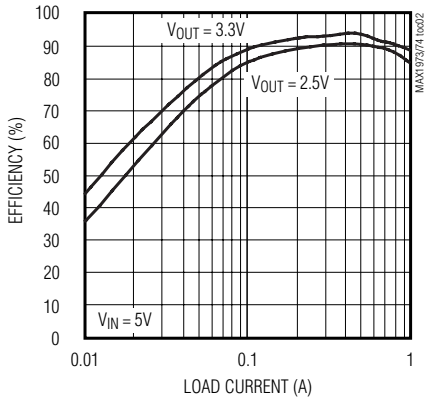
Typical Operating Characteristics

(Circuits of Figure 2, 3, and 4; T_A = +25°C, unless otherwise noted.)

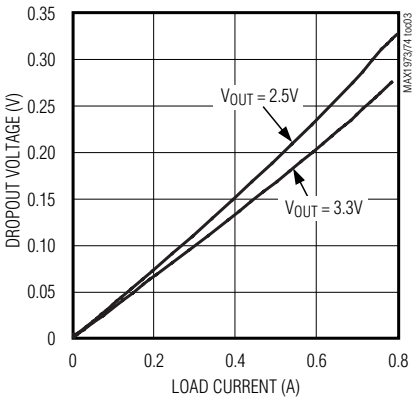
EFFICIENCY vs. LOAD CURRENT



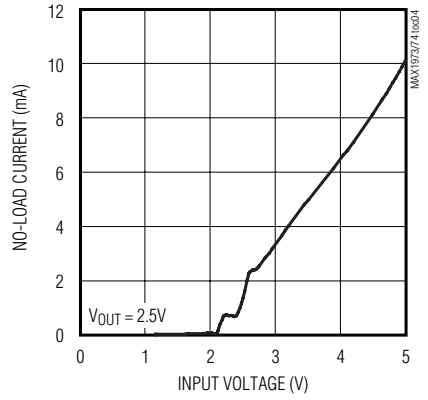
EFFICIENCY vs. LOAD CURRENT



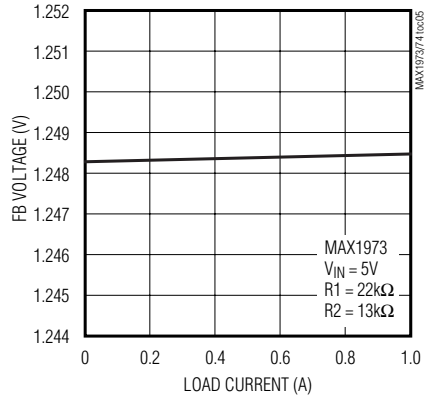
DROPOUT VOLTAGE vs. LOAD CURRENT



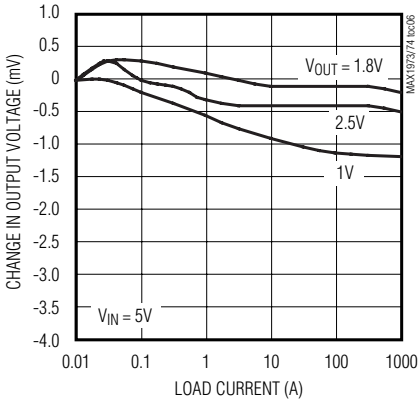
NO-LOAD CURRENT vs. INPUT VOLTAGE



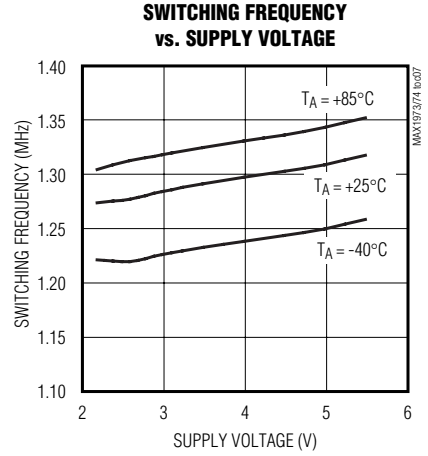
FB VOLTAGE vs. LOAD CURRENT



CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT



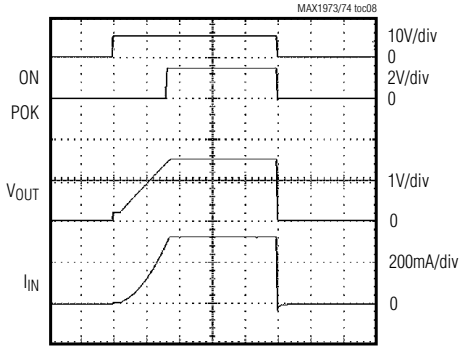
SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

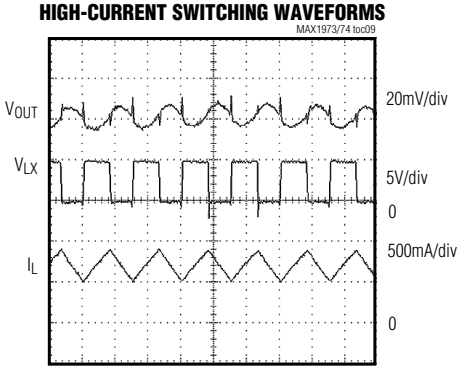
(Circuits of Figure 2, 3, and 4; T_A = +25°C, unless otherwise noted.)

MAX1974
STARTUP WAVEFORMS



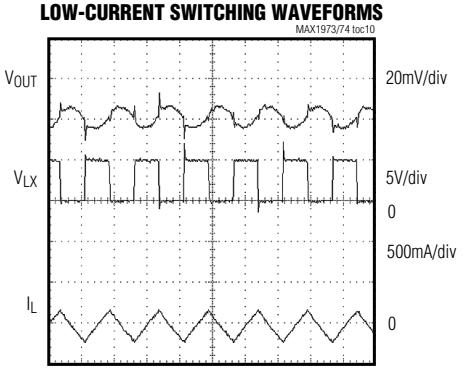
V_{IN} = 5V, 100kΩ PULLUP RESISTOR POK TO V_{OUT}

MAX1973
HIGH-CURRENT SWITCHING WAVEFORMS



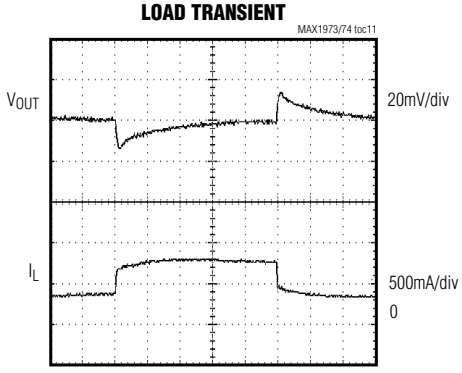
500ns/div
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 800mA

MAX1973
LOW-CURRENT SWITCHING WAVEFORMS



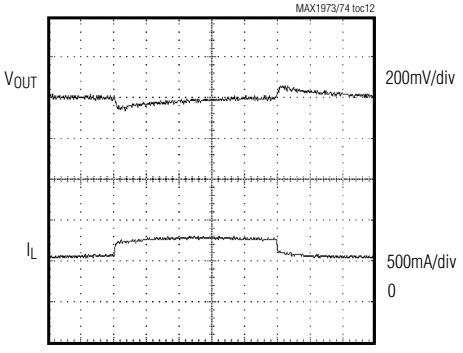
500ns/div
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 10mA

MAX1973
LOAD TRANSIENT



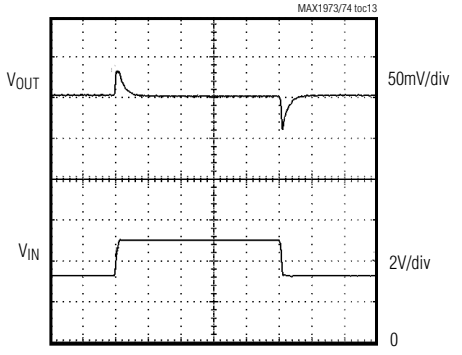
500ns/div
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 400mA TO 800mA

MAX1973
LOAD TRANSIENT



20µs/div
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 600mA TO 800mA

MAX1973
LINE TRANSIENT



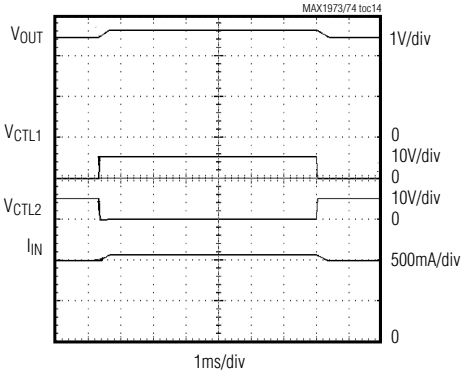
200µs/div
V_{IN} = 3.3V TO 5V TO 3.3V, I_{OUT} = 800mA

Smallest 1A, 1.4MHz Step-Down Regulators

Typical Operating Characteristics (continued)

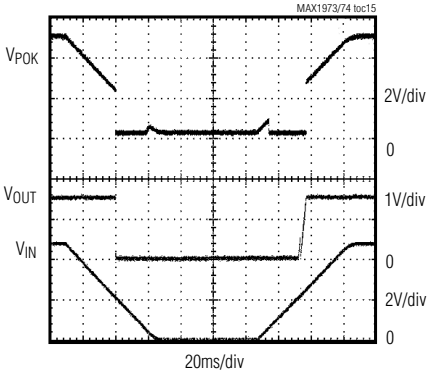
(Circuits of Figure 2, 3, and 4; T_A = +25°C, unless otherwise noted.)

MAX1973
VOLTAGE MARGIN STEP CHANGE RESPONSE



V_{IN} = 5V, VOUT = 2.5V, I_{OUT} = 800mA, -4% TO +4% TO -4%

MAX1974
POK AND INPUT VOLTAGE



MAX1974 WITH 100kΩ PULLUP RESISTOR
FROM POK TO IN, I_{LOAD} = 100mA

Pin Description

PIN	NAME		FUNCTION
	MAX1973	MAX1974	
1	FBSEL	FBSEL	Feedback-Mode Selector. Connect FBSEL to GND to set the output voltage to 1.8V (MAX1973) or 1V (MAX1974). Connect FBSEL to IN to set the output voltage to 2.5V (MAX1973) or 1.5V (MAX1974). Leave FBSEL unconnected to set the output voltage using a resistor-divider at FB.
2	COMP	COMP	Compensation. Connect a series RC network to GND. COMP is internally pulled to GND when the device is in shutdown or in undervoltage lockout (see the *Compensation Components* section).
3	FB	FB	Feedback Input. Connect to the output if a preset voltage is used, or to a resistor-divider from the output to GND for an adjustable output voltage.
4	SS	SS	Soft-Start Pin and Reference Output. Bypass to GND with at least 0.01µF. Connect 0.1µF to GND for a soft-start ramp time of 6.25ms for the MAX1973, or 3.75ms for the MAX1974. SS is internally pulled to GND when the device is shut down or in undervoltage lockout.
5	GND	GND	Ground
6	CTL2	—	Control Input 2. Controls enable/disable and voltage margining (see Table 1).
	—	POK	Power-OK Output. Open-drain output goes low when output is below 90% of nominal output. POK is also low when the device is shut down or in undervoltage lockout.
7	PGND	PGND	Power Ground
8	LX	LX	Inductor Connection. Connect an inductor from LX to the output.
9	IN	IN	Input Supply Voltage. Input voltage range is 2.6V to 5.5V. Connect a 4.7µF capacitor from IN to PGND.
10	CTL1	—	Control Input 1. Controls Enable/Disable and voltage margining (see Table 1).
	—	ON	Enable Input. Connect to IN or drive high for normal operation. Drive low to put device in shutdown.

Detailed Description

The MAX1973/MAX1974 are 1.4MHz fixed-frequency PWM current-mode step-down DC/DC converters. A high 1.4MHz switching frequency allows use of small inductors and small capacitors for filtering and decoupling. An internal synchronous rectifier improves efficiency and eliminates the need for an external Schottky freewheeling diode. On-chip current sensing uses the on-resistance of the internal MOSFETs, eliminating current-sensing resistors and improving efficiency.

The input voltage range is 2.6V to 5.5V. The output voltage is selectable to one of two presets, or adjustable by using a resistor-divider. The output voltage of the MAX1973 is preset to 1.8V or 2.5V by connecting FBSEL to GND or IN, respectively. The MAX1974 is preset to 1.0V or 1.5V by connecting FBSEL to GND or IN, respectively. In adjustable mode (see the *Output Voltage Selection* section), the output voltage is programmable down to 0.75V on the MAX1974, and down to 1.25V on the MAX1973.

PWM Control Scheme

The MAX1973/MAX1974 use a fixed-frequency PWM current-mode control scheme. The heart of the PWM current-mode controller is an open-loop comparator that compares the integrated voltage feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp (see Figure 1). At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in a magnetic field.

The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Because the average inductor current is nearly the same as the peak inductor current (assuming that the inductor value is relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the output LC filter pole, normally found in a voltage-mode PWM, to a higher frequency. To preserve inner loop stability and eliminate inductor staircasing, an internal slope-compensation ramp is summed into the main PWM comparator.

During the second half of the switching cycle (off-time), the internal high-side MOSFET turns off and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit, the high-side MOSFET is not turned on at the rising edge of the clock, and the low-side MOSFET remains on to let the inductor current ramp down.

100% Duty-Cycle Operation

The MAX1973/MAX1974 can operate at 100% duty cycle. In this state, the high-side P-channel MOSFET is turned on (not switching). The dropout voltage in 100% duty-cycle operation is the output current multiplied by the sum of the on-resistance of the P-channel MOSFET ($R_{DS(ON)P}$) and the inductor resistance (R_L).

$$V_{DROPOUT} = I_{OUT} \times (R_{DS(ON)P} + R_L)$$

Current Sense and Current Limit

The current-sense circuit amplifies the current-sense voltage generated by the high-side MOSFET's on-resistance and the inductor current ($R_{DS(ON)} \times$ INDUCTOR). This amplified current-sense signal and the internal slope compensation signal are summed together at the PWM comparator's inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the integrated feedback voltage.

The internal high-side MOSFET has a current limit of 1.6A (typ). If the current flowing out of LX exceeds this maximum, the high-side MOSFET turns off and the synchronous rectifier MOSFET turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. There is also a synchronous rectifier current limit of -0.85A, to protect the device from current flowing into LX. If this negative current limit is exceeded, the synchronous rectifier turns off, and the inductor current continues to flow through the high-side MOSFET body diode back to the input until the beginning of the next cycle, or until the inductor current drops to zero.

Soft-Start

To reduce the supply inrush current, soft-start circuitry ramps up the output voltage during startup by charging the SS capacitor with a 20µA current source. When SS reaches its nominal value, the output is in full regulation. The soft-start time (t_{SS}) is determined from:

$$t_{SS} = \frac{V_{SS}}{I_{SS}} \times C_{SS}$$

where V_{SS} is the soft-start (reference) voltage (1.25V for the MAX1973; 0.75V for the MAX1974), I_{SS} is 20µA, and C_{SS} is the value of the capacitor connected to SS.

Soft-start occurs when power is first applied and when the device exits shutdown. The part also goes through

Smallest 1A, 1.4MHz Step-Down Regulators

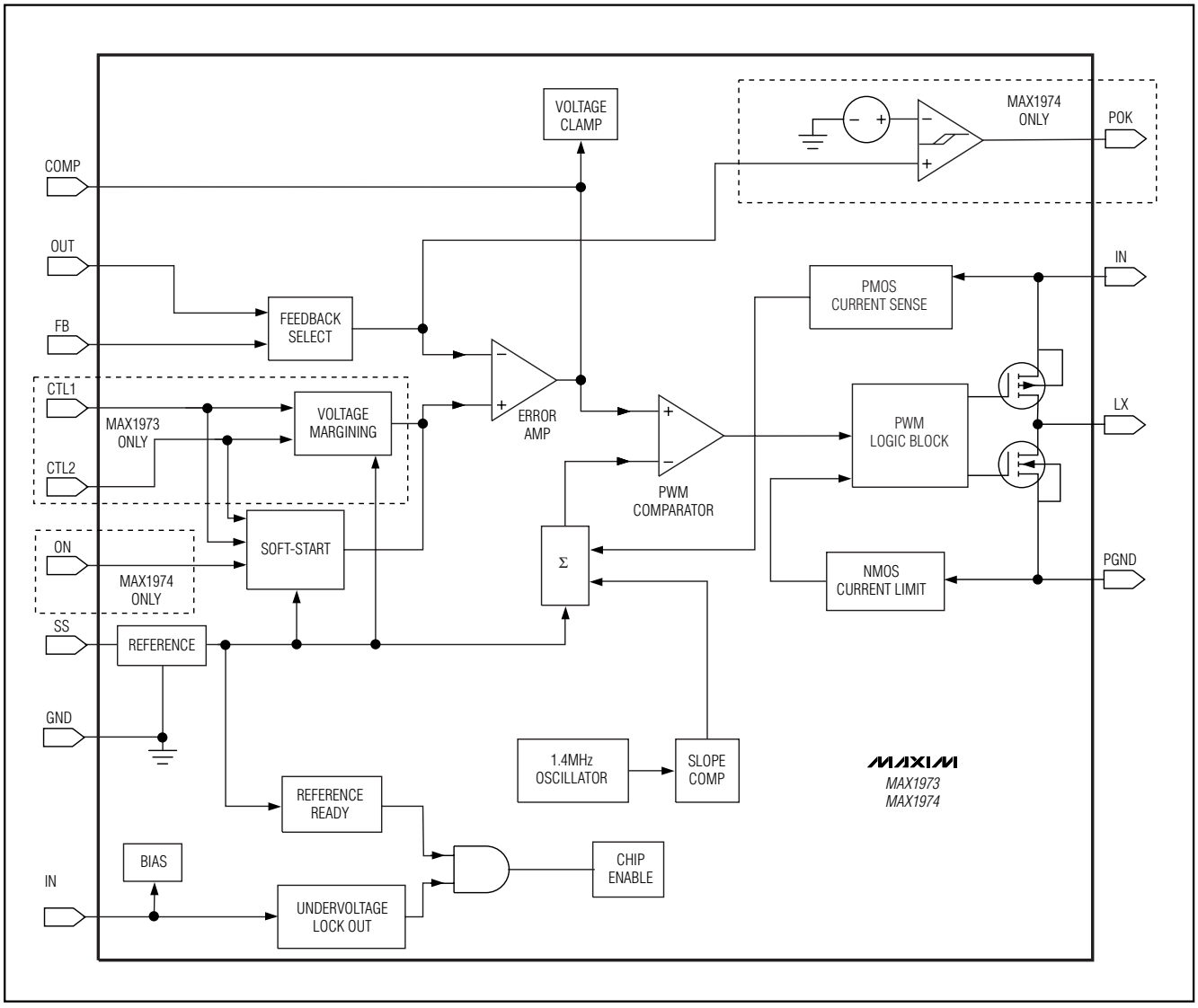


Figure 1. Functional Diagram

soft-start when coming out of undervoltage lockout (UVLO) or thermal-overload protection.

Undervoltage Lockout (UVLO)

If V_{IN} drops below 2.35V (typ), the MAX1973/MAX1974 assume that the supply voltage is too low to provide a valid output voltage, and the UVLO circuit inhibits switching. Once V_{IN} rises above 2.4V, UVLO is disabled and the soft-start sequence begins.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation and protects the IC from damage in case of an overload or short-circuit condition. When the IC junction temperature (T_J) exceeds +170°C, the device shuts down. The part turns on again after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Voltage Margining and Shutdown

A voltage-margining feature is provided on the MAX1973 to shift the output voltage up or down by 4%. Voltage margining is useful for the automatic testing of systems at high and low supply conditions to find potential failures. See Table 1 for the MAX1973 voltage margining and shutdown truth table.

A shutdown feature is included on both the MAX1973 and the MAX1974. Shutdown turns off the IC and reduces the supply current about 0.1µA. For the MAX1974, drive ON high for normal operation, or low for shutdown. For the MAX1973, drive both CTL1 and CTL2 high for normal operation, or drive both low for shutdown. For a simple enable/shutdown function with no voltage margining on the MAX1973, connect CTL1 to CTL2 and drive as one input.

Power-OK Output (POK)

A power-OK output (POK) is provided on the MAX1974. This is an open-drain output indicating when the output voltage is in regulation. If the output voltage falls below 90% of its nominal value, POK goes low. POK remains low until the output voltage rises to 92.5% of its nominal value. At that point, POK goes high impedance. To use POK as a logic output, connect a 10kΩ to 100kΩ pullup resistor from POK to the power supply of the logic receiving the POK signal. POK continues to function in shutdown or UVLO. Note that a minimum voltage of 1V at IN is required to ensure that POK provides a valid output. When V_{IN} drops to zero, POK is high impedance. See the *Typical Operating Characteristics.*

Applications Information

Output Voltage Selection

The output voltage can be set to one of two preset values, or can be set by an external resistor-divider. For preset output voltages, connect FB to the output as shown in Figures 2 and 3. Connect FBSEL to GND or IN to select the desired preset output voltage (see Table 2).

To set the output voltage to a value other than the preset values, FBSEL is not connected, and FB is connected to a voltage-divider as shown in Figures 4 and 5. Select a value for R2 in the 1kΩ to 22kΩ range, and then calculate the value of R1 from the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Table 1. CTL_ Input Functions (MAX1973)

CTL1	CTL2	FUNCTION
GND	GND	Shutdown
GND	IN	Positive voltage margining, regulation voltage increased 4% from normal operation
IN	GND	Negative voltage margining, regulation voltage lowered 4% from normal operation
IN	IN	Normal operation

Table 2. Preset Output Voltages

FBSEL	OUTPUT VOLTAGE	
	MAX1973	MAX1974
GND	1.8V	1V
IN	2.5V	1.5V
Not Connected	Adjustable down to 1.25V	Adjustable down to 0.75V

For the MAX1973, V_{FB} = 1.25V, allowing its output to be set down to 1.25V. For the MAX1974, V_{FB} = 0.75V, allowing its output to be set down to 0.75V

The MAX1973/MAX1974 PWM circuitry is capable of a stable minimum duty cycle of 17%. This limits the minimum output voltage that can be generated to 0.17 × V_{IN}. Instability may result for V_{IN}/V_{OUT} ratios below 0.17.

Inductor Selection

A 2.2µH to 4.7µH inductor with a saturation current of at least 1.25A is recommended for full-load (1mA) applications. For lower load currents, the inductor current rating can be reduced. For most applications, use an inductor with a current rating 1.25 times the maximum required output current. For best efficiency, the inductor's DC resistance should be as small as possible. See Table 3 for recommended inductors and manufacturers.

For most designs, the inductor value (L_{INIT}) can be derived from the following equation:

$$L_{INIT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW}}$$

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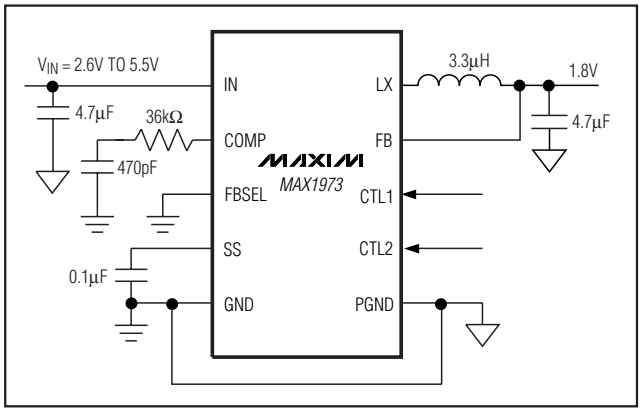


Figure 2. MAX1973 with 1.8V Preset Output

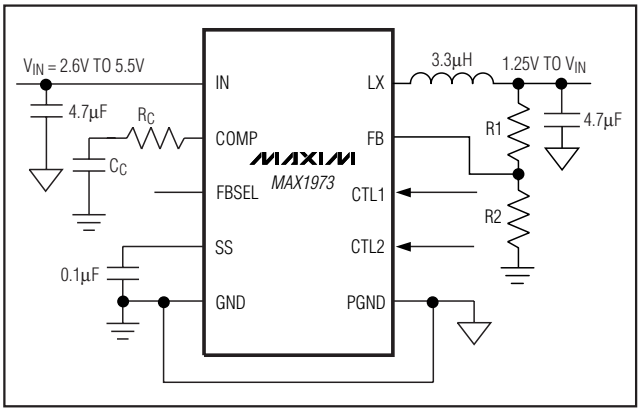


Figure 4. MAX1973 with Adjustable Output Voltage Set by R1 and R2

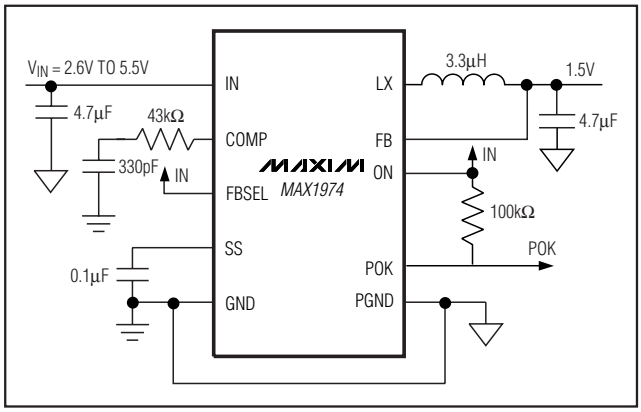


Figure 3. MAX1974 with Preset 1.5V Output

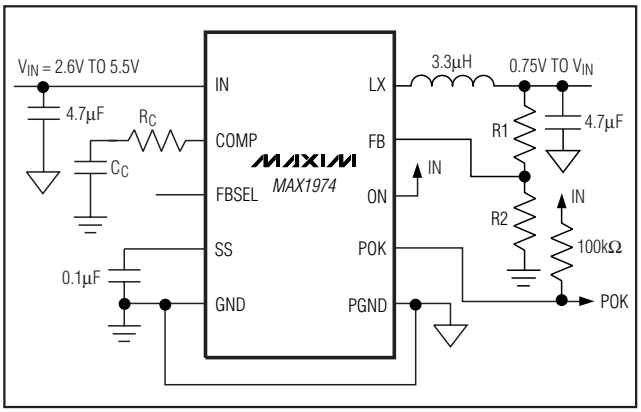


Figure 5. MAX1974 with Adjustable Output Voltage Set by R1 and R2

where f_{SW} is the switching frequency (1.4×10^6 Hz), and LIR is the inductor ripple current as a percentage of the maximum load current. Keep LIR between 20% and 40% for best compromise of cost, size, and performance. The peak inductor current is approximately:

$$I_{L(PEAK)} = \left[1+\frac{LIR}{2}\right]\times I_{OUT(MAX)}$$

Input Capacitor

A 4.7µF ceramic input capacitor is recommended for most applications because of its low equivalent series resistance (ESR), equivalent series inductance (ESL), and cost. To ensure stability over a wide temperature range, an X5R or X7R dielectric is recommended.

The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}}\sqrt{V_{OUT}(V_{IN}-V_{OUT})}$$

Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Output Capacitor

A 4.7µF ceramic output capacitor is recommended for most applications because of its low ESR, ESL, and lower cost. To ensure stability over a wide temperature range, an X5R or X7R dielectric is recommended.

Key selection parameters for a ceramic output capacitor are capacitance, ESR, and voltage rating. These affect the overall stability, output ripple voltage, and transient

Table 3. Recommended Inductors

MANUFACTURER	PART	INDUCTANCE (µH)	ESR (mΩ)	SATURATION CURRENT (A)	DIMENSIONS L × W × H (mm)
Coilcraft	LPO1704-32M	3.3	160	1.3	5.5 × 6.6 × 1
Sumida	CDRD3D16-R3	3.3	85	1.1	4 × 4 × 1.8
Toko	A682AY-3R3M	3.3	134	0.97	4.4 × 4.4 × 3.1

response of the DC-DC converter. With ceramic capacitors, the voltage ripple from ESL is negligible.

Output ripple is generated by variations in the charge stored in the output capacitance, and the voltage drop across the capacitor ESR.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

The output voltage ripple due to the output capacitance is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

The output voltage ripple due to capacitor ESR is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

I_{P-P} is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be set by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output voltage ripple. Because the inductor ripple current is inversely proportional to inductor value, output voltage ripple decreases with larger inductance.

Load transient response depends on the selected output capacitor. During a load transient, the output voltage instantly changes by ESR × ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. With a higher bandwidth the response time is faster. However, to maintain stable operation, the bandwidth should not be set above $f_{SW}/10$.

Compensation Components

An internal transconductance error amplifier compensates the control loop. Connect a series resistor and capacitor between COMP and GND to form a pole-zero pair. The external inductor, output capacitor, compensation resistor, and compensation capacitor determine the loop bandwidth and stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitor are selected to optimize the control loop. Table 4 and Table 5 list typical component values. The rest of this section is a more detailed discussion on calculating compensation components.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The voltage across the internal high-side MOSFET's on-resistance is used to sense inductor current. Current-mode control eliminates the double pole caused by the inductor and output capacitor found in other control schemes. Simple Type 1 compensation with a single resistor (R_C) and capacitor (C_C) is all that is needed to provide a stable and high-bandwidth loop.

Use the formula below to calculate the value of C_C, then use the nearest standard value:

$$C_C = \frac{V_{FB}}{0.5 \times I_{OUT(MAX)}} \times \frac{1}{R_{CS}} \times g_m \times \frac{1}{2\pi \times f_C}$$

where V_{FB} is 1.25V for the MAX1973 and 0.75V for the MAX1974, the current-sense transresistance (R_{CS}) is 0.26Ω (typ), and the transconductance from FB to COMP (g_m) is 50µS (typ). For best stability and response performance, the closed-loop unity-gain frequency (f_C) should be approximately 140kHz (one-tenth the switching frequency).

Use the following equation to calculate R_C:

$$R_C = \frac{C_{OUT}}{C_C} \times \frac{V_{OUT}}{0.5 \times I_{OUT(MAX)}}$$

Below is a numerical example of calculating compensation values for a circuit using the MAX1973 with 2.5V output and maximum output current of 1A:

MAX1973

Smallest 1A, 1.4MHz Step-Down Regulators

V_{OUT} = 2.5V
$I_{OUT(MAX)}$ = 1A
C_{OUT} = 4.7µF

V_{FB} = 1.25V
R_{CS} = 0.26Ω
g_m = 50µS
f_C = 140kHz

$$C_C = \frac{V_{FB}}{0.5 \times I_{OUT(MAX)}} \times \frac{1}{R_{CS}} \times g_m \times \frac{1}{2\pi \times f_C}$$

$$= \frac{1.25}{0.5 \times 1} \times \frac{1}{0.26} \times 50 \times 10^{-6} \times \frac{1}{2\pi \times 140000} = 547pF$$

Select the nearest standard value: C_C = 560pF

$$R_C = \frac{C_{OUT}}{C_C} \times \frac{V_{OUT}}{0.5 \times I_{OUT(MAX)}} =$$

$$\frac{4.7 \times 10^{-6}}{560 \times 10^{-12}} \times \frac{2.5}{0.5 \times 1} = 41.9k\Omega$$

Select the nearest standard value: R_C = 43kΩ

PC Board Layout

A properly designed PC board layout is important in any switching regulator. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to IC pins as possible. Keep the power ground plane (connected to PGND) and signal ground plane (connected to GND) separate. Connect the two ground planes with a single connection from PGND to GND.
2) Input and output capacitors are connected to the power ground plane; all other capacitors are connected to the signal ground plane.
3) Keep the high-current paths as short and wide as possible.
4) If possible, connect IN, LX, and PGND separately to a large land area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place feedback resistors (if used) as close to the IC as possible.
6) Route high-speed switching nodes (LX) away from sensitive analog areas (FB, COMP, SS).

Table 4. Recommended Components for the MAX1973

V_{OUT} (V)	C_{IN} (µF)	C_{OUT} (µF)	C_C (pF)	R_C (kΩ)
2.5	4.7	4.7	560	43
1.8	4.7	4.7	560	30

Table 5. Recommended Components for the MAX1974

V_{OUT} (V)	C_{IN} (µF)	C_{OUT} (µF)	C_C (pF)	R_C (kΩ)
1.5	4.7	4.7	330	43
1.0	4.7	4.7	330	27

Selector Guide

PART	FEATURES	OUTPUT PRESET
MAX1973EUB	Voltage Margining	1.8V or 2.5V
MAX1974EUB	Power-OK Output	1V or 1.5V

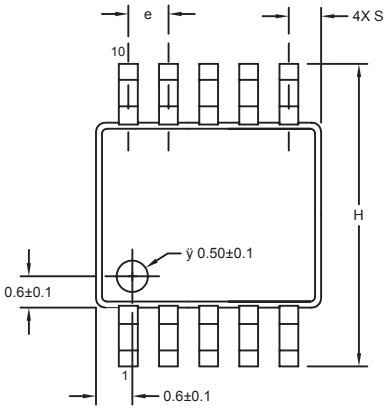
Chip Information

TRANSISTOR COUNT: 1998
PROCESS: BiCMOS

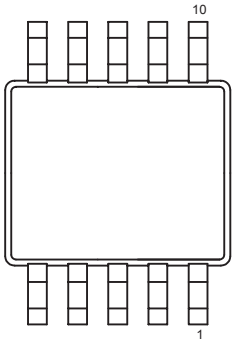
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

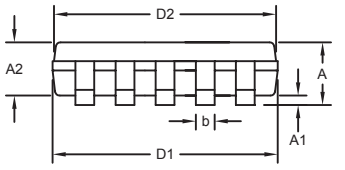


TOP VIEW

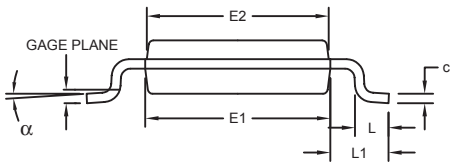


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

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