3 V, Voltage Monitoring Microprocessor Supervisory Circuits

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

FEATURES

- Precision supply voltage monitor
  - 2.63 V (ADM706P, ADM706R, ADM708R)
  - 2.93 V (ADM706S, ADM708S)
  - 3.08 V (ADM706T, ADM708T)
- 100 µA quiescent current
- 200 ms reset pulse width
- Debounced manual reset input ($\overline{MR}$)
- Independent watchdog timer
  - 1.6 second timeout (ADM706x)
- Reset output
  - Active high (ADM706P)
  - Active low (ADM706R, ADM706S, ADM706T)
  - Both active high and active low (ADM708R, ADM708S, ADM708T)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{RESET}$ valid with V_{CC} = 1 V
- Superior upgrade for MAX706P/R/S/T, MAX708R/S/T

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Critical microprocessor monitoring
- Battery-operated systems
- Portable instruments

FUNCTIONAL BLOCK DIAGRAMS

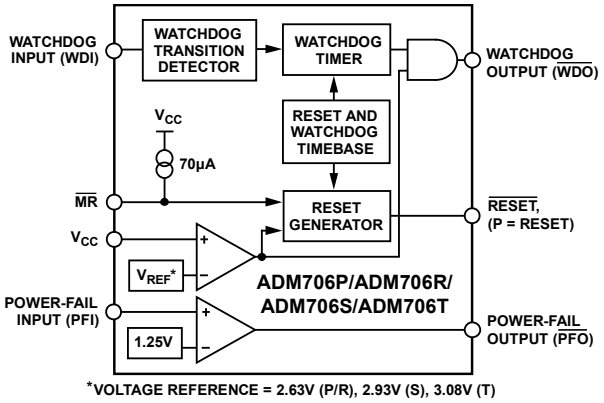


Figure 1. ADM706P/ADM706R/ADM706S/ADM706T

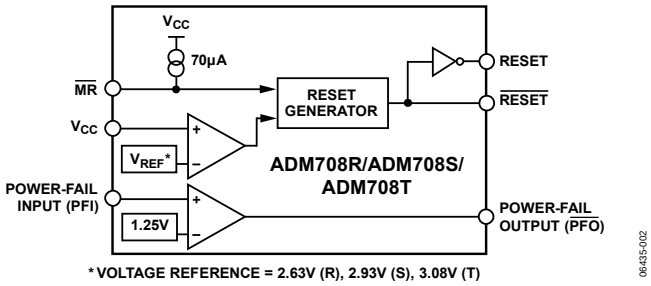


Figure 2. ADM708R/ADM708S/ADM708T

GENERAL DESCRIPTION

The ADM706P/ADM706R/ADM706S/ADM706T and the ADM708R/ADM708S/ADM708T microprocessor supervisory circuits are suitable for monitoring either 3 V or 3.3 V power supplies.

The ADM706P/ADM706R/ADM706S/ADM706T provide power-supply monitoring circuitry that generate a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1 V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.6 seconds.

In addition, there is a 1.25 V threshold detector for power-fail warning, low battery detection, or to monitor an additional power supply. An active low debounced $\overline{MR}$ input is also included.

The ADM706R, ADM706S, and ADM706T are identical except for the reset threshold monitor levels, which are 2.63 V, 2.93 V, and 3.08 V, respectively. The ADM706P is identical to the ADM706R in that the reset threshold is 2.63 V. It differs only in that it has an active high reset output.

The ADM708R/ADM708S/ADM708T provide similar functionality as the ADM706R/ADM706S/ADM706T and only differ in that a watchdog timer function is not available. Instead, an active high reset output (RESET) is provided in addition to the active low ($\overline{RESET}$) output.

All parts are available in narrow 8-lead PDIP and 8-lead SOIC packages.

Rev. C

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REVISION HISTORY

5/08—Rev. B to Rev. C

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2/07—Rev. A to Rev. B

Updated Format ... Universal
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SPECIFICATIONS

V_{CC} = 2.70 V to 5.5 V (ADM706P/ADM70xR), V_{CC} = 3.00 V to 5.5 V (ADM70xS), V_{CC} = 3.15 V to 5.5 V (ADM70xT), $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		100	200	µA	V_{CC} < 3.6 V
		150	350	µA	V_{CC} < 5.5 V
LOGIC OUTPUT					
Reset Threshold (V_{RST})	2.55	2.63	2.70	V	ADM706P/ADM70xR
	2.85	2.93	3.00	V	ADM70xS
	3.00	3.08	3.15	V	ADM70xT
Reset Threshold Hysteresis		20		mV	
RESET PULSE WIDTH	160	200	280	ms	ADM706P/ADM70xR, V_{CC} = 3 V
	160	200	280	ms	ADM70xS/ADM70xT, V_{CC} = 3.3 V
		200		ms	V_{CC} = 5.0 V
$\overline{\text{RESET}}$ OUTPUT VOLTAGE (ADM70xR/ADM70xS/ADM70xT)					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC} − 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
V_{OL}			0.3	V	V_{CC} = 1 V, I_{SINK} = 100 µA
RESET OUTPUT VOLTAGE (ADM706P)					
V_{OH}	V_{CC} − 0.6 V			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 215 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC} − 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
RESET OUTPUT VOLTAGE (ADM708x)					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
V_{OH}	V_{CC} − 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA
WATCHDOG INPUT (ADM706x)					
Watchdog Timeout Period	1.00	1.60	2.25	sec	ADM706P/ADM706R: V_{CC} = 3 V; ADM706S/ADM706T: V_{CC} = 3.3 V; V_{IL} = 0.4 V, V_{IH} = V_{CC} × 0.8 V
WDI Pulse Width	100			ns	V_{RST} (max) < V_{CC} < 3.6 V
	50			ns	4.5 V < V_{CC} < 5.5 V
WDI Input Threshold					
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	V_{CC} = 5.0 V
V_{IH}	3.5			V	V_{CC} = 5.0 V
WDI Input Current	−1.0	+0.02	+1.0	µA	WDI = 0 V or V_{CC}
$\overline{\text{WDO}}$ OUTPUT VOLTAGE					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
	V_{CC} − 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MANUAL RESET INPUT					
$\overline{MR}$ Pull-Up Current ($\overline{MR}$ = 0 V)	25	70	250	µA	V_{RST} (max) < V_{CC} < 3.6 V
	100	250	600	µA	4.5 V < V_{CC} < 5.5 V
$\overline{MR}$ Pulse Width	500			ns	V_{RST} (max) < V_{CC} < 3.6 V
	150			ns	4.5 V < V_{CC} < 5.5 V
$\overline{MR}$ INPUT THRESHOLD					
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	4.5 V < V_{CC} < 5.5 V
V_{IH}	2.0			V	4.5 V < V_{CC} < 5.5 V
$\overline{MR}$ TO RESET OUTPUT DELAY			750	ns	V_{RST} (max) < V_{CC} < 3.6 V
			250	ns	4.5 V < V_{CC} < 5.5 V
POWER-FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	ADM70xP/ADM70xR, V_{CC} = 3 V ADM70xS/ADM70xT, V_{CC} = 3.3 V, PFI falling
PFI Input Current	−25	+0.01	+25	nA	
$\overline{PFO}$ OUTPUT VOLTAGE					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC} − 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
All Other Inputs	−0.3 V to V_{CC} + 0.3 V
Input Current	
V_{CC}	20 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, N-8 (PDIP)	727 mW
θ_{JA} Thermal Impedance	135°C/W
Power Dissipation, R-8 (SOIC)	470 mW
θ_{JA} Thermal Impedance	110°C/W
Operating Temperature Range	
Industrial (Version A)	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	−65°C to +150°C
ESD Rating	>4.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

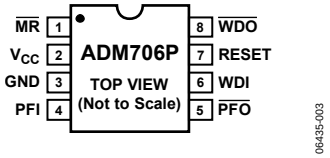


Figure 3. ADM706P

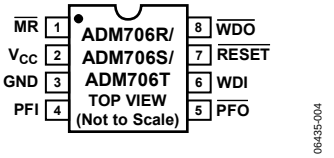


Figure 4. ADM706R/ADM706S/ADM706T

Table 3. Pin Function Descriptions ADM706P/ADM706R/ADM706S/ADM706T

Pin No.	Mnemonic	Description
1	$\overline{MR}$	Manual Reset Input. When taken below 0.6 V, a RESET/$\overline{RESET}$ is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch because it is internally debounced. An internal 70 µA pull-up current holds the input high when floating.
2	V_{CC}	Power Supply Input.
3	GND	Ground. Ground reference for all signals (0 V).
4	PFI	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI should be connected to GND.
5	$\overline{PFO}$	Power-Fail Output. $\overline{PFO}$ is the output from the power-fail comparator. It goes low when PFI is less than 1.25 V.
6	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output, $\overline{WDO}$, goes low. The timer resets with each transition at the WDI input. Either a high-to-low or a low-to-high transition clears the counter. The internal timer is also cleared whenever reset is asserted.
7 (ADM706R/ADM706S/ ADM706T Only)	$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It is triggered either by V_{CC} being below the reset threshold or by a low signal on the $\overline{MR}$ input. $\overline{RESET}$ remains low whenever V_{CC} is below the reset threshold. It remains low for 200 ms after V_{CC} goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
7 (ADM706P Only)	RESET	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$.
8	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low if the internal watchdog timer times out as a result of inactivity on the WDI input. It remains low until the watchdog timer is cleared. $\overline{WDO}$ also goes low during low line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ remains low. As soon as V_{CC} goes above the reset threshold, $\overline{WDO}$ goes high immediately.

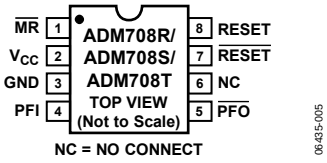


Figure 5. ADM708R/ADM708S/ADM708T

Table 4. Pin Function Descriptions ADM708R/ADM708S/ADM708T

Pin No.	Mnemonic	Description
1	$\overline{MR}$	Manual Reset Input. When taken below 0.6 V, a RESET/$\overline{RESET}$ is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch because it is internally debounced. An internal 70 µA pull-up current holds the input high when floating.
2	V_{CC}	Power Supply Input.
3	GND	Ground. Ground reference for all signals (0 V).
4	PFI	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI should be connected to GND.
5	$\overline{PFO}$	Power-Fail Output. $\overline{PFO}$ is the output from the power-fail comparator. It goes low when PFI is less than 1.25 V.
6	NC	No Connect.
7	$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It is triggered either by V_{CC} being below the reset threshold or by a low signal on the $\overline{MR}$ input. $\overline{RESET}$ remains low whenever V_{CC} is below the reset threshold. It remains low for 200 ms after V_{CC} goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	RESET	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$.

TYPICAL PERFORMANCE CHARACTERISTICS

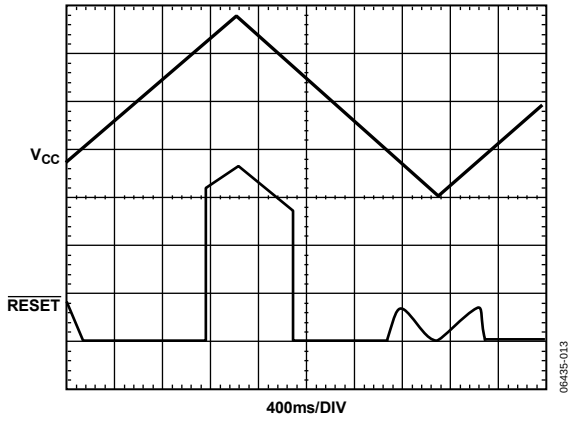


Figure 6. ADM70xR/ADM70xS/ADM70xT $\overline{RESET}$ Output Voltage vs. Supply Voltage

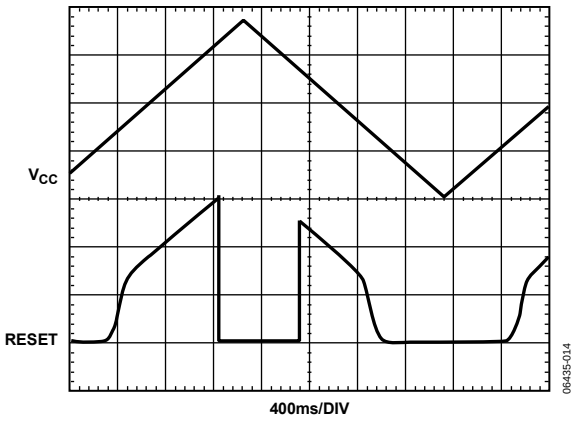


Figure 7. RESET Output Voltage vs. Supply Voltage

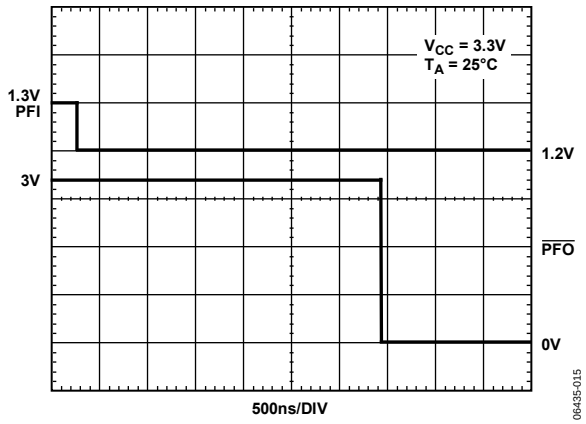


Figure 8. PFI Assertion Response Time

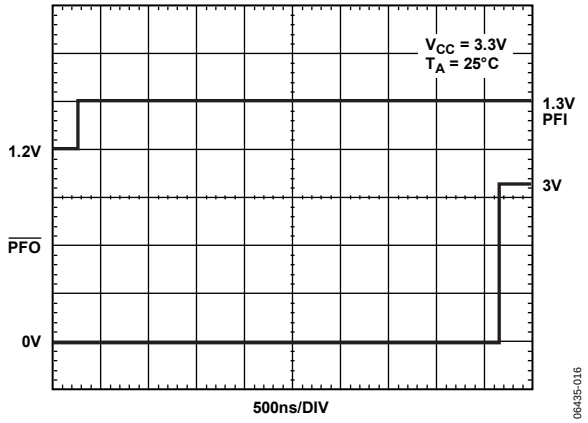


Figure 9. PFI Deassertion Response Time

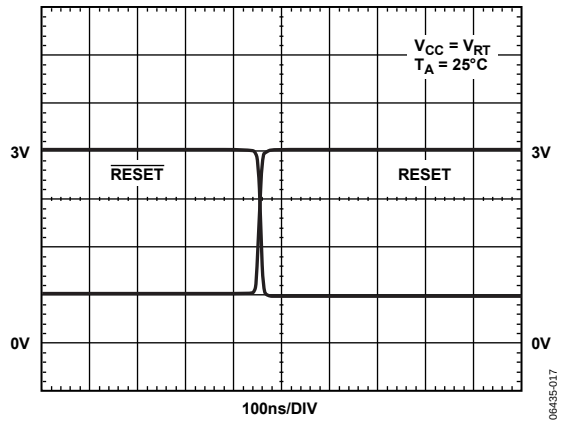


Figure 10. $\overline{RESET}$, RESET Assertion

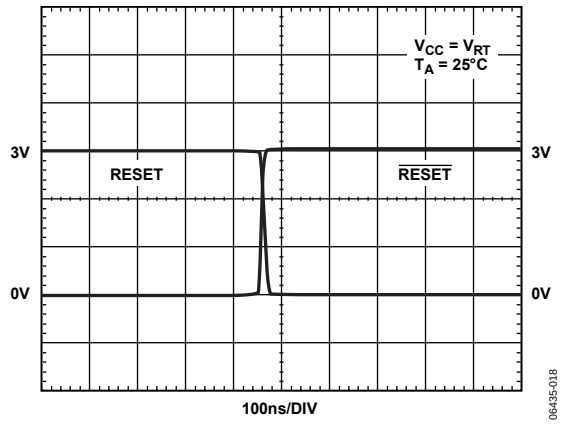


Figure 11. $\overline{RESET}$, RESET Deassertion

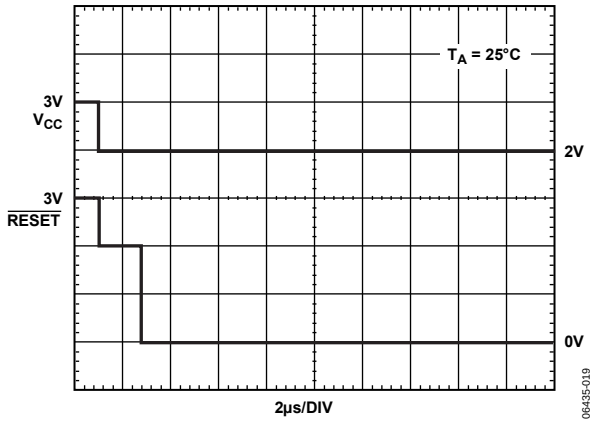


Figure 12. ADM70xR/ADM70xS/ADM70xT $\overline{RESET}$ Response Time

CIRCUIT INFORMATION

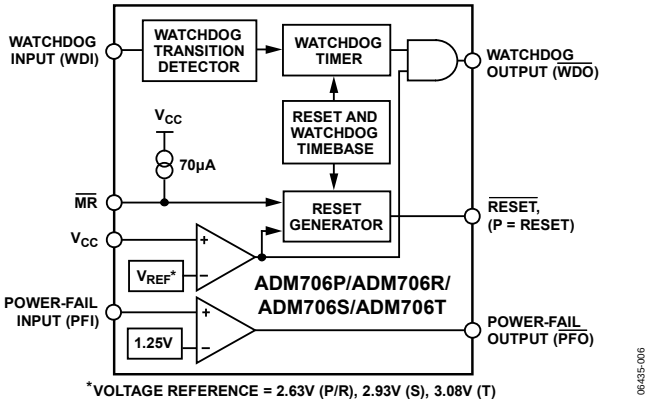


Figure 13. ADM706 Functional Block Diagram

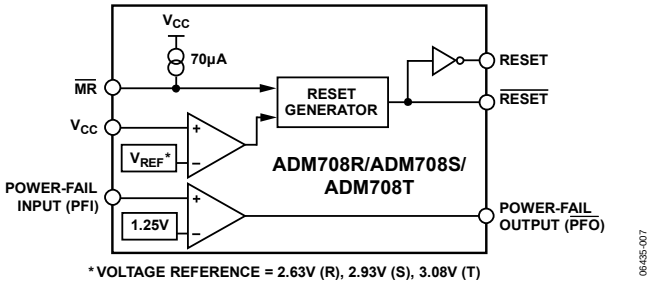


Figure 14. ADM708 Functional Block Diagram

POWER-FAIL RESET

The reset output provides a reset (RESET or $\overline{\text{RESET}}$) output signal to the microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold voltage is dependent on whether a P, R, S, or T suffix device is used. An internal timer holds the reset output active for 200 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset line is similarly activated and remains active for 200 ms after the supply recovers. If another interruption occurs during an active reset period, the reset timeout period continues for an additional 200 ms.

The reset output is guaranteed to remain valid with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply starts up.

The ADM706P provides an active high RESET signal; the ADM706R/ADM706S/ADM706T provide an active low $\overline{\text{RESET}}$ signal; and the ADM708R/ADM706S/ADM706T provide both RESET and $\overline{\text{RESET}}$.

MANUAL RESET

The $\overline{\text{MR}}$ input allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The $\overline{\text{MR}}$ input is TTL-/CMOS-compatible; it can also be driven by any logic reset output. If unused, the $\overline{\text{MR}}$ input can be tied high or left floating.

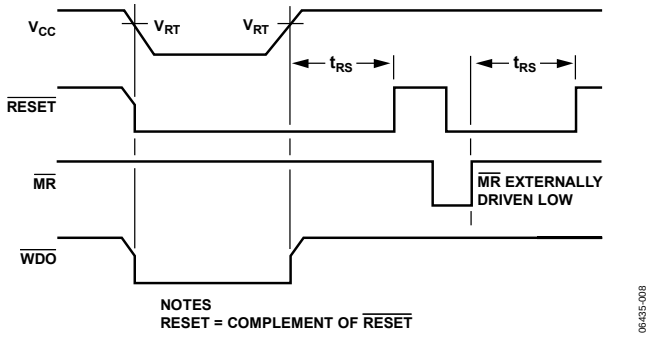


Figure 15. $\overline{\text{RESET}}$, $\overline{\text{MR}}$, and $\overline{\text{WDO}}$ Timing

WATCHDOG TIMER (ADM706x)

The watchdog timer circuit is used to monitor the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.6 seconds), the watchdog output ($\overline{\text{WDO}}$) is driven low. The $\overline{\text{WDO}}$ output is connected to a nonmaskable interrupt (NMI) on the processor. Therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine is used to rectify the problem.

The watchdog timer is cleared either by a high-to-low or by a low-to-high transition on WDI. Pulses as narrow as 50 ns are detected. The timer is also cleared by RESET/$\overline{\text{RESET}}$ going active. Therefore, the watchdog timeout period begins after reset goes inactive.

When V_{CC} falls below the reset threshold, $\overline{\text{WDO}}$ is forced low whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by RESET/$\overline{\text{RESET}}$ going active.

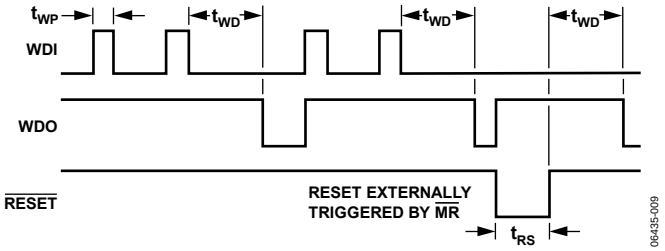


Figure 16. Watchdog Timing

POWER-FAIL COMPARATOR

The power-fail comparator is an independent comparator that can be used to monitor the input power supply. The inverting input of the comparator is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input is used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ($\overline{PFO}$) goes low, indicating a power failure. For early warning of power failure, the comparator is used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The $\overline{PFO}$ output is used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

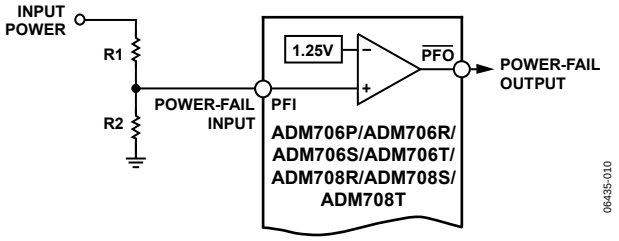


Figure 17. Power-Fail Comparator

ADDING HYSTERESIS TO THE POWER-FAIL COMPARATOR

For increased noise immunity, hysteresis can be added to the power-fail comparator. Because the comparator circuit is noninverting, hysteresis is added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 18. When $\overline{PFO}$ is low, Resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity is achieved by connecting a capacitor between PFI and GND.

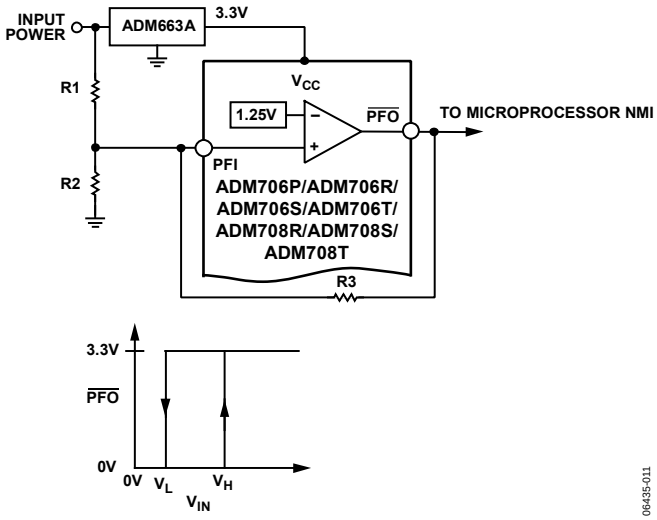


Figure 18. Adding Hysteresis to the Power-Fail Comparator

$$V_H = 1.25\left[1 + \left(\frac{R2 + R3}{R2 \times R3}\right) R1\right]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{R3}\right)$$

$$V_{MID} = 1.25\left(\frac{R1 + R2}{R2}\right)$$

VALID $\overline{RESET}$ BELOW 1 V V_{CC}

The ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T are guaranteed to provide a valid reset level with V_{CC} as low as 1 V. Refer to the Typical Performance Characteristics section. As V_{CC} drops below 1 V, the internal transistor does not have sufficient drive to hold it on so the voltage on $\overline{RESET}$ is no longer held at 0 V. A pull-down resistor, as shown in Figure 19, can be connected externally to hold the line low if it is required.

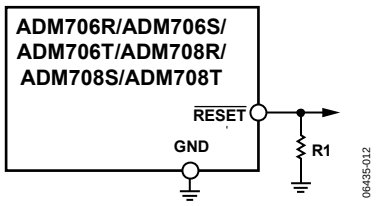


Figure 19. $\overline{RESET}$ Valid Below 1 V

APPLICATIONS INFORMATION

A typical operating circuit is shown in Figure 20. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistor R1 and Resistor R2 are to be selected so that when the supply voltage drops below the desired level (for example, 5 V), the voltage on PFI drops below the 1.25 V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

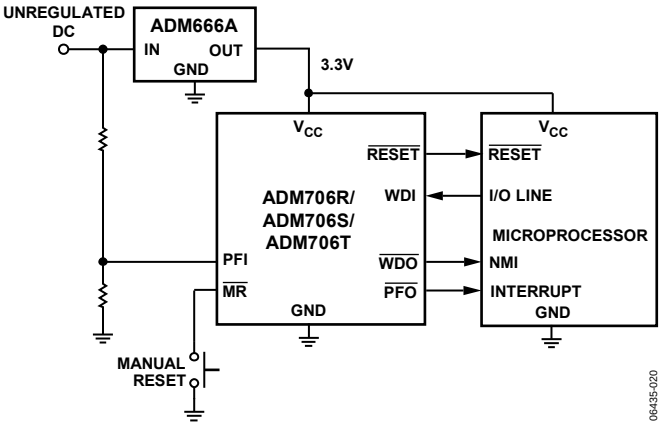


Figure 20. Typical Application Circuit

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines toggle this line at least once every 1.6 seconds. If a problem occurs and this line is not toggled, $\overline{\text{WDO}}$ goes low and a nonmaskable interrupt is generated. This interrupt routine is to be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, the $\overline{\text{WDO}}$ output is to be connected to the input as shown in Figure 21.

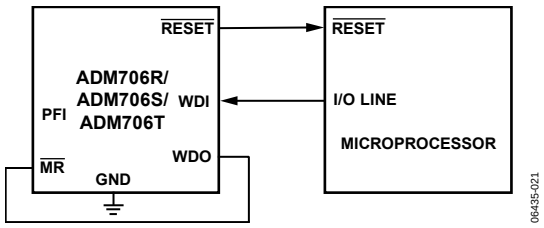


Figure 21. $\overline{\text{RESET}}$ from WDO

MONITORING ADDITIONAL SUPPLY LEVELS

It is possible to use the power-fail comparator to monitor a second supply as shown in Figure 22. The two sensing resistors, R1 and R2, are selected such that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The $\overline{\text{PFO}}$ output can be connected to the $\overline{\text{MR}}$ input so that a reset is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.

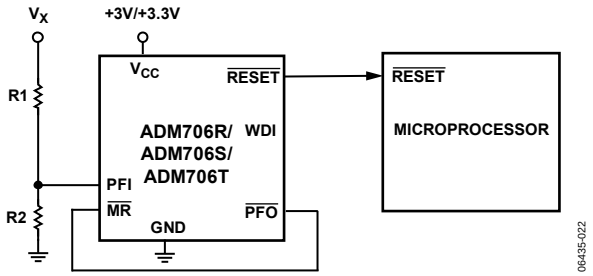


Figure 22. Monitoring 3 V/3.3 V and an Additional Supply, V_X

MICROPROCESSORS WITH BIDIRECTIONAL $\overline{\text{RESET}}$

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor is to be inserted between the ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T $\overline{\text{RESET}}$ output pin and the microprocessor reset pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, it should be buffered as shown in Figure 23.

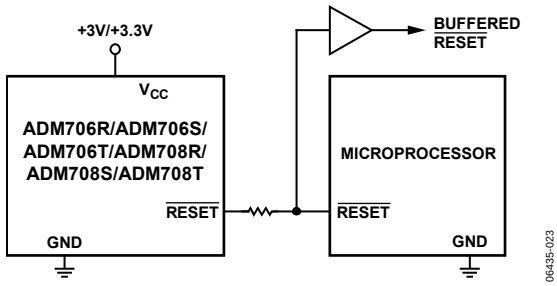
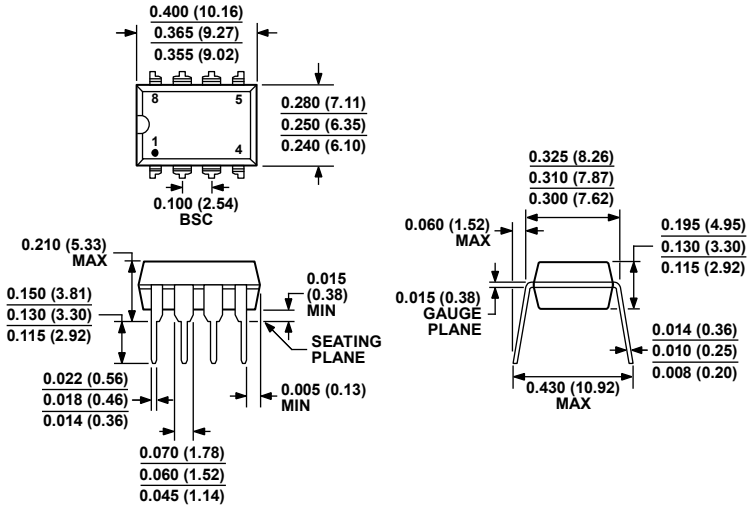


Figure 23. Bidirectional Input/Output $\overline{\text{RESET}}$

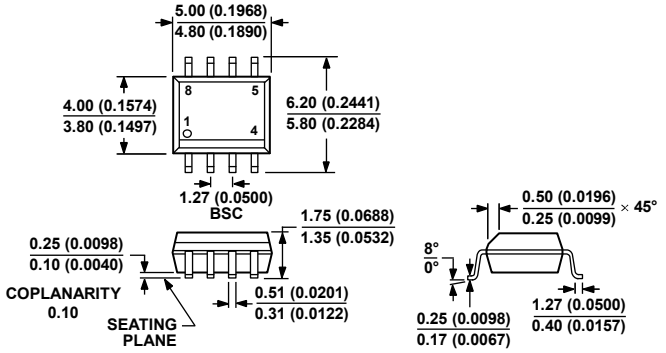
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 24. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimension shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
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012407-A

Figure 25. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM706PAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM706PANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM706PAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM706RANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM706RAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM706SANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM706SAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM706TANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM706TAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM708RANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM708RAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM708SANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM708SAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TAN	−40°C to +85°C	8-Lead PDIP	N-8
ADM708TANZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
ADM708TAR	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TAR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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