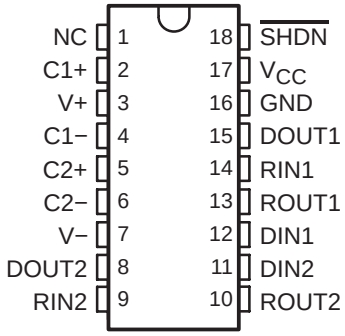
- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V $V_{CC}$ Supply**
- **Operates Up To 200 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 2 μA Typical**
- **External Capacitors . . . 4 × 0.1 μF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description/ordering information

The MAX222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/μs driver output slew rate. By using $\overline{\text{SHDN}}$, all receivers can be disabled.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP (N) | Tube of 20 | MAX222CN | MAX222CN |
| | SOIC (DW) | Tube of 20 | MAX222CDW | MAX222C |
| | | Reel of 1000 | MAX222CDWR | |
| −40°C to 85°C | PDIP (N) | Tube of 20 | MAX222IN | MAX222IN |
| | SOIC (DW) | Tube of 20 | MAX222IDW | MAX222I |
| | | Reel of 1000 | MAX222IDWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004, Texas Instruments Incorporated

### Function Tables

**EACH DRIVER**

| INPUT $D_{IN}$ | OUTPUT $D_{OUT}$ |
|---|---|
| L | H |
| H | L |

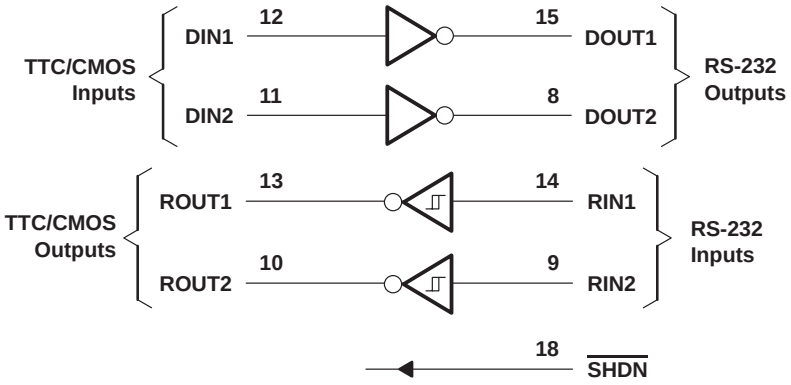
H = high level, L = low level

**EACH RECEIVER**

| INPUT $R_{IN}$ | OUTPUT $R_{OUT}$ |
|---|---|
| L | H |
| H | L |
| Open | H |

H = high level, L = low level, Open = input disconnected or connected driver off

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.3 V to 6 V
Input voltage range, $V_I$: Drivers . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Receivers . . . . . ±30 V
Output voltage range, $V_O$: Drivers . . . . . ±15 V
Receivers . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Short-circuit duration, $D_{OUT}$ . . . . . Continuous
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DW package . . . . . TBD°C/W
N package . . . . . TBD°C/W
Operating virtual junction temperature, $T_J$ . . . . . 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4 and Figure 4)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | Driver high-level input voltage | $D_{IN}$ | 2 | | | V |
| | Shutdown high-level input voltage | $\overline{SHDN}$ | 2 | | | V |
| $V_{IL}$ | Driver low-level input voltage | $D_{IN}$ | | | 0.8 | V |
| | Shutdown low-level input voltage | $\overline{SHDN}$ | | | 0.8 | V |
| $V_I$ | Driver input voltage | $D_{IN}$ | 0 | | 5.5 | V |
| | Receiver input voltage | | −30 | | 30 | |
| $T_A$ | Operating free-air temperature | MAX222C | 0 | | 70 | °C |
| | | MAX222I | −40 | | 85 | |

NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 5 V ± 0.5 V.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | $V_{CC}$ = 5 V | $\overline{SHDN}$ = $V_{CC}$ | No load | | 4 | 10 | mA |
| | | | | 3 kΩ on both inputs | | 15 | | |
| | Shutdown supply current | | | | | 2 | 50 | µA |
| $\overline{SHDN}$ | Shutdown input leakage current | | | | | | ±1 | µA |

NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 5 V ± 0.5 V.

## DRIVER SECTION

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | $D_{IN}$ = GND | 5 | 8 | | V |
| $V_{OL}$ | Low-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | $D_{IN}$ = $V_{CC}$ | −5 | −8 | | V |
| $I_{IH}$ | Driver high-level input current | DIN = $V_{CC}$ | | | 5 | 40 | µA |
| | Control high-level input current | $\overline{SHDN}$ = $V_{CC}$ | | | 0.01 | 1 | |
| $I_{IL}$ | Driver low-level input current | DIN = 0 V | | | −5 | −40 | µA |
| | Control low-level input current | $\overline{SHDN}$ = 0 V | | | −0.01 | −1 | |
| $I_{OS}$‡ | Short-circuit output current | $V_{CC}$ = 5.5 V, | $V_O$ = 0 V | ±7 | ±22 | | mA |
| $I_{off}$ | Output leakage current | $V_{CC}$ = 5.5 V, $\overline{SHDN}$ = GND, | $V_O$ = ±10 V | | ±0.01 | ±10 | µA |
| $r_o$ | Output resistance | $V_{CC}$, V+, and V− = 0 V, | $V_O$ = ±2 V | 300 | 10 M | | Ω |

† All typical values are at $V_{CC}$ = 5 V, and $T_A$ = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 5 V ± 0.5 V.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Data rate | $C_L$ = 1000 pF, One $D_{OUT}$ switching, | $R_L$ = 3 kΩ, See Figure 1 | 200 | | | kbit/s |
| $t_{PLH}$ (D) | Propagation delay time, low- to high-level output | See Figure 1 | | | 1.5 | 3.5 | µs |
| $t_{PHL}$ (D) | Propagation delay time, high- to low-level output | See Figure 1 | | | 1.3 | 3.5 | µs |
| $t_{PHL}$ (D) − $t_{PLH}$ (D) | Driver (+ to −) propagation delay difference | | | | 300 | | ns |
| $t_{sk(p)}$ | Pulse skew§ | $C_L$ = 150 pF to 2500 pF | $R_L$ = 3 kΩ to 7 kΩ, See Figure 2 | | 300 | | ns |
| SR(tr) | Slew rate, transition region (see Figure 1) | $R_L$ = 3 kΩ to 7 kΩ, $V_{CC}$ = 5 V | $C_L$ = 50 pF to 2500 pF | 6 | 12 | 30 | V/µs |
| $t_{ET}$ | Driver output enable time (after $\overline{SHDN}$ goes high) | | | | 250 | | µs |
| $t_{DT}$ | Driver output disable time (after $\overline{SHDN}$ goes low) | | | | 300 | | ns |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 5 V ± 0.5 V.

## RECEIVER SECTION

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −1 mA | 3.5 | $V_{CC}$ − 0.2 V | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 3.2 mA | | | 0.4 | V |
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 5 V | | 1.7 | 2.4 | V |
| $V_{IT−}$ | Negative-going input threshold voltage | $V_{CC}$ = 5 V | 0.8 | 1.3 | | V |
| $V_{hys}$ | Input hysteresis ($V_{IT+} − V_{IT−}$) | | 0.2 | 0.5 | 1 | V |
| $r_i$ | Input resistance | $V_I$ = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

† All typical values are at $V_{CC}$ = 5 V, and $T_A$ = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 5 V ± 0.5 V.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

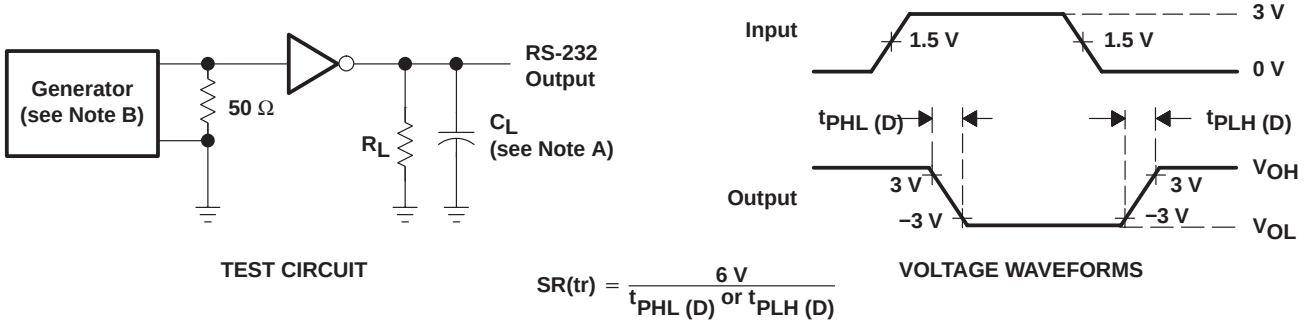
| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ (R) | Propagation delay time, low- to high-level output | $C_L$= 150 pF | | 0.6 | 1 | µs |
| $t_{PHL}$ (R) | Propagation delay time, high- to low-level output | $C_L$= 150 pF | | 0.5 | 1 | µs |
| $t_{PHL}$ (R) − $t_{PLH}$ (R) | Receiver (+ to −) propagation delay difference | | | 100 | | ns |
| $t_{sk(p)}$ | Pulse skew‡ | | | 100 | | ns |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
‡ Pulse skew is defined as $|t_{PLH} − t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF, at $V_{CC}$ = 5 V ± 0.5 V.

### ESD protection

| PIN | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $D_{OUT}$, $R_{IN}$ | Human-Body Model | ±15 | kV |

## PARAMETER MEASUREMENT INFORMATION



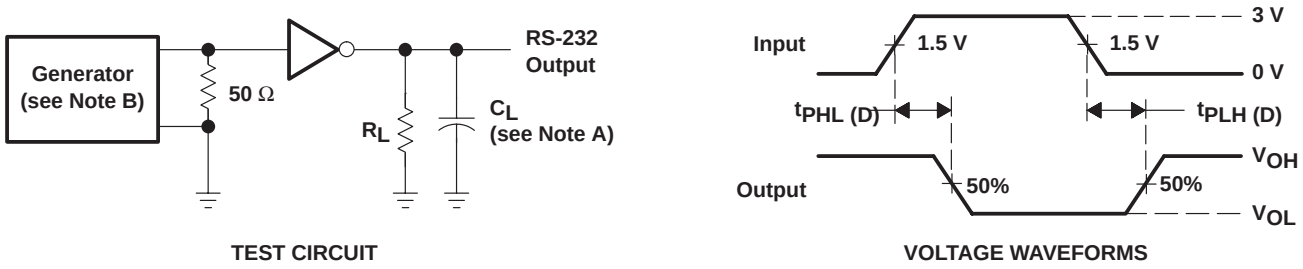

TEST CIRCUIT

VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)} \text{ or } t_{PLH\ (D)}}$$

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 1. Driver Slew Rate**

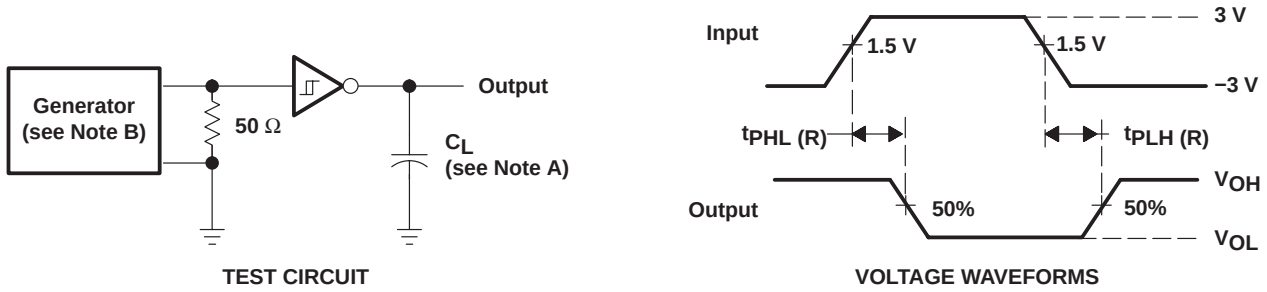



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 2. Driver Pulse Skew**



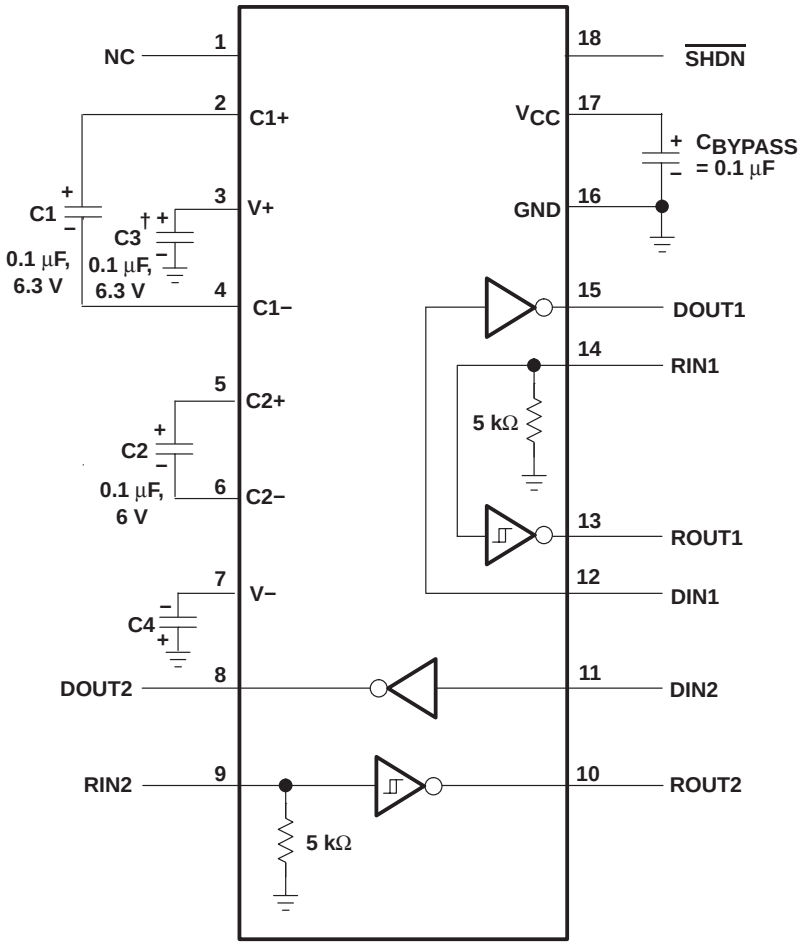

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 3. Receiver Propagation Delay Times**

## APPLICATION INFORMATION




† C3 can be connected to $V_{CC}$ or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 4. Typical Operating Circuit and Capacitor Values**

## APPLICATION INFORMATION

### capacitor selection

The capacitor type used for C1−C4 is not critical for proper operation. The MAX222 requires 0.1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on $V_+$ and $V_-$.

Use larger capacitors (up to 10 µF) to reduce the output impedance at $V_+$ and $V_-$.

Bypass $V_{CC}$ to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple $V_{CC}$ to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

### ESD protection

TI MAX222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

### ESD test conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

### Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-kΩ resistor.

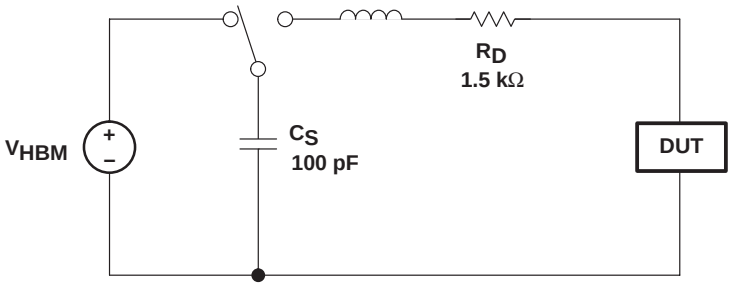



**Figure 5. HBM ESD Test Circuit**

## APPLICATION INFORMATION

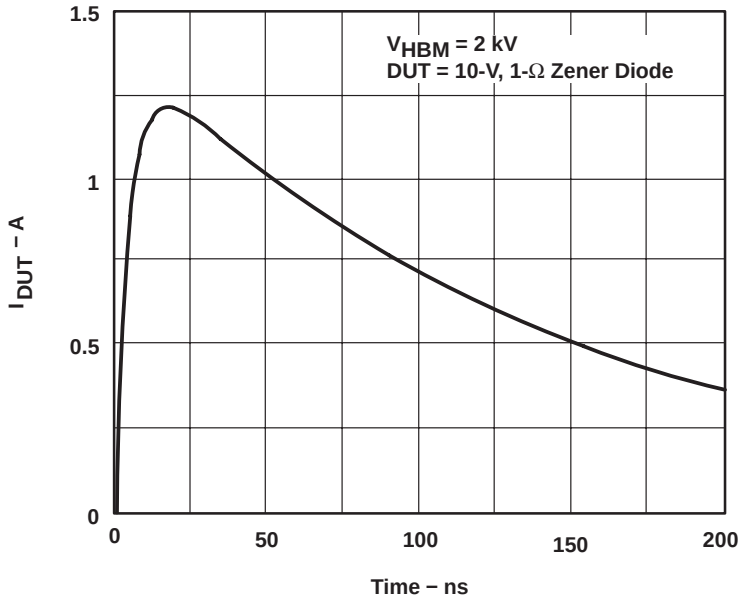



**Figure 6. Typical HBM Current Waveform**

### Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MAX222CDW | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | MAX222C | Samples |
| MAX222CDWG4 | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | MAX222C | Samples |
| MAX222CDWR | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | MAX222C | Samples |
| MAX222CDWRG4 | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | MAX222C | Samples |
| MAX222CN | ACTIVE | PDIP | N | 18 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | MAX222CN | Samples |
| MAX222CNE4 | ACTIVE | PDIP | N | 18 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | MAX222CN | Samples |
| MAX222IDW | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | MAX222I | Samples |
| MAX222IDWG4 | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | MAX222I | Samples |
| MAX222IDWR | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | MAX222I | Samples |
| MAX222IDWRG4 | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | MAX222I | Samples |
| MAX222IN | ACTIVE | PDIP | N | 18 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | MAX222IN | Samples |
| MAX222INE4 | ACTIVE | PDIP | N | 18 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | MAX222IN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

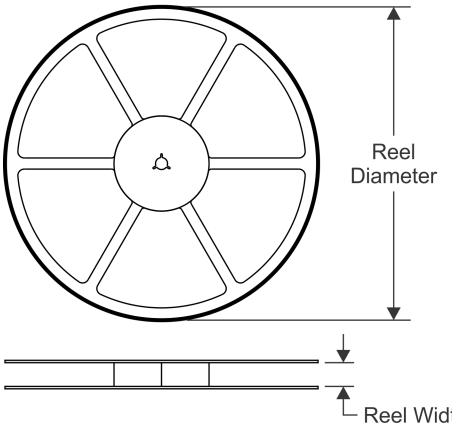
**(4)** Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

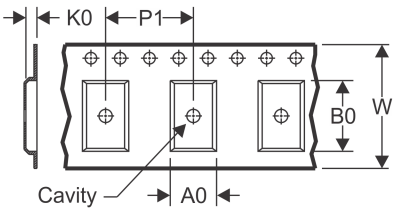
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

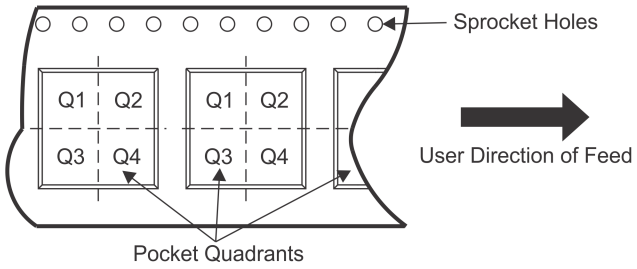



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

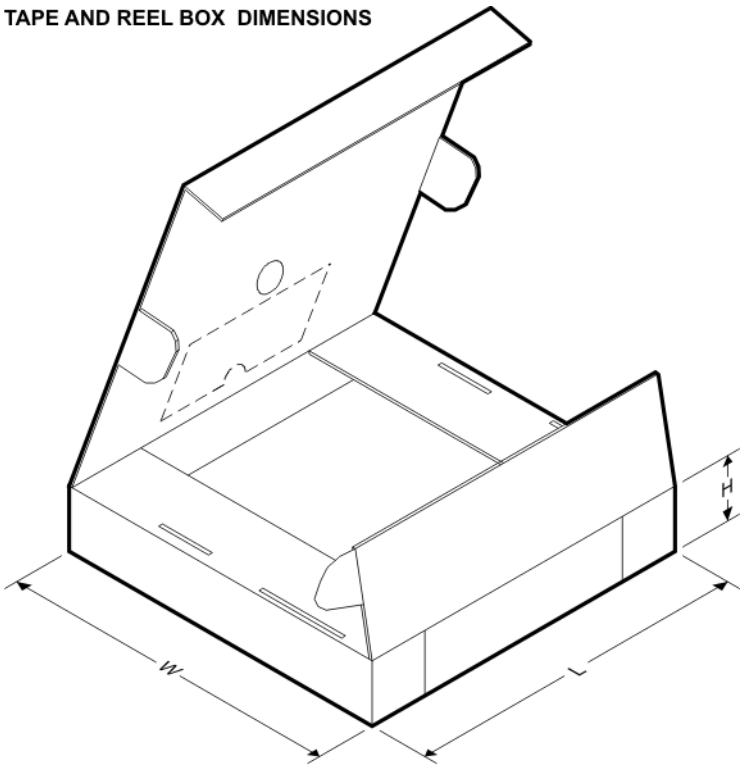
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MAX222CDWR | SOIC | DW | 18 | 2000 | 330.0 | 24.4 | 10.9 | 12.0 | 2.7 | 12.0 | 24.0 | Q1 |
| MAX222IDWR | SOIC | DW | 18 | 2000 | 330.0 | 24.4 | 10.9 | 12.0 | 2.7 | 12.0 | 24.0 | Q1 |

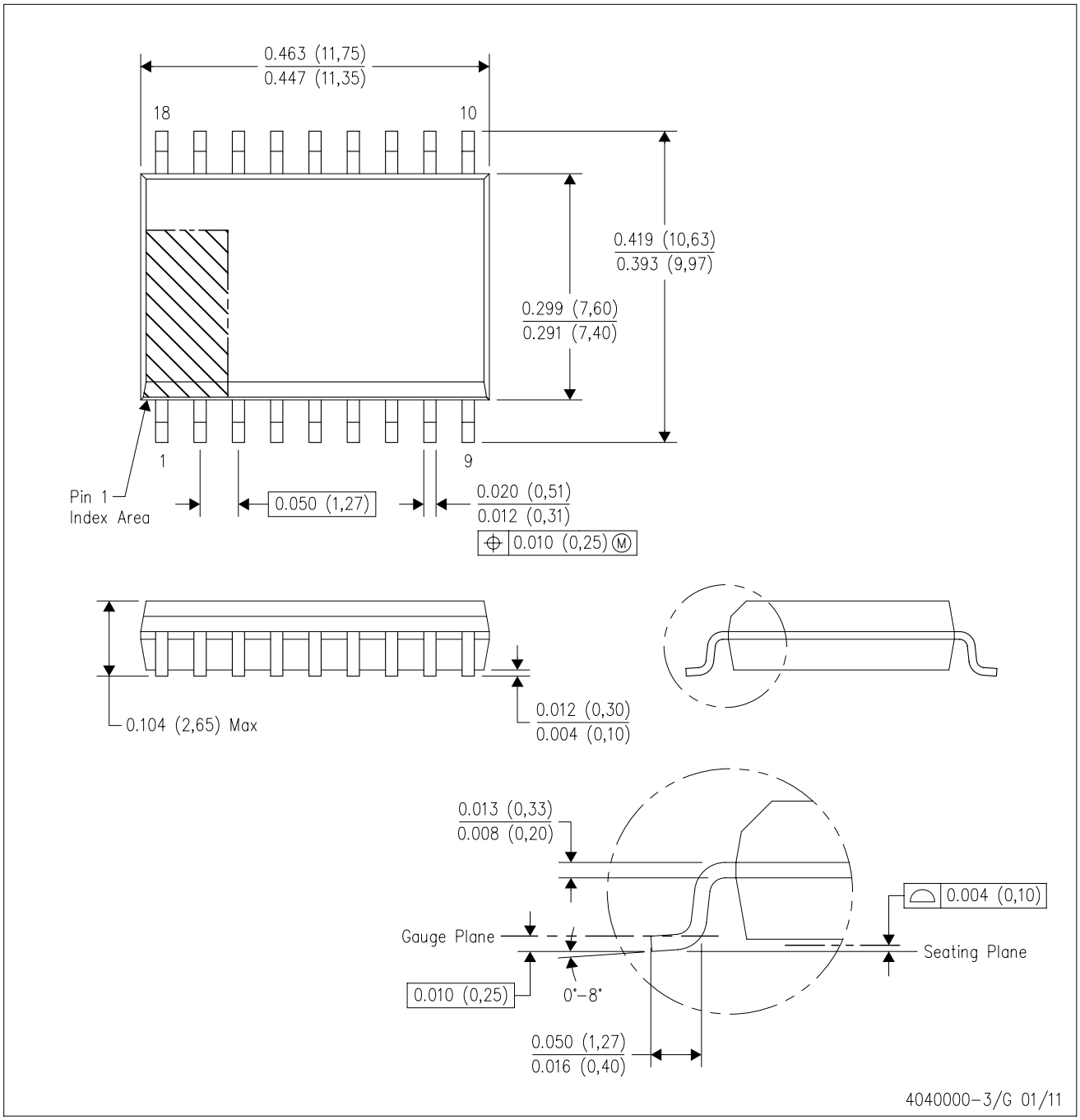
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

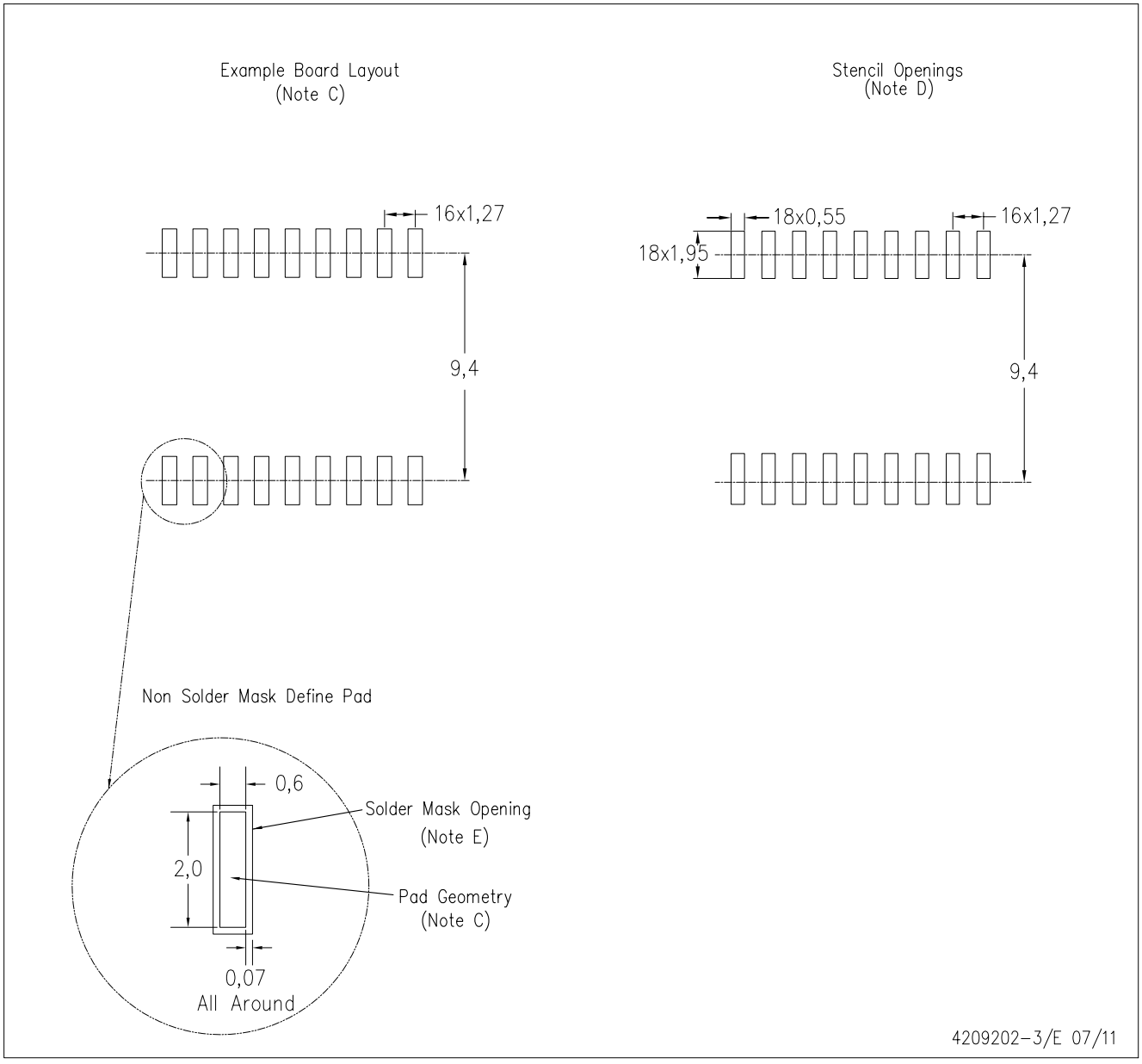
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MAX222CDWR | SOIC | DW | 18 | 2000 | 370.0 | 355.0 | 55.0 |
| MAX222IDWR | SOIC | DW | 18 | 2000 | 370.0 | 355.0 | 55.0 |

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated