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April 1st, 2010
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RENESAS

MOS INTEGRATED CIRCUIT

# μPD720102

## USB 2.0 HOST CONTROLLER

The μPD720102 complies with the universal serial bus specification revision 2.0 and open host controller interface specification for full-/low-speed signaling and Intel's enhanced host controller interface specification for high-speed signaling and works up to 480 Mbps. The μPD720102 is integrated 2 host controller cores with PCI interface and USB 2.0 transceivers into a single chip.

**Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.**
**μPD720102 User's Manual: S17999E**

### FEATURES

- Compliant with universal serial bus specification revision 2.0 (data rate: 1.5/12/480 Mbps)
- Compliant with open host controller interface specification for USB release 1.0a
- Compliant with enhanced host controller interface specification for USB revision 1.0
- PCI multi-function device consists of one OHCI host controller core for full-/low-speed signaling and one EHCI host controller core for high-speed signaling
- Root hub with 3 (Max.) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
- Supports hyper-speed transfer mode using HSMODE signal
- 32-bit 33 MHz host interface compliant with PCI specification revision 2.2
- Supports PCI mobile design guide version 1.1
- Supports PCI-bus power management interface specification revision 1.1
- PCI bus bus-master access
- Supports 3.3 V PCI
- System clock is generated by 30 MHz crystal or 48 MHz clock input
- Operational registers direct-mapped to PCI memory space
- 3.3 V single power supply, 1.5 V internal operating voltage from on chip regulator
- On chip Rs and Rpd resistors for USB signals

### ORDERING INFORMATION

| | Part Number | Package | Remark |
|---|---|---|---|
| | μPD720102GC-YEB-A | 120-pin plastic TQFP (fine pitch) (14 × 14) | Lead-free product |
| <R> | μPD720102F1-CA7-A | 121-pin plastic FBGA (8 × 8) | Lead-free product |

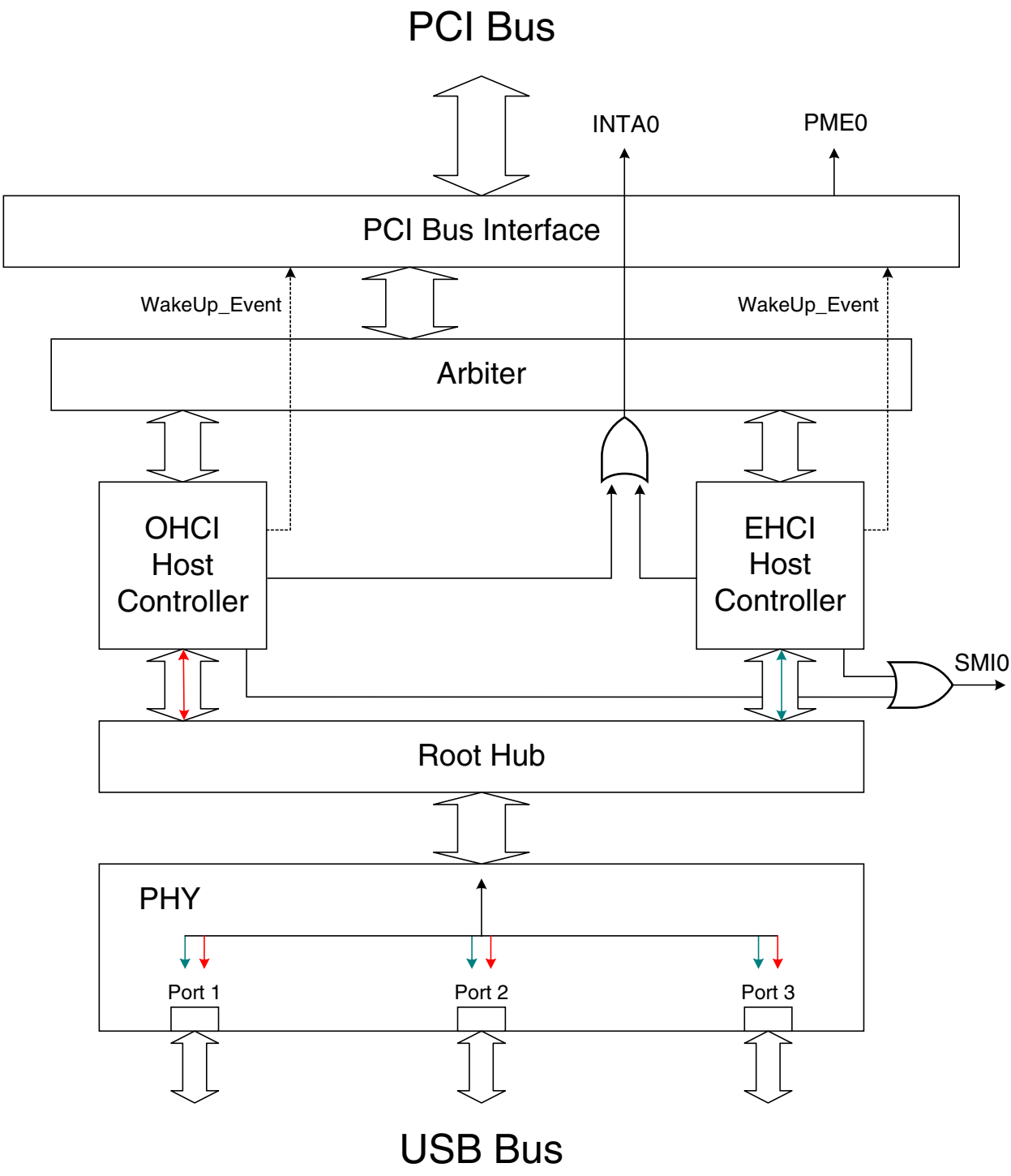
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Date Published March 2007 NS CP (N)
Printed in Japan

**The mark "<R>" shows major revised points.**

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**BLOCK DIAGRAM**

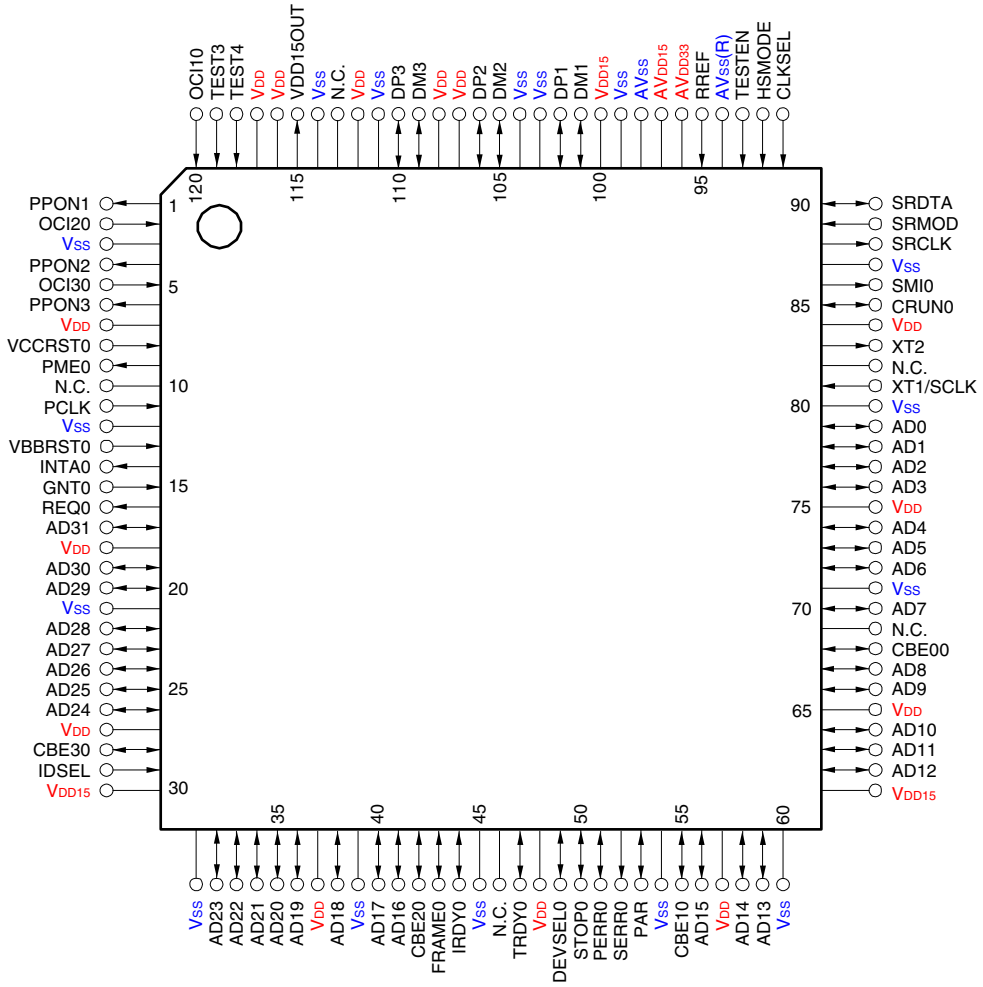


| | | |
|---|---|---|
| PCI Bus Interface | : | handles 32-bit 33 MHz PCI bus master and target function which comply with PCI specification revision 2.2. The number of enabled ports is set by bit in configuration space. |
| Arbiter | : | arbitrates among two OHCI host controller cores and one EHCI host controller core. |
| OHCI Host Controller | : | handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling. |
| EHCI Host Controller | : | handles high- (480 Mbps) signaling. |
| Root Hub | : | handles USB hub function in host controller and controls connection (routing) between host controller core and port. |
| PHY | : | consists of high-speed transceiver, full-/low-speed transceiver, serializer, deserializer, etc. |
| INTA0 | : | is the PCI interrupt signal for OHCI Host Controller. |
| SMI0 | : | is the interrupt signal which is specified by open host controller interface specification for USB release 1.0a and enhanced host controller interface specification revision 1.0. The SMI signal of each OHCI host controller and EHCI host controller appears at this signal. |
| PME0 | : | is the interrupt signal which is specified by PCI-bus power management interface specification revision 1.1. Wakeup signal of each host controller core appears at this signal. |

## PIN CONFIGURATION

- **120-pin plastic TQFP (fine pitch) (14 × 14)**
  μPD720102GC-YEB-A

**Top View**



**Pin Name**

- **120-pin plastic TQFP (fine pitch) (14 × 14)**
  μPD720102GC-YEB-A

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | PPON1 | 31 | $V_{SS}$ | 61 | $V_{DD15}$ | 91 | CLKSEL |
| 2 | OCI20 | 32 | AD23 | 62 | AD12 | 92 | HSMODE |
| 3 | $V_{SS}$ | 33 | AD22 | 63 | AD11 | 93 | TESTEN |
| 4 | PPON2 | 34 | AD21 | 64 | AD10 | 94 | $AV_{SS}$(R) |
| 5 | OCI30 | 35 | AD20 | 65 | $V_{DD}$ | 95 | RREF |
| 6 | PPON3 | 36 | AD19 | 66 | AD9 | 96 | $AV_{DD33}$ |
| 7 | $V_{DD}$ | 37 | $V_{DD}$ | 67 | AD8 | 97 | $AV_{DD15}$ |
| 8 | VCCRST0 | 38 | AD18 | 68 | CBE00 | 98 | $AV_{SS}$ |
| 9 | PME0 | 39 | $V_{SS}$ | 69 | N.C. | 99 | $V_{SS}$ |
| 10 | N.C. | 40 | AD17 | 70 | AD7 | 100 | $V_{DD15}$ |
| 11 | PCLK | 41 | AD16 | 71 | $V_{SS}$ | 101 | DM1 |
| 12 | $V_{SS}$ | 42 | CBE20 | 72 | AD6 | 102 | DP1 |
| 13 | VBBRST0 | 43 | FRAME0 | 73 | AD5 | 103 | $V_{SS}$ |
| 14 | INTA0 | 44 | IRDY0 | 74 | AD4 | 104 | $V_{SS}$ |
| 15 | GNT0 | 45 | $V_{SS}$ | 75 | $V_{DD}$ | 105 | DM2 |
| 16 | REQ0 | 46 | N.C. | 76 | AD3 | 106 | DP2 |
| 17 | AD31 | 47 | TRDY0 | 77 | AD2 | 107 | $V_{DD}$ |
| 18 | $V_{DD}$ | 48 | $V_{DD}$ | 78 | AD1 | 108 | $V_{DD}$ |
| 19 | AD30 | 49 | DEVSEL0 | 79 | AD0 | 109 | DM3 |
| 20 | AD29 | 50 | STOP0 | 80 | $V_{SS}$ | 110 | DP3 |
| 21 | $V_{SS}$ | 51 | PERR0 | 81 | XT1/SCLK | 111 | $V_{SS}$ |
| 22 | AD28 | 52 | SERR0 | 82 | N.C. | 112 | $V_{DD}$ |
| 23 | AD27 | 53 | PAR | 83 | XT2 | 113 | N.C. |
| 24 | AD26 | 54 | $V_{SS}$ | 84 | $V_{DD}$ | 114 | $V_{SS}$ |
| 25 | AD25 | 55 | CBE10 | 85 | CRUN0 | 115 | VDD15OUT |
| 26 | AD24 | 56 | AD15 | 86 | SMI0 | 116 | $V_{DD}$ |
| 27 | $V_{DD}$ | 57 | $V_{DD}$ | 87 | $V_{SS}$ | 117 | $V_{DD}$ |
| 28 | CBE30 | 58 | AD14 | 88 | SRCLK | 118 | TEST4 |
| 29 | IDSEL | 59 | AD13 | 89 | SRMOD | 119 | TEST3 |
| 30 | $V_{DD15}$ | 60 | $V_{SS}$ | 90 | SRDTA | 120 | OCI10 |

**Remark** $AV_{SS}$(R) should be used to connect RREF through 1 % precision reference resistor of 1.6 kΩ.

## <R> PIN CONFIGURATION

- **121-pin plastic FBGA (8 × 8)**
  μPD720102F1-CA7-A

**Bottom View**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 11 |
| 20 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 32 | 10 |
| 19 | 56 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 66 | 33 | 9 |
| 18 | 55 | 84 | 105 | 106 | 107 | 108 | 109 | 92 | 67 | 34 | 8 |
| 17 | 54 | 83 | 104 | 117 | 118 | 119 | 110 | 93 | 68 | 35 | 7 |
| 16 | 53 | 82 | 103 | 116 | 121 | 120 | 111 | 94 | 69 | 36 | 6 |
| 15 | 52 | 81 | 102 | 115 | 114 | 113 | 112 | 95 | 70 | 37 | 5 |
| 14 | 51 | 80 | 101 | 100 | 99 | 98 | 97 | 96 | 71 | 38 | 4 |
| 13 | 50 | 79 | 78 | 77 | 76 | 75 | 74 | 73 | 72 | 39 | 3 |
| 12 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 2 |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 1 |
| L | K | J | H | G | F | E | D | C | B | A | |

<R> **Pin name**

- **121-pin plastic FBGA (8 × 8)**
  μPD720102F1-CA7-A

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | DP3 | 32 | RREF | 63 | $V_{SS}$ | 94 | $V_{DD}$ |
| 2 | PPON1 | 33 | $V_{DD15}$ | 64 | SMI0 | 95 | VDD15OUT |
| 3 | OCI30 | 34 | DM1 | 65 | $AV_{SS}$(R) | 96 | TEST3 |
| 4 | VCCRST0 | 35 | DP1 | 66 | $AV_{DD33}$ | 97 | $V_{DD}$ |
| 5 | PCLK | 36 | $V_{SS}$ | 67 | $V_{SS}$ | 98 | $V_{DD}$ |
| 6 | GNT0 | 37 | DM2 | 68 | $V_{SS}$ | 99 | $V_{DD}$ |
| 7 | AD30 | 38 | DP2 | 69 | $V_{SS}$ | 100 | $V_{DD}$ |
| 8 | AD28 | 39 | $V_{DD}$ | 70 | $V_{SS}$ | 101 | $V_{DD15}$ |
| 9 | AD25 | 40 | DM3 | 71 | $V_{SS}$ | 102 | $V_{DD15}$ |
| 10 | CBE30 | 41 | TEST4 | 72 | $V_{SS}$ | 103 | $V_{SS}$ |
| 11 | $V_{SS}$ | 42 | OCI20 | 73 | OCI10 | 104 | $V_{SS}$ |
| 12 | AD23 | 43 | PPON3 | 74 | PPON2 | 105 | $V_{DD15}$ |
| 13 | AD21 | 44 | PME0 | 75 | VBBRST0 | 106 | $V_{DD15}$ |
| 14 | AD18 | 45 | INTA0 | 76 | AD31 | 107 | $V_{SS}$ |
| 15 | CBE20 | 46 | REQ0 | 77 | AD27 | 108 | $V_{SS}$ |
| 16 | TRDY0 | 47 | AD29 | 78 | IDSEL | 109 | $V_{SS}$ |
| 17 | STOP0 | 48 | AD26 | 79 | $V_{SS}$ | 110 | $AV_{SS}$ |
| 18 | PAR | 49 | AD24 | 80 | AD19 | 111 | $V_{DD}$ |
| 19 | AD14 | 50 | AD22 | 81 | AD16 | 112 | $V_{DD}$ |
| 20 | $V_{SS}$ | 51 | AD20 | 82 | IRDY0 | 113 | $V_{DD}$ |
| 21 | AD12 | 52 | AD17 | 83 | SERR0 | 114 | $V_{SS}$ |
| 22 | AD11 | 53 | FRAME0 | 84 | CBE10 | 115 | $V_{SS}$ |
| 23 | CBE00 | 54 | DEVSEL0 | 85 | AD9 | 116 | $V_{DD}$ |
| 24 | AD6 | 55 | PERR0 | 86 | AD8 | 117 | $V_{DD}$ |
| 25 | AD3 | 56 | AD15 | 87 | AD4 | 118 | $V_{DD}$ |
| 26 | AD1 | 57 | AD13 | 88 | AD0 | 119 | $V_{DD}$ |
| 27 | XT1/SCLK | 58 | AD10 | 89 | CRUN0 | 120 | $V_{DD}$ |
| 28 | XT2 | 59 | AD7 | 90 | SCLK | 121 | $V_{DD}$ |
| 29 | SRMOD | 60 | AD5 | 91 | SRDTA | | |
| 30 | HSMODE | 61 | AD2 | 92 | CLKSEL | | |
| 31 | TESTEN | 62 | $V_{SS}$ | 93 | AVDD15 | | |

**Remark** $AV_{SS}$(R) should be used to connect RREF through 1 % precision reference resistor of 1.6 kΩ.

## 1. PIN INFORMATION

(1/2)

| Pin Name | I/O<br>Normal (Test) | Buffer Type | Active Level | Function |
|---|---|---|---|---|
| AD (31:0) | I/O | 3.3 V PCI I/O with OR input | | PCI “AD [31:0]” signal |
| CBE (3:0)0 | I/O | 3.3 V PCI I/O with OR input | | PCI “C/BE [3:0]” signal |
| PAR | I/O | 3.3 V PCI I/O with OR input | | PCI “PAR” signal |
| FRAME0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “FRAME#” signal |
| IRDY0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “IRDY#” signal |
| TRDY0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “TRDY#” signal |
| STOP0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “STOP#” signal |
| IDSEL | I | 3.3 V PCI input with OR input | High | PCI “IDSEL” signal |
| DEVSEL0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “DEVSEL#” signal |
| REQ0 | O (I/O) | 3.3 V PCI I/O with OR input | Low | PCI “REQ#” signal |
| GNT0 | I | 3.3 V PCI input with OR input | Low | PCI “GNT#” signal |
| PERR0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “PERR#” signal |
| SERR0 | O (I/O) | 3.3 V PCI I/O with OR input Note 1 | Low | PCI “SERR#” signal |
| INTA0 | O (I/O) | 3.3 V PCI I/O with OR input Note 1 | Low | PCI “INTA#” signal |
| PCLK | I | 3.3 V PCI input with OR input | | PCI “CLK” signal |
| VBBRST0 | I | 3.3 V schmitt input | Low | PCI “RST#” signal |
| CRUN0 | I/O | 3.3 V PCI I/O with OR input | Low | PCI “CLKRUN#” signal |
| PME0 | O | N-ch open drain buffer | Low | PCI “PME#” signal |
| VCCRST0 | I | 3.3 V schmitt input | Low | PCI “RST#” signal for $D3_{cold}$ support |
| SMI0 | O (I/O) | 3.3 V I/O buffer | Low | System management interrupt output |
| XT1/SCLK | I | OSC block | | System clock input or oscillator in |
| XT2 | O | OSC block | | Oscillator out |
| CLKSEL | I | 3.3 V Input | | Input clock frequency select signal |
| HSMODE | I | 3.3 V Input | High | Hyper-Speed transfer mode enable signal |
| SRCLK | O (I/O) | 3.3 V I/O buffer | | Serial ROM clock out |
| SRDTA | I/O | 3.3 V I/O buffer | | Serial ROM data |
| SRMOD | I | 3.3 V Input with pull down resistor | High | Serial ROM input enable |
| TESTEN Note 2 | I | 3.3 V Input with pull down resistor | High | Test enable pin |
| TEST3 Note 2 | I | 3.3 V Input with pull down resistor | High | Test control |
| TEST4 Note 2 | I | 3.3 V Input with pull down resistor | High | Test control |

**Notes 1.** These signals become N-ch open drain buffers in normal operation.

**2.** These pins must be open on board.

(2/2)

| Pin Name | I/O<br>Normal (Test) | Buffer Type | Active Level | Function |
|---|---|---|---|---|
| OCI (3:1)0 | I (I/O) | 3.3 V I/O buffer with OR input | Low | USB port's overcurrent status input |
| PPON (3:1) | O (I/O) | 3.3 V I/O buffer | High | USB port's power supply control output |
| DP (3:1) | I/O | USB high speed D+ I/O | | USB high speed D+ signal |
| DM (3:1) | I/O | USB high speed D− I/O | | USB high speed D− signal |
| RREF | A | Analog | | Reference resistor |
| VDD15OUT | O | Internal regulator output | | 1.5 V voltage output from internal regulator |
| $V_{DD15}$ | | | | 1.5 V $V_{DD}$ from VDD15OUT |
| $V_{DD}$ | | | | 3.3 V $V_{DD}$ |
| $AV_{DD15}$ | | | | 1.5 V $V_{DD}$ for analog circuit |
| $AV_{DD33}$ | | | | 3.3 V $V_{DD}$ for analog circuit |
| $V_{SS}$ | | | | $V_{SS}$ |
| $AV_{SS}$ | | | | $V_{SS}$ for analog circuit |
| $AV_{SS}$(R) | | | | $V_{SS}$ for RREF circuit |
| N.C. | | | | No connection |

**Remark** The signal marked as "(I/O)" in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

## 2. HOW TO CONNECT TO EXTERNAL ELEMENTS

### 2.1 Handling Unused Pins

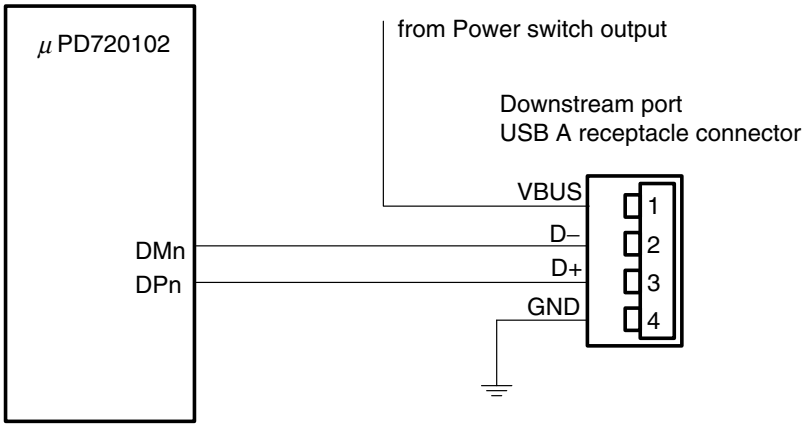
To realize less than 3 ports host controller implementation, appropriate value shall be set to Port No field in EXT1 register. And unused pins shall be connected as shown below.

**Table 2-1. Unused Pin Connection**

| Pin | Direction | Connection Method |
|---|---|---|
| DPx | I/O | No connection (Open) |
| DMx | I/O | No connection (Open) |
| OCIx | I | "H" clamp |
| PPONx | O | No connection (Open) |

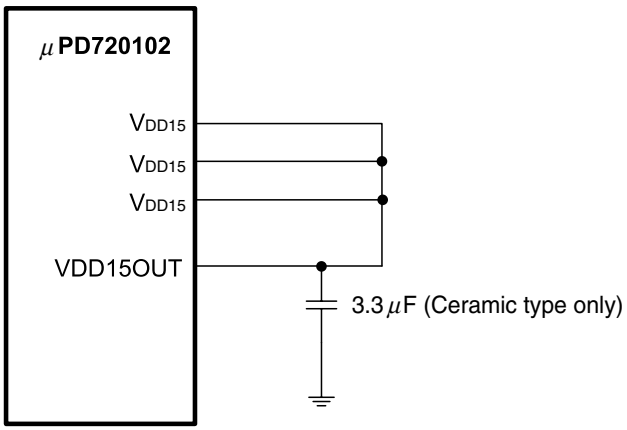
### 2.2 USB Port Connection

**Figure 2–1. USB Downstream Port Connection**



### 2.3 Internal Regulator Circuit Connection

**Figure 2–2. Internal Regulator Circuit Connection**

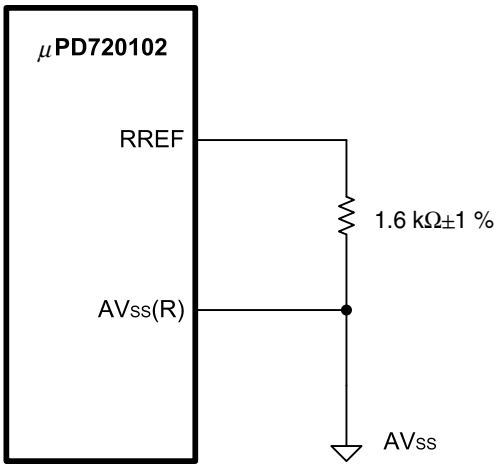



**Caution VDD15OUT must be routed to only $V_{DD15}$ (and $AV_{DD15}$). In case that VDD15OUT is also used for power supply of other ICs, this may cause unstable operation of the μPD720102.**

**Remark** $V_{DD15}$ is powered by VDD15OUT from internal regulator. It is not necessary to use external regulator for $V_{DD15}$.

### 2.4 Analog Circuit Connection

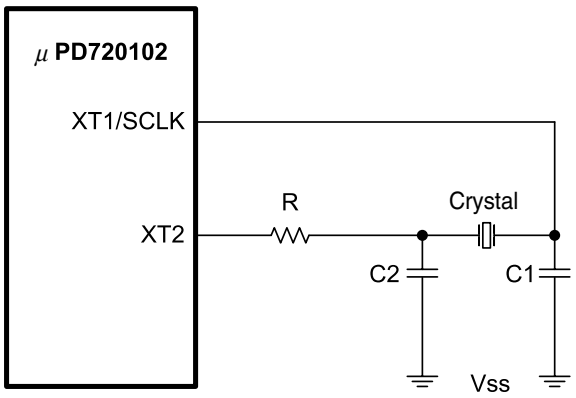
**Figure 2–3. Analog Circuit Connection**




<R> **Remark** The board layout should minimize the total path length from RREF through the resistor to $AV_{SS}$(R) and path length to $AV_{SS}$ (analog ground). $AV_{SS}$ must be stable.

### 2.5 Crystal Connection

**Figure 2–4. Crystal Connection**




The following crystals are evaluated on our reference design board. Table 2-2 shows the external parameters.

**Table 2-2. External Parameters**

| Vender | Crystal | R | C1 | C2 |
|---|---|---|---|---|
| KDS Note 1 | AT-49 30.000 MHz | 100 Ω | 12 pF | 12 pF |
| NDK Note 2 | AT-41 30.000 MHz | 470 Ω | 10 pF | 10 pF |

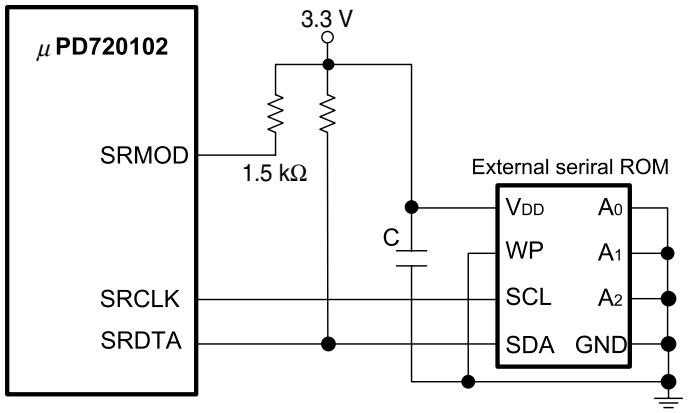
**Notes 1.** DAISHINKU CORP.
**2.** NIHON DEMPA KOGYO CO., LTD.

In using these crystals, contact KDS or NDK to get the specification on external components to be used in conjunction with the crystal.

KDS's home page: http://www.kds.info/english.html
NDK's home page: http://www.ndk.com/

### 2.6 External Serial ROM Connection

**Figure 2–5. External Serial ROM Connection**




The following serial ROM is used on our reference design board.

**Table 2-3. External Parameters**

| Vender | Product name | Size |
|---|---|---|
| Atmel Corporation | AT24C01A-10SC-2.7 | 128 bytes |

SRMOD/SRCLK/SRDTA can be opened, when serial ROM is not necessary on board.

# 3. ELECTRICAL SPECIFICATIONS

## 3.1 Buffer List

- 3.3 V input buffer
  CLKSEL, HSMODE
- 3.3 V input buffer with pull down resistor
  SRMOD, TESTEN, TEST3, TEST4
- 3.3 V input schmitt buffer
  VBBRST0, VCCRST0
- 3.3 V $I_{OL}$ = 9 mA bi-directional buffer
  SMI0, PPON(3:1), SRCLK, SRDTA
- 3.3 V $I_{OL}$ = 9 mA bi-directional buffer with enable (OR type)
  OCI(3:1)0
- 3.3 V PCI input buffer with enable (OR type)
  IDSEL, GNT0, PCLK
- 3.3 V PCI bi-directional buffer with enable (OR type)
  AD(31:0), CBE(3:0)0, PAR, FRAME0, IRDY0, TRDY0, STOP0, DEVSEL0, REQ0, PERR0, SERR0, INTA0, CRUN0
- N-ch open drain buffer
  PME0
- 3.3 V oscillator interface
  XT1/SCLK, XT2
- USB interface, analog signal
  DP(3:1), DM(3:1), RREF

### 3.2 Terminology

#### Terms Used in Absolute Maximum Ratings

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD}$, $V_{DD15}$, $AV_{DD33}$, $AV_{DD15}$ | Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a $V_{DD}$ pin. |
| Input voltage | $V_I$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin. |
| Output voltage | $V_O$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin. |
| Output current | $I_O$ | Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin. |
| Operating ambient temperature | $T_A$ | Indicates the ambient temperature range for normal logic operations. |
| Storage temperature | $T_{stg}$ | Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device. |

#### Terms Used in Recommended Operating Range

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD}$, $AV_{DD33}$ | Indicates the voltage range for normal logic operations occur when $V_{SS}$ = 0 V. |
| High-level input voltage | $V_{IH}$ | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer.<br>* If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage. |
| Low-level input voltage | $V_{IL}$ | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer.<br>* If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage. |
| Hysteresis voltage | $V_H$ | Indicates the differential between the positive and the negative trigger voltage. |
| Input rise time | $t_{ri}$ | Indicates allowable input rise time to input signal transition time from 0.1 x $V_{DD}$ to 0.9 x $V_{DD}$. |
| Input fall time | $t_{fi}$ | Indicates allowable input fall time to input signal transition time from 0.9 x $V_{DD}$ to 0.1 x $V_{DD}$. |

**Terms Used in DC Characteristics**

| Parameter | Symbol | Meaning |
|---|---|---|
| Off-state output leakage current | $I_{OZ}$ | Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance. |
| Input leakage current | $I_I$ | Indicates the current that flows when the input voltage is supplied to the input pin. |
| Low-level output current | $I_{OL}$ | Indicates the current that flows to the output pins when the rated low-level output voltage is being applied. |
| High-level output current | $I_{OH}$ | Indicates the current that flows from the output pins when the rated high-level output voltage is being applied. |

### 3.3 Electrical Specifications

#### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$, $AV_{DD33}$ | | –0.5 to +4.6 | V |
| | $V_{DD15}$, $AV_{DD15}$ | | –0.5 to +2.0 | V |
| Input voltage, 3.3 V buffer | $V_I$ | $V_I < V_{DD} + 0.5$ V | –0.5 to +4.6 | V |
| Output voltage, 3.3 V buffer | $V_O$ | $V_O < V_{DD} + 0.5$ V | –0.5 to +4.6 | V |
| Output current | $I_O$ | 3.3 V buffer ($I_{OL}$ = 9 mA) | 29 | mA |
| | | PCI buffer | 58 | mA |
| Operating ambient temperature | $T_A$ | | –20 to +70 | °C |
| Storage temperature | $T_{stg}$ | | –40 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

#### Recommended Operating Ranges

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$, $AV_{DD33}$ | | 3.135 | 3.3 | 3.465 | V |
| High-level input voltage | $V_{IH}$ | | | | | |
| 3.3 V high-level input voltage | | VBBRST0, VCCRST0 | 2.4 | | $V_{DD}$ | V |
| | | Other input pins | 2.0 | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL}$ | | | | | |
| 3.3 V low-level input voltage | | VBBRST0, VCCRST0 | 0 | | 0.6 | V |
| | | Other input pins | 0 | | 0.8 | V |
| Hysteresis voltage | $V_H$ | | | | | |
| 3.3 V hysteresis voltage | | | 0.3 | | 1.5 | V |
| Input rise time | $t_{ri}$ | | | | | |
| Normal buffer | | | 0 | | 200 | ns |
| Schmitt buffer | | | 0 | | 10 | ms |
| Input fall time | $t_{fi}$ | | | | | |
| Normal buffer | | | 0 | | 200 | ns |
| Schmitt buffer | | | 0 | | 10 | ms |

**DC Characteristics ($V_{DD}$ = 3.135 to 3.465 V, $T_A$ = –20 to +70°C)**

**Control pin block**

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Off-state output current | $I_{OZ}$ | $V_O = V_{DD}$ or $V_{SS}$ | | ±10 | μA |
| Low-level output current<br>3.3 V low-level output current (9 mA) | $I_{OL}$ | $V_{OL}$ = 0.4 V | 9.0 | | mA |
| High-level output current<br>3.3 V high-level output current (9 mA) | $I_{OH}$ | $V_{OH}$ = 2.4 V | –9.0 | | mA |
| Input leakage current<br>3.3 V buffer<br>3.3 V buffer with pull down resistor | $I_I$ | $V_I = V_{DD}$ or $V_{SS}$<br>$V_I = V_{DD}$ | | ±10<br>175 | μA<br>μA |

**PCI interface block**

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | | $0.5V_{DD}$ | $V_{DD}$+0.5 | V |
| Low-level input voltage | $V_{IL}$ | | –0.5 | $0.3V_{DD}$ | V |
| Low-level output current | $I_{OL}$ | $V_{OL} = 0.1V_{DD}$ | 1.5 | | mA |
| High-level output current | $I_{OH}$ | $V_{OH} = 0.9V_{DD}$ | –0.5 | | mA |
| Input leakage current | $I_{il}$ | $0 < V_{IN} < V_{DD}$ | | ±10 | μA |
| PME0 leakage current | $I_{OFF}$ | $V_O$ < 3.6 V<br>$V_{DD}$ off or floating | | 1 | μA |

**USB interface block**

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Output pin impedance | $Z_{HSDRV}$ | | 40.5 | 49.5 | Ω |
| **Input Levels for Low-/full-speed:** | | | | | |
| High-level input voltage (drive) | $V_{IH}$ | | 2.0 | | V |
| High-level input voltage (floating) | $V_{IHZ}$ | | 2.7 | 3.6 | V |
| Low-level input voltage | $V_{IL}$ | | | 0.8 | V |
| Differential input sensitivity | $V_{DI}$ | $\lvert(D+) - (D-)\rvert$ | 0.2 | | V |
| Differential common mode range | $V_{CM}$ | Includes $V_{DI}$ range | 0.8 | 2.5 | V |
| **Output Levels for Low-/full-speed:** | | | | | |
| High-level output voltage | $V_{OH}$ | $R_L$ of 14.25 kΩ to GND | 2.8 | 3.6 | V |
| Low-level output voltage | $V_{OL}$ | $R_L$ of 1.425 kΩ to 3.6 V | 0.0 | 0.3 | V |
| SE1 | $V_{OSE1}$ | | 0.8 | | V |
| Output signal crossover point voltage | $V_{CRS}$ | | 1.3 | 2.0 | V |
| **Input Levels for High-speed:** | | | | | |
| High-speed squelch detection threshold (differential signal) | $V_{HSSQ}$ | | 100 | 150 | mV |
| High-speed disconnect detection threshold (differential signal) | $V_{HSDSC}$ | | 525 | 625 | mV |
| High-speed data signaling common mode voltage range | $V_{HSCM}$ | | −50 | +500 | mV |
| High-speed differential input signaling level | See **Figure 3–2**. | | | | |
| **Output Levels for High-speed:** | | | | | |
| High-speed idle state | $V_{HSOI}$ | | −10 | +10 | mV |
| High-speed data signaling high | $V_{HSOH}$ | | 360 | 440 | mV |
| High-speed data signaling low | $V_{HSOL}$ | | −10 | +10 | mV |
| Chirp J level (differential signal) | $V_{CHIRPJ}$ | | 700 | 1100 | mV |
| Chirp K level (differential signal) | $V_{CHIRPK}$ | | −900 | −500 | mV |

**Figure 3–1. Differential Input Sensitivity Range for Low-/full-speed**

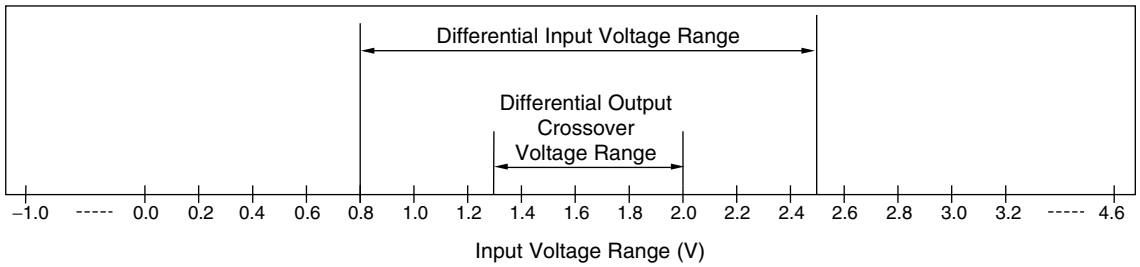



**Figure 3–2. Receiver Sensitivity for Transceiver at DP/DM**

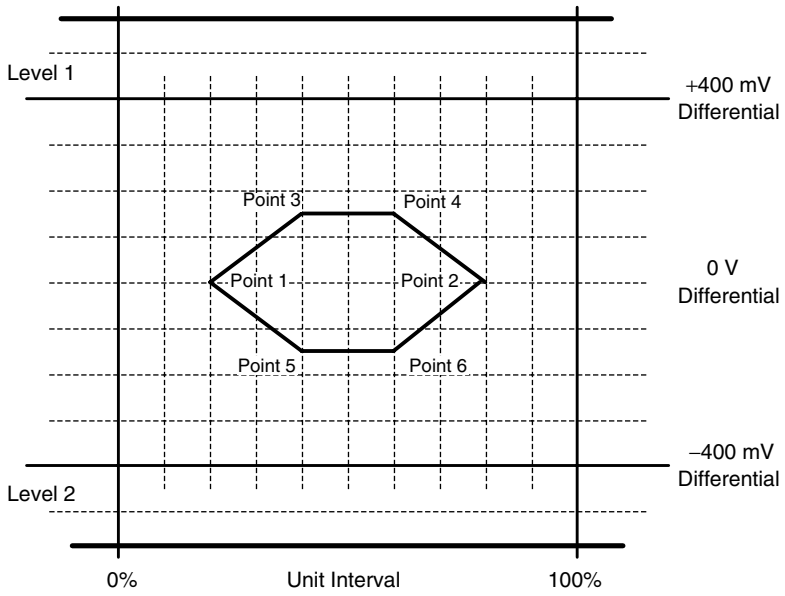
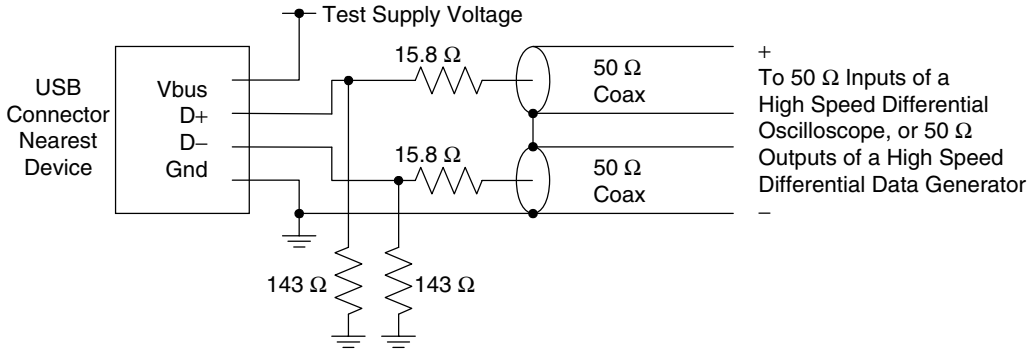



**Figure 3–3. Receiver Measurement Fixtures**



**Power consumption**

| Parameter | Symbol | Condition | With 30 MHz Crystal | | With 48 MHz Oscillator | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Power Consumption | $P_{WD0-0}$ | Device state = D0, All the ports does not connect to any function, and each OHCI controller is under USB suspend and EHCI controller is stopped. Note 1 | 11.0 | 16.0 | 3.0 | 7.0 | mA |
| | $P_{WD0-1}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 1. Note 2 | | | | | |
| | | Full- or low-speed device is on the port. | 15.6 | 22.6 | 7.7 | 13.5 | mA |
| | | High-speed device is on the port. | 60.3 | 70.8 | 60.7 | 71.3 | mA |
| | $P_{WD0-2}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 2. Note 2 | | | | | |
| | | Full- or low-speed devices are on the port. | 17.4 | 31.6 | 9.5 | 22.4 | mA |
| | | High-speed devices are on the port. | 96.1 | 111.8 | 96.6 | 112.4 | mA |
| | $P_{WD0-3}$ | The power consumption under the state without suspend. Device state = D0, The number of active ports is 3. Note 2 | | | | | |
| | | Full- or low-speed devices are on the port. | 18.8 | 40.0 | 10.8 | 31.5 | mA |
| | | High-speed devices are on the port. | 130.7 | 151.8 | 131.2 | 152.2 | mA |
| | $P_{WD0_C}$ | The power consumption under suspend state during PCI clock is stopped by CRUN0. Device state = D0. | 11.0 | 16.0 | 3.0 | 7.0 | mA |
| | $P_{WD1}$ | Device state = D1, Analog PLL output is stopped. Note 3 | 2.1 | 5.9 | 3.0 | 7.0 | mA |
| | $P_{WD2}$ | Device state = D2, Analog PLL output is stopped. Note 3 | 2.1 | 5.9 | 3.0 | 7.0 | mA |
| | $P_{WD3H}$ | Device state = $D3_{hot}$, VCCRST0 = High, Analog PLL output is stopped. Note 3 | 2.1 | 5.9 | 3.0 | 7.0 | mA |
| | $P_{WD3C}$ | Device state = $D3_{cold}$, VCCRST0 = Low. Note 4 | 0.03 | 3.0 | 1.38 | 5.2 | mA |

**Notes 1.** When any device is not connected to all the ports of HC, the power consumption for HC does not depend on the number of active ports.

**2.** The number of active ports is set by the value of Port No Field in PCI configuration space EXT register.

**3.** This is the case when PCI bus state is B0.

**4.** This is the case when PCI bus state is B3.

**Remark** These are estimated value on Windows™ XP environment.

**Pin capacitance**

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_I$ | $V_{DD}$ = 0 V, $T_A$ = 25°C | | 8 | pF |
| Output capacitance | $C_O$ | $f_C$ = 1 MHz | | 8 | pF |
| I/O capacitance | $C_{IO}$ | Unmeasured pins returned to 0 V | | 8 | pF |
| PCI input pin capacitance | $C_{in}$ | | | 8 | pF |
| PCI clock input pin capacitance | $C_{clk}$ | | | 8 | pF |
| PCI IDSEL input pin capacitance | $C_{IDSEL}$ | | | 8 | pF |

**AC Characteristics ($V_{DD}$ = 3.135 to 3.465 V, $T_A$ = –20 to +70°C)**

**System clock ratings**

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | $f_{CLK}$ | Crystal | –500 ppm | 30 | +500 ppm | MHz |
| | | Oscillator block | –500 ppm | 48 | +500 ppm | MHz |
| Clock duty cycle | $t_{DUTY}$ | | 40 | 50 | 60 | % |

**Remarks 1.** Recommended accuracy of clock frequency is ± 100 ppm.

**2.** Required accuracy of crystal or oscillator block is including initial frequency accuracy, the spread of crystal capacitor loading, supply voltage, temperature, and aging, etc.

**PCI interface block**

| | Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| <R> | PCI clock cycle time | $t_{cyc}$ | | 30 | 33 | ns |
| | PCI clock pulse, high-level width | $t_{high}$ | | 11 | | ns |
| | PCI clock pulse, low-level width | $t_{low}$ | | 11 | | ns |
| | PCI clock, rise slew rate | $S_{cr}$ | 0.2$V_{DD}$ to 0.6$V_{DD}$ | 1 | 4 | V/ns |
| | PCI clock, fall slew rate | $S_{cf}$ | 0.2$V_{DD}$ to 0.6$V_{DD}$ | 1 | 4 | V/ns |
| | PCI reset active time (vs. power supply stability) | $t_{rst}$ | | 1 | | ms |
| | PCI reset active time (vs. CLK start) | $t_{rst-clk}$ | | 100 | | μs |
| | Output float delay time (vs. RST0↓) | $t_{rst-off}$ | | | 40 | ns |
| | PCI reset rise slew rate | $S_{rr}$ | | 50 | | mV/ns |
| | PCI bus signal output time (vs. PCLK↑) | $t_{val}$ | | 2 | 11 | ns |
| | PCI point-to-point signal output time (vs. PCLK↑) | $t_{val}$ (ptp) | REQ0 | 2 | 12 | ns |
| | Output delay time (vs. PCLK↑) | $t_{on}$ | | 2 | | ns |
| | Output float delay time (vs. PCLK↑) | $t_{off}$ | | | 28 | ns |
| | Input setup time (vs. PCLK↑) | $t_{su}$ | | 7 | | ns |
| | Point-to-point input setup time (vs. PCLK↑) | $t_{su}$ (ptp) | GNT0 | 10 | | ns |
| | Input hold time | $t_h$ | | 0 | | ns |

**USB interface block**

(1/2)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **Low-speed Source Electrical Characteristics** | | | | | |
| Rise time (10 to 90%) | $t_{LR}$ | $C_L$ = 200 to 600 pF, $R_S$ = 36 Ω | 75 | 300 | ns |
| Fall time (90 to 10%) | $t_{LF}$ | $C_L$ = 200 to 600 pF, $R_S$ = 36 Ω | 75 | 300 | ns |
| Differential rise and fall time matching | $t_{LRFM}$ | ($t_{LR}/t_{LF}$) | 80 | 125 | % |
| Low-speed data rate | $t_{LDRATHS}$ | Average bit rate | 1.49925 | 1.50075 | Mbps |
| Source jitter total (including frequency tolerance): | | | | | |
| To next transition | $t_{DDJ1}$ | | −25 | +25 | ns |
| For paired transitions | $t_{DDJ2}$ | | −14 | +14 | ns |
| Source jitter for differential transition to SE0 transition | $t_{LDEOP}$ | | −40 | +100 | ns |
| Receiver jitter: | | | | | |
| To next transition | $t_{UJR1}$ | | −152 | +152 | ns |
| For paired transitions | $t_{UJR2}$ | | −200 | +200 | ns |
| Source SE0 interval of EOP | $t_{LEOPT}$ | | 1.25 | 1.50 | μs |
| Receiver SE0 interval of EOP | $t_{LEOPR}$ | | 670 | | ns |
| Width of SE0 interval during differential transition | $t_{FST}$ | | | 210 | ns |
| **Full-speed Source Electrical Characteristics** | | | | | |
| Rise time (10 to 90%) | $t_{FR}$ | $C_L$ = 50 pF | 4 | 20 | ns |
| Fall time (90 to 10%) | $t_{FF}$ | $C_L$ = 50 pF | 4 | 20 | ns |
| Differential rise and fall time matching | $t_{FRFM}$ | ($t_{FR}/t_{FF}$) | 90 | 111.11 | % |
| Full-speed data rate | $t_{FDRATHS}$ | Average bit rate | 11.9940 | 12.0060 | Mbps |
| Frame interval | $t_{FRAME}$ | | 0.9995 | 1.0005 | ms |
| Consecutive frame interval jitter | $t_{RFI}$ | No clock adjustment | | 42 | ns |
| Source jitter total (including frequency tolerance): | | | | | |
| To next transition | $t_{DJ1}$ | | −3.5 | +3.5 | ns |
| For paired transitions | $t_{DJ2}$ | | −4.0 | +4.0 | ns |
| Source jitter for differential transition to SE0 transition | $t_{FDEOP}$ | | −2 | +5 | ns |
| Receiver jitter: | | | | | |
| To next transition | $t_{JR1}$ | | −18.5 | +18.5 | ns |
| For paired transitions | $t_{JR2}$ | | −9 | +9 | ns |
| Source SE0 interval of EOP | $t_{FEOPT}$ | | 160 | 175 | ns |
| Receiver SE0 interval of EOP | $t_{FEOPR}$ | | 82 | | ns |
| Width of SE0 interval during differential transition | $t_{FST}$ | | | 14 | ns |

(2/2)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **High-speed Source Electrical Characteristics** | | | | | |
| Rise time (10 to 90%) | $t_{HSR}$ | | 500 | | ps |
| Fall time (90 to 10%) | $t_{HSF}$ | | 500 | | ps |
| Driver waveform | See **Figure 3–4**. | | | | |
| High-speed data rate | $t_{HSDRAT}$ | | 479.760 | 480.240 | Mbps |
| Microframe interval | $t_{HSFRAM}$ | | 124.9375 | 125.0625 | μs |
| Consecutive microframe interval difference | $t_{HSRFI}$ | | | 4 high-speed | Bit times |
| Data source jitter | See **Figure 3–4**. | | | | |
| Receiver jitter tolerance | See **Figure 3–2**. | | | | |
| **Hub Event Timings** | | | | | |
| Time to detect a downstream facing port connect event | $t_{DCNN}$ | | 2.5 | 2000 | μs |
| Time to detect a disconnect event at a hub's downstream facing port | $t_{DDIS}$ | | 2.0 | 2.5 | μs |
| Duration of driving resume to a downstream port | $t_{DRSMDN}$ | Nominal | 20 | | ms |
| Time from detecting downstream resume to rebroadcast | $t_{URSM}$ | | | 1.0 | ms |
| Inter-packet delay for packets traveling in same direction for high-speed | $t_{HSIPDSD}$ | | 88 | | Bit times |
| Inter-packet delay for packets traveling in opposite direction for high-speed | $t_{HSIPDOD}$ | | 8 | | Bit times |
| Inter-packet delay for root hub response for high-speed | $t_{HSRSPIPD1}$ | | | 192 | Bit times |
| Time for which a Chirp J or Chirp K must be continuously detected during reset handshake | $t_{FILT}$ | | 2.5 | | μs |
| Time after end of device Chirp K by which hub must start driving first Chirp K | $t_{WTDCH}$ | | | 100 | μs |
| Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream during reset | $t_{DCHBIT}$ | | 40 | 60 | μs |
| Time before end of reset by which a hub must end its downstream chirp sequence | $t_{DCHSE0}$ | | 100 | 500 | μs |

**Figure 3–4. Transmit Waveform for Transceiver at DP/DM**

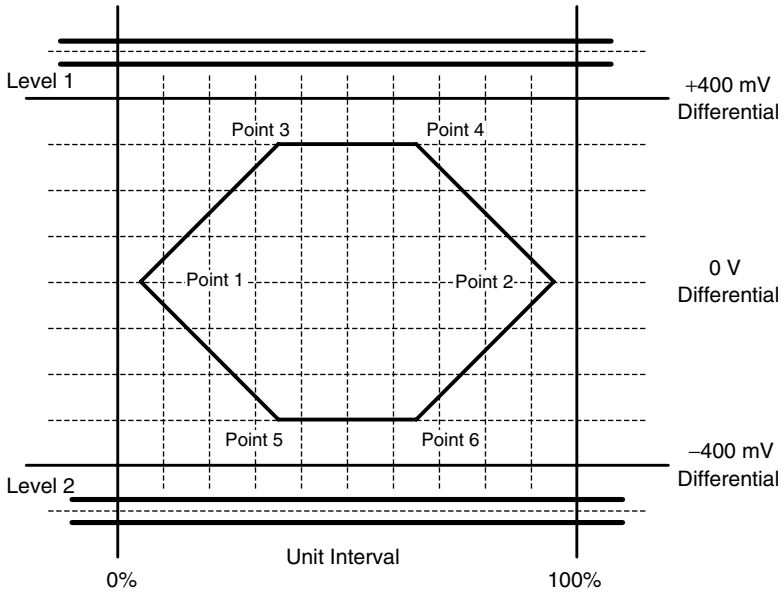
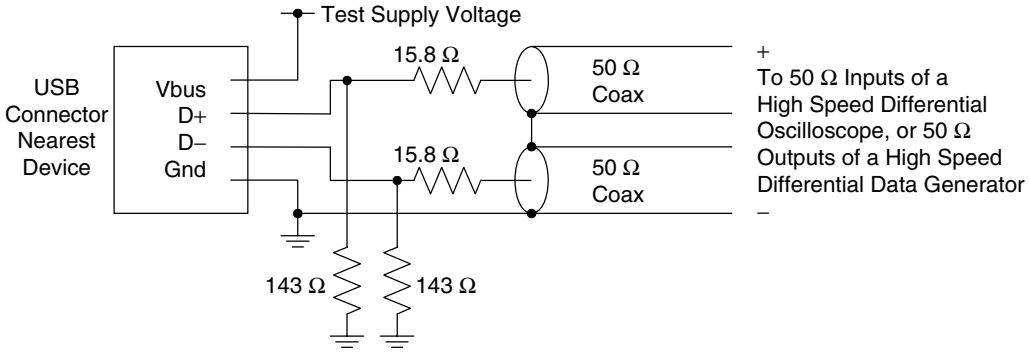
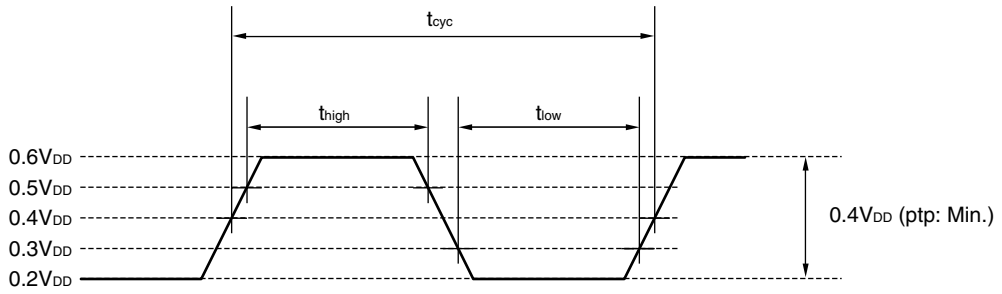



**Figure 3–5. Transmitter Measurement Fixtures**

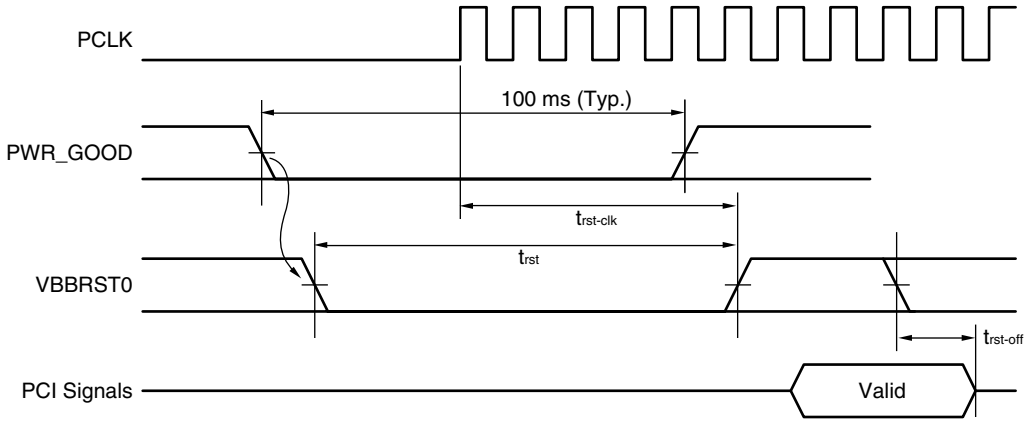


### 3.4 Timing Diagram

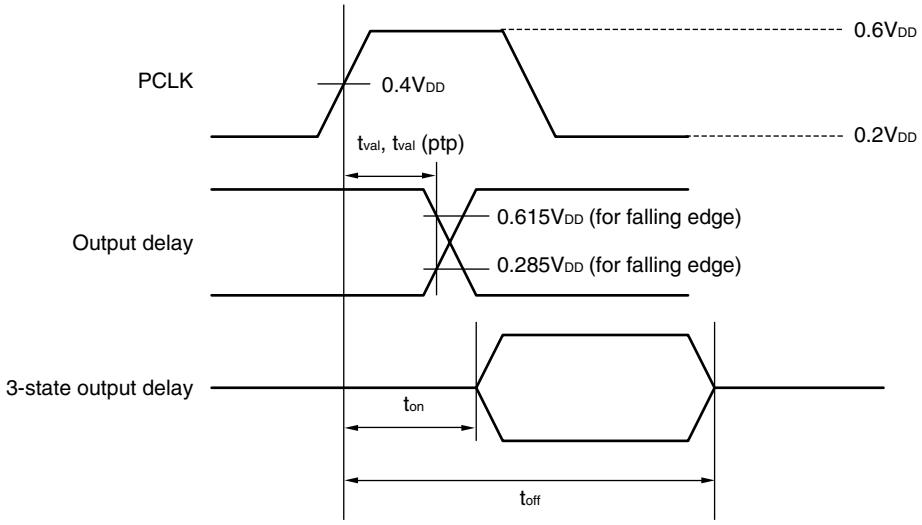
**PCI clock**



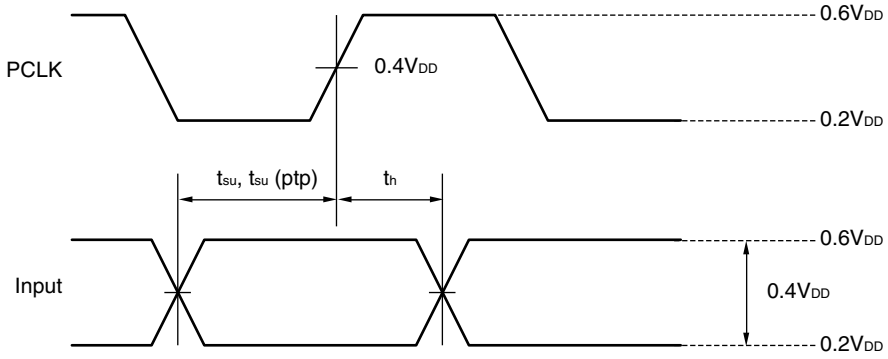

**PCI reset**



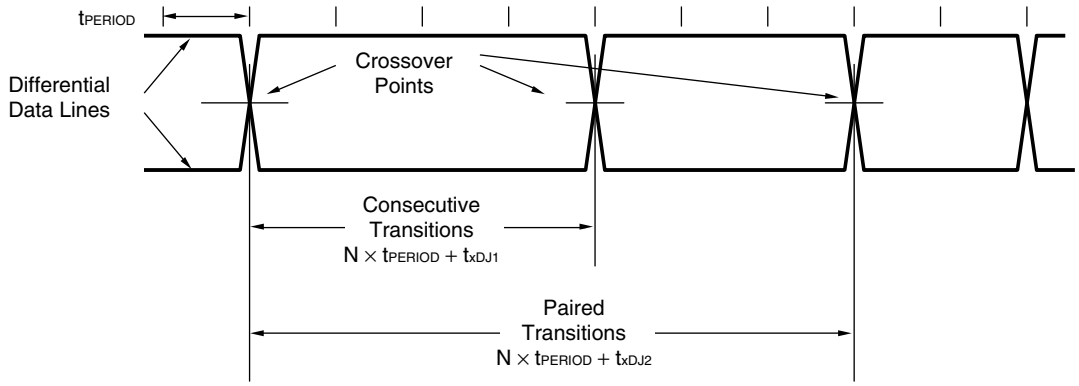
**PCI output timing measurement condition**



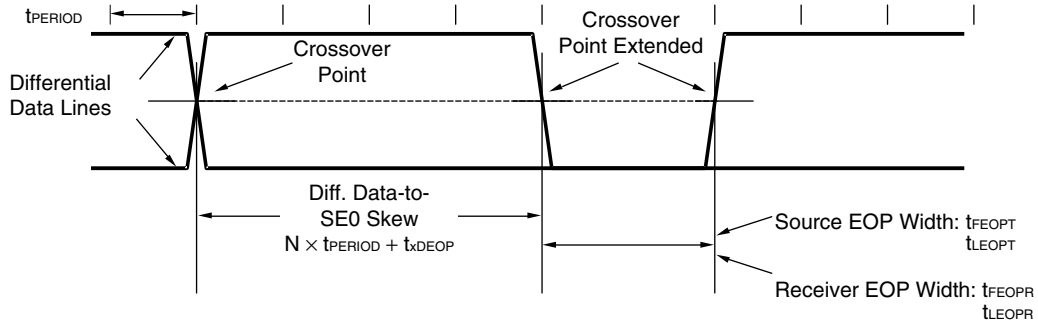

**PCI input timing measurement condition**



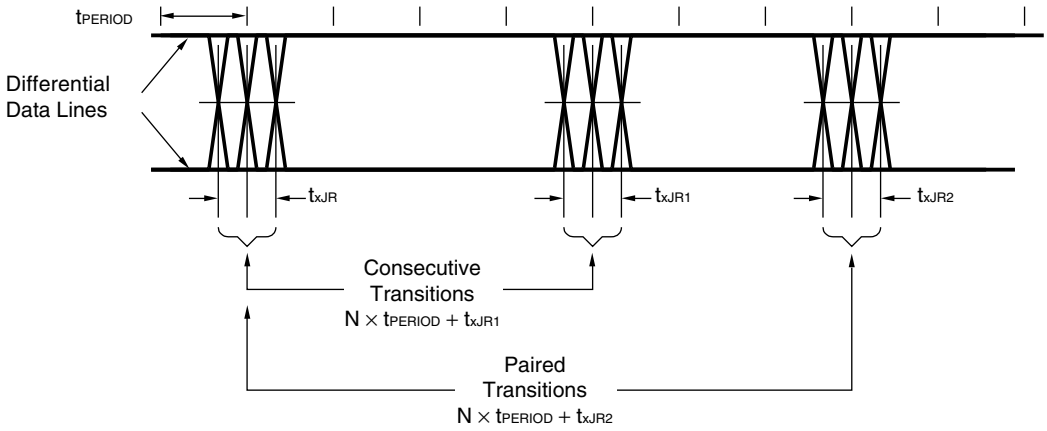
**USB differential data jitter for full-speed**



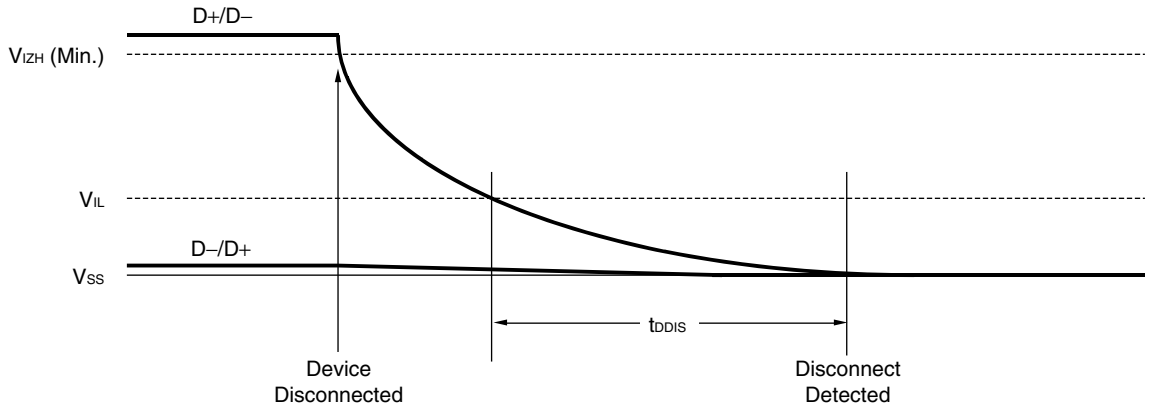

**USB differential-to-EOP transition skew and EOP width for low-/full-speed**



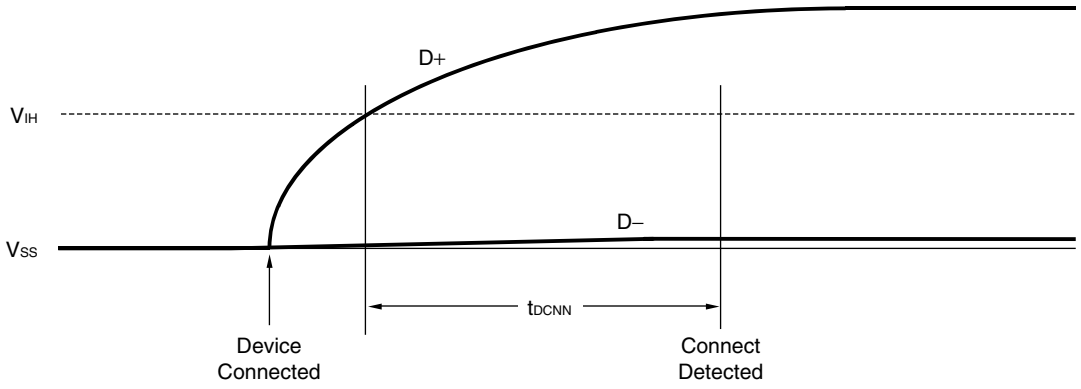

**USB receiver jitter tolerance for low-/full-speed**



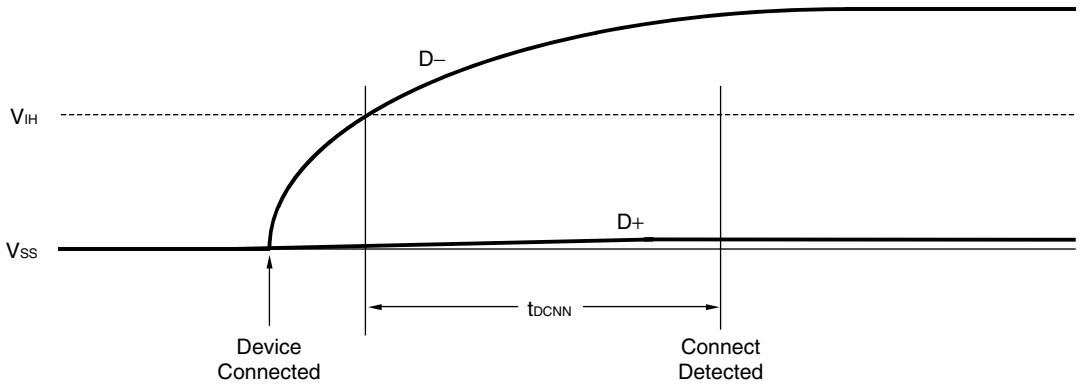
**Low-/full-speed disconnect detection**




**Full-/high-speed device connect detection**



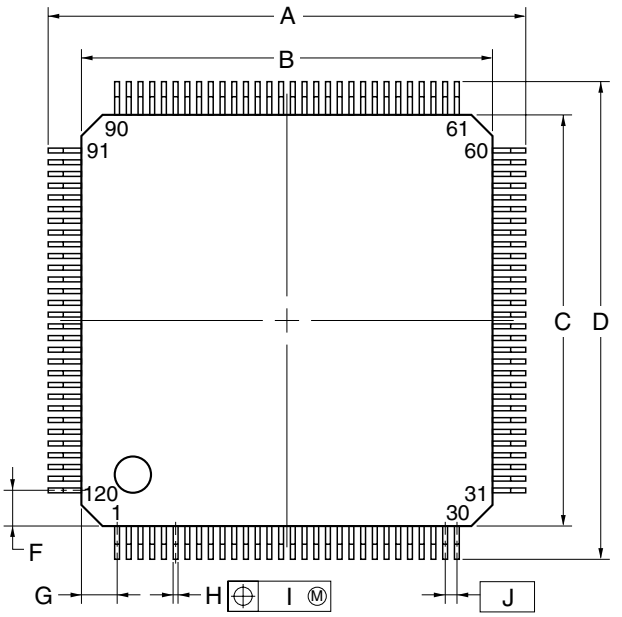

**Low-speed device connect detection**

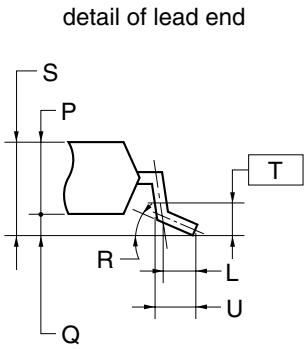


## 4. PACKAGE DRAWINGS

• μPD720102GC-YEB-A

## 120-PIN PLASTIC TQFP (FINE PITCH) (14x14)




**NOTE**

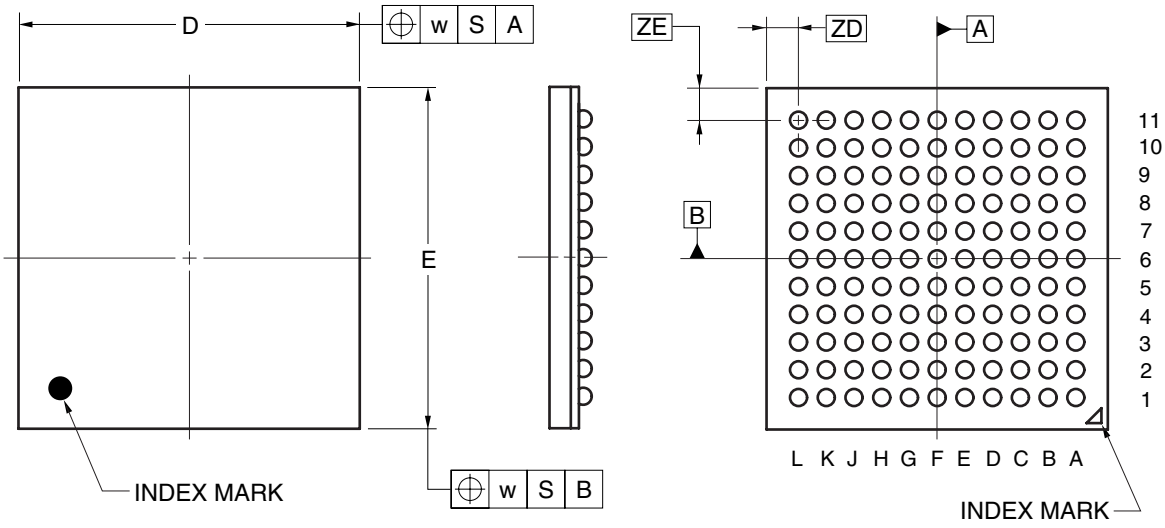
Each lead centerline is located within 0.07 mm of its true position (T.P.) at maximum material condition.

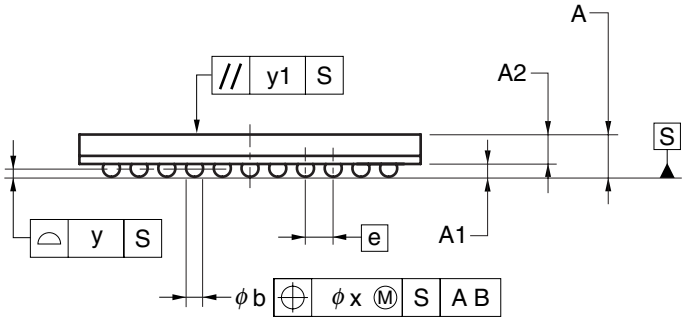
| ITEM | MILLIMETERS |
|---|---|
| A | 16.00±0.20 |
| B | 14.00±0.20 |
| C | 14.00±0.20 |
| D | 16.00±0.20 |
| F | 1.20 |
| G | 1.20 |
| H | 0.18±0.05 |
| I | 0.07 |
| J | 0.40 (T.P.) |
| K | 1.00±0.20 |
| L | 0.50 |
| M | $0.17^{+0.03}_{-0.07}$ |
| N | 0.08 |
| P | 1.00±0.05 |
| Q | 0.10±0.05 |
| R | $3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$ |
| S | 1.20MAX. |
| T | 0.25 |
| U | 0.60±0.15 |

**P120GC-40-YEB-1**

<R> • μPD720102F1-CA7-A

## 121-PIN PLASTIC FBGA (8x8)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 8.00±0.10 |
| E | 8.00±0.10 |
| w | 0.20 |
| A | 0.99±0.10 |
| A1 | 0.30±0.05 |
| A2 | 0.69 |
| e | 0.65 |
| b | 0.40±0.05 |
| x | 0.08 |
| y | 0.10 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

P121F1-65-CA7

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## 5. RECOMMENDED SOLDERING CONDITIONS

The μPD720102 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

• μPD720102GC-YEB-A: 120-pin plastic TQFP (Fine pitch) (14 × 14)

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3,<br>Exposure limit [Note]: 7 days (10 to 72 hours pre-backing is required at 125C° afterwards),<br>Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.<br><Caution><br>Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking. | IR60-107-3 |
| Partial heating method | Pin temperature: 350°C or below,<br>Heat time: 3 seconds or less (per each side of the device) ,<br>Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. | – |

**Note** The Maximum number of days during which the product can be stored at a temperature of 5 to 25°C and a relative humidity of 20 to 65% after dry-pack package is opened.

<R> • μPD720102F1-CA7-A: 121-pin plastic FBGA (8 × 8)

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Peak package's surface temperature: 260 °C, Reflow time: 60 seconds or less (220 °C or higher), Maximum allowable number of reflow processes: 3,<br>Exposure limit [Note]: 7 days (10 to 72 hours pre-backing is required at 125C° afterwards),<br>Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.<br><Caution><br>Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking. | IR60-107-3 |

**Note** The Maximum number of days during which the product can be stored at a temperature of 5 to 25°C and a relative humidity of 20 to 65% after dry-pack package is opened.

**[MEMO]**

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

### ② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

### ④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

### ⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

### ⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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