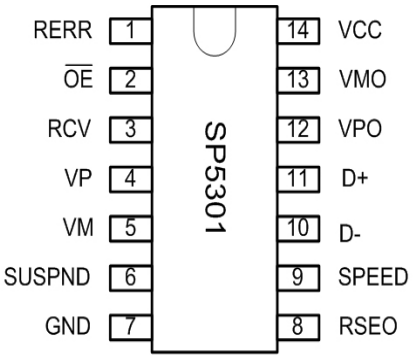
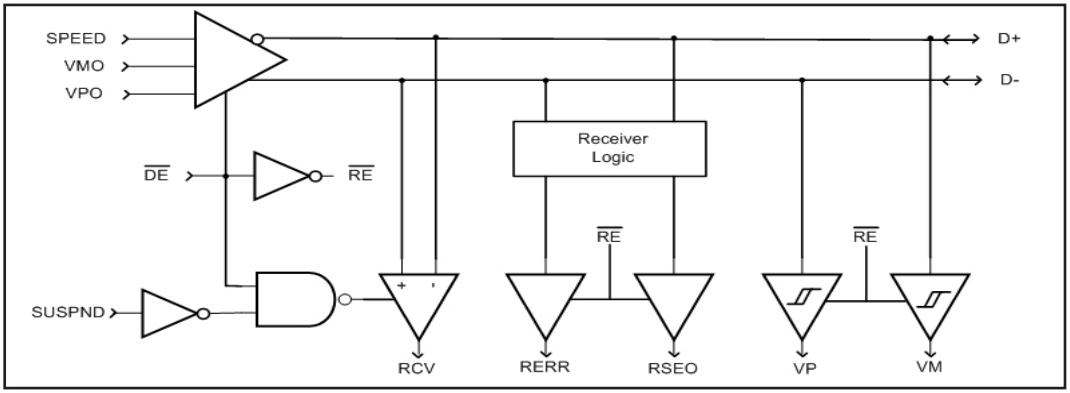
Universal Serial Bus Transceiver

- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports 12Mbps "Full Speed" and 1.5Mbps "Low Speed" serial data transmission
- Compatible with the VHDL "Serial Interface Engine" from USB developer's conference
- Hysteresis on VP and VM Function)
- Ease of use for PC peripheral expansion
- Protocol flexibility for mixed-mode isochronous data transfers and asynchronous messaging
- Available in 14 pin TSSOP package
- Rail to Rail receiver common mode input range, 20mV typical receiver sensitivity
- Low Power; 20 nA in SUSPEND mode
- Enhanced version of the PDIUSBP11



DESCRIPTION

The SP5301 is a half-duplex Universal Serial Bus (USB) differential transceiver that interfaces with the USB Serial Interface Engine (SIE). The SP5301 is designed to allow 3.3V or 5.0V standard and programmable logic to interface with the physical layer of the Universal Bus. The USB protocol can support multiple connections for up to 127 physical devices composed of many diverse functions. It is capable of transmitting and receiving serial data at both full speed (12Mbps) and low speed (1.5Mbps) data rates. Implementation of the Serial Interface Engine along with the USB transceiver allow the designer to make flexible USB compatible devices with widely available logic components. The SP5301 is specifically geared towards low-cost USB solutions for the PC peripheral market.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.5V to +6.5V
I_{GND}, I_{CC} (DC V_{CC} or GND current).....±100mA
Input Current and Voltages:
I_{IK} (DC input diode current at V_I < 0).....-50mA
V_I (DC input voltage, Note 1).....-0.5 to +6.5V
$V_{I/O}$ (DC input voltage range, I/O).....-0.5V to V_{CC} + 0.5V
Output Currents and Voltages:
I_{OK} (DC output diode current where $V_O > V_{CC}$ or $V_O < 0$).....±50mA
V_O (DC output voltage), Note 1.....-0.5V to (V_{CC} + 0.5V)
I_O (DC output source or sink current for VP/VM/RCV/RERR/RSEO pins, V_O = 0 to V_{CC}).....±15mA
I_O (DC output source or sink current for D+/D- pins, V_O = 0 to V_{CC}.....±50mA
Storage Temperature.....-65°C to +150°C
Ptot (Power dissipation per package).....1000mW



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

$\overline{OE}$	SUSPND	RCV	RERR	RSEO	VP/VM	D+/D-	Comments
0	0	0	0	0	0	Active	Driving
0	1	0	0	0	0	Active	Driving
1	0	Active	Active	Active	Active	HI-Z	Receiving
1	1	0	Active	Active	Active	HI-Z	Low Power State

Function Table

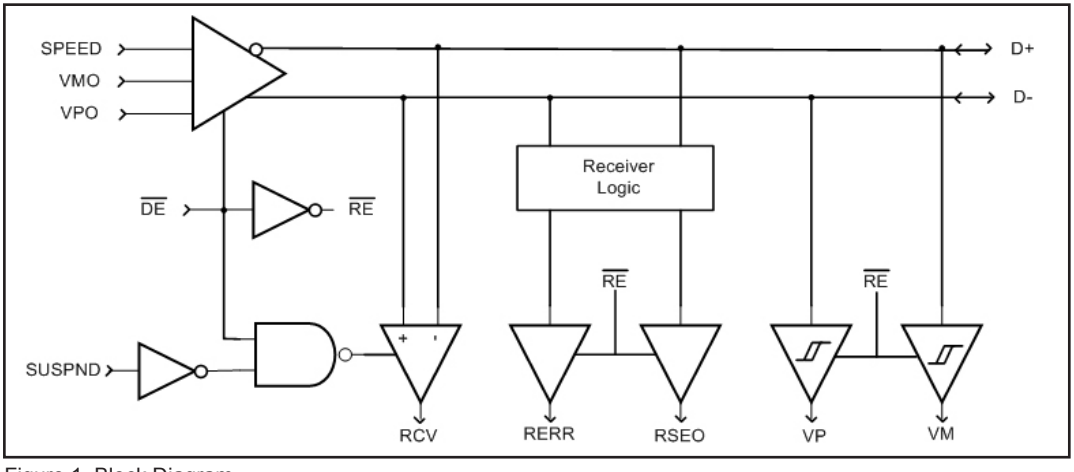


Figure 1. Block Diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for Vcc = +3.0V to +3.6V with T_{amb} = 0°C to +70°C.

Typical values apply at Vcc = +3.3V and T_{amb} = 25°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC Characteristics					
HIGH level input, V_{IH}	2.0			V	Note 2
LOW level input, V_{IL}			0.8	V	Note 2
HIGH level Driver output impedance, R_{DH}	28	35	43	Ω	Note 3, Note 4
LOW level Driver output impedance, R_{DL}	28	35	43	Ω	Note 3, Note 4
D+/D- High output level, V_{OH}	2.8			V	R_L of 15k to Ground
D+/D- Low output level, V_{OL}			0.3	V	R_L of 1.5k to 3.6V
Logic High level output, V_{OH}	2.2	2.7		V	Vcc = 3.0V, I_O = 6mA, Note 2
Logic High level output, V_{OH}	2.4			V	Vcc = 3.0V, I_O = 4mA, Note 2
Logic High level output, V_{OH}	2.8			V	Vcc = 3.0V, I_O = 200µA, Note 2
Logic Low level output, V_{OL}		0.3	0.8	V	Vcc = 3.0V, I_O = 6mA, Note 2
Logic Low level output, V_{OL}			0.4	V	Vcc = 3.0V, I_O = 4mA, Note 2
Logic Low level output, V_{OL}			0.2	V	Vcc = 3.0V, I_O = 200µA, Note 2
Receiver Differential Input Threshold, V_{DI}	-90	+/-20	+90	mV	Common Mode Voltage 0V to Vcc
Receiver Common Mode Range, V_{CM}	0		Vcc	V	
Quiescent supply current, I_{CCQ}		450	800	µA	Vcc = 3.6V, V_I = Vcc or GND, I_O = 0
Supply current in SUSPND, I_{CCS}		0.02	1.0	µA	Vcc = 3.6V, V_I = Vcc or GND, I_O = 0
Active Supply current (Full Speed), I_{CCFS}		6	14	mA	Vcc = 3.6V, C_L = 50pF, 1,0,1,0....input
Active Supply current (Low Speed), I_{CCLS}		3	8	mA	Vcc = 3.6V, C_L = 350pF, 1,0,1,0....input
Input Leakage current, I_I		+/-0.1	+/-5	µA	Vcc = 3.6V, V_I = 5.5V or GND, not for I/O pins
Tri-State output OFF-state current, I_{OZ}			+/-10	µA	V_L = V_I or V_{IL}, V_O = Vcc or GND, Note 3
Transceiver Capacitance (D+/D-), C_{IN}			20	pF	

Note 2: All signals except D+ and D-.
Note 3: See "Load D+ and D-" diagram for testing details.
Note 4: This value includes a 22Ω external resistor.

Unless otherwise noted, the following specifications apply for Vcc = +3.0V to +3.6V with T_{amb} = 0°C to +70°C.

Typical values apply at Vcc = +3.3V and T_{amb} = 25°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
AC Characteristics					
VPO/VMO to D+/D- Delay, Full Speed, t_{PLH}	4	11	15	ns	Figure 2, 9
VPO/VMO to D+/D- Delay, Full Speed, t_{PHL}	4	11	15	ns	Figure 2, 9
D+/D- Rise Time, Full Speed, t_{RISE}	4	5.6	20	ns	Figure 3, 9
D+/D- Fall Time, Full Speed, t_{FALL}	4	5.6	20	ns	Figure 3, 9
VPO/VMO to D+/D- Delay, Low Speed, t_{PLH}	30	80	200	ns	Figure 2, 9
VPO/VMO to D+/D- Delay, Low Speed, t_{PHL}	30	80	200	ns	Figure 2, 9
D+/D- Rise Time, Low Speed, t_{RISE}	75	110	250	ns	Figure 3, 9
D+/D- Fall Time, Low Speed, t_{FALL}	75	110	250	ns	Figure 3, 9
D+/D- to RCV Delay, t_{PLH}		8.0	16	ns	Figure 4, 7
D+/D- to RCV Delay, t_{PHL}		8.0	16	ns	Figure 4, 7
D+/D- to VP/VM Delay, t_{PLH}		6.0	10	ns	Figure 2, 7
D+/D- to VP/VM Delay, t_{PHL}		6.0	10	ns	Figure 2, 7
D+/D- to RERR Delay, t_{PLH}		14	20	ns	Figure 7, Note 5
D+/D- to RERR Delay, t_{PHL}		14	20	ns	Figure 7, Note 5
D+/D- to RSEO Delay, t_{PLH}		11	16	ns	Figure 7, Note 5
D+/D- to RSEO Delay, t_{PHL}		11	16	ns	Figure 7, Note 5
$\overline{OE}$ to D+/D-, t_{PHZ}		11	20	ns	Figure 5, 8
$\overline{OE}$ to D+/D-, t_{PZH}		12	20	ns	Figure 5, 8
$\overline{OE}$ to D+/D-, t_{PLZ}		11	20	ns	Figure 5, 8
$\overline{OE}$ to D+/D-, t_{PZL}		12	20	ns	Figure 5, 8
Setup for SPEED, t_{SU}	0			ns	Figure6, 9
D+/D- Crossover point, V_{CR}	1.3		2.0	V	

Note 5: Delay defined from midpoint of input to midpoint of output, with other input at static (High or Low).

DESCRIPTION

The SP5301 is a half-duplex Universal Serial Bus (USB) differential transceiver that interfaces with the VHDL Serial Interface Engine (SIE) from the USB developer's conference. The SP5301 is designed to allow digital logic to communicate with the physical layer of the Universal Bus.

The USB is a cable bus that supports data exchange between a host computer and a wide range of peripherals. Attached peripherals share USB bandwidth through a host scheduled token based protocol. The USB allows peripherals to be atached, configured, used, and detached while the host and other peripherals are in operation. This is referred to as dynamic, or hot, attachment and removal. USB attributes include lower costs, hot plug-and-play with dynamic attach-detach capabilities, ease of design and use, multiple peripherals, guaranteed latency, and guaranteed bandwidth.

The USB is specified to be an industry standard extension to the PC architecture with a focus on Computer Telephony Integration (CTI), consumer, and productivity applications. The architecture of the USB protocol can ease the expansion of PC peripherals, provide a low-cost solution that supports tranfer rates up to 12Mbps, and can fully support real-time data for voice, audio, and compressed video.

The USB protocol can provide protocol flexibility for mixed-mode isochronous data transfers and asynchrounous messaging. Guaranteed bandwidth and low latencies are appropriate for many telephony and audio applications. A 12Mbps bus covers the mid-speed and low-speed data ranges. Typically, mid-speed data types are isochronous and low-speed data comes from interactive devices. Isochronous communication can only be used by full speed devices.

THEORY OF OPERATION

The USB protocol can support multiple connections for up to 127 physical devices composed of many diverse functions. This makes the SP5301 an ideal solution for multidrop applications. This lower protocol overhead results in high bus utilization. An isochronous workload may utilize the entire USB bus bandwidth. The USB protocol reflects a robust capability of dynamic insertion and removal of devices identified in user perceived real-time. This PC plug and play quality preserves the marketable synergy with the PC industry, being a simple protocol to implement and integrate into existing operating systems.

The SP5301 contains a differential driver and a differential receiver in a half-duplex configuration. The driver is enabled by the $\overline{OE}$ pin. If $\overline{OE}$ is asserted LOW, the driver is active and the D- and D+ pins drive USB signals. The differential receiver is also controlled by the $\overline{OE}$ pin. If $\overline{OE}$ is HIGH, while SUSPEND is LOW, the receiver is active and the driver is in tri-state. In this receive mode, the D- and D+ pins are now receiving USB signals.

The typical driver output voltage swing for D- and D+ of the SP5301 will be less than +0.3V for the LOW state and greater than +2.8V for the HIGH state.

The SP5301 is a USB differential interface with very high receiver input sensitivity. This makes data virtually immune to noise on the USB pipeline. The ±90mV minimum receiver input sensitivity of the SP5301 ensures recovery of even severely attenuated signals.

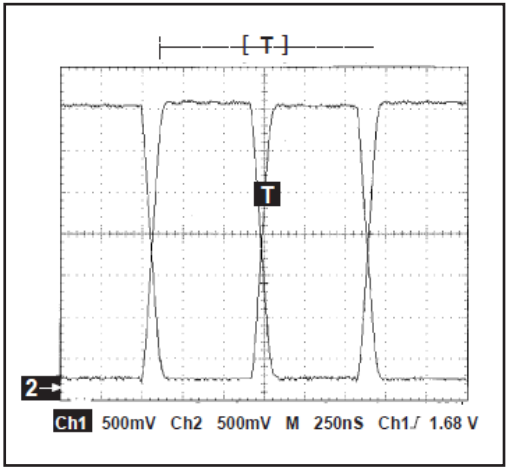
The SP5301 incorporates a receive error circuit. This error circuit outputs CMOS signals on the receive error pin (RERR) and the receive single ended zero pin (RSE0) under specific conditions from the USB bus. When $\overline{OE}$ is asserted LOW, it enables the USB driver to transmit data on the D+ and D- output pins. The receive error circuit is disabled in this condition and both RERR and RSE0 are forced low. The receive error circuit is activated in receive mode when $\overline{OE}$ is HIGH. The receive error circuit will signal an error state when both D+ and D- are HIGH by forcing RERR HIGH. The receiver error circuit will signal a single ended zero when both D+ and D- are LOW by forcing RSE0 HIGH. A single ended zero is a valid state and is used to signal an end of packet (EOP) in signal transmission. (CAUTION: Since both RERR and RSE0 are CMOS outputs, care must be taken to ensure that RERR and RSE0 are NOT connected to VCC or GND.)

The SP5301 has a suspend input pin (SUSPND) which enables a low power state while the USB bus is inactive. When SUSPND is asserted HIGH or SP5301 is in transmit mode ($\overline{OE}$ is LOW), the receive data pin (RCV) will be forced LOW.

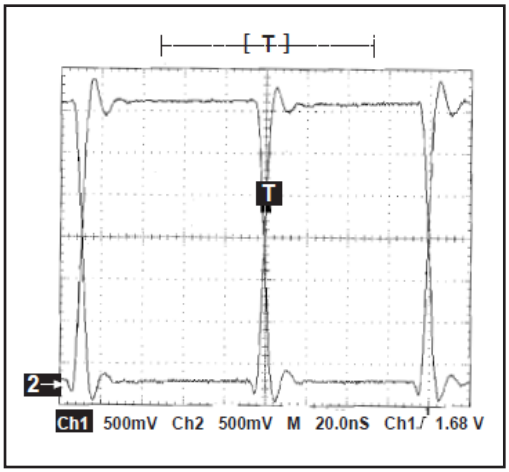
The SP5301 can transmit and receive serial data at both full speed, 12Mbps, and at low speed, 1.5Mbps, data rates. At full speed, the active supply current of the SP5301 is 6mA. In the suspend state, the supply current is typically 20nA.

Full speed USB applications include ISDN, PBX, POTS, sampled analog devices, audio, printers, and telephony designs. Low speed USB applications include locator devices, keyboards, mouse, tablets, light pens, stylus, game peripherals, virtual reality peripherals, and monitor configurations. The USB protocol provides full support for the real-time data for voice, audio, and compressed video. The SP5301 is specifically geared towards low-cost USB solutions for the PC peripheral markets

Waveforms 1 and 2 below show device behavior in transmit mode, at both low and full speed, with the D+/D- pins driving the load specified in figure 9.

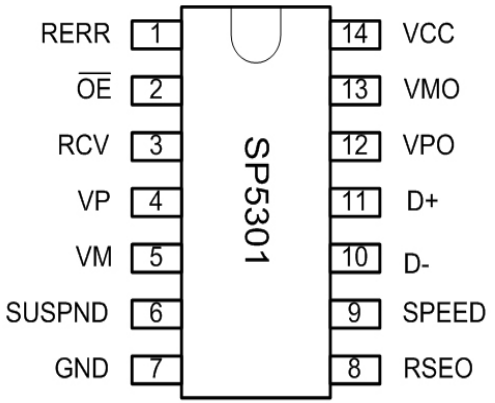


Waveform 1. D+/D- Transmit Mode, low speed



Waveform 2. D+/D- Transmit Mode, full speed

PINOUT



PIN ASSIGNMENTS

Pin 1 — RERR — Receive Error. This CMOS level output pin is forced HIGH when both D+ and D- are HIGH to signal an error state. **CAUTION**: Since RERR is a CMOS output, care must be taken to ensure that RERR is **NOT** connected to VCC or GND.

Pin 2 — $\overline{OE}$ — Output Enable Not. When asserted LOW, this input pin enables the driver to transmit data on the bus. When HIGH, the receiver is active and the driver outputs are in tri-state.

Pin 3 — RCV — Receive data. This is a CMOS level output pin from D+ and D-, typically connected to the inputs of the USB Serial Interface Engine (SIE).

Pin 4, 5 — VP, VM — Gated version of D+ and D-. Used to detect single ended zero (SEO), error conditions, and interconnect speed. These pins have CMOS level outputs.

VP	VM	RESULT
0	0	SEO
0	1	Low Speed
1	0	Full Speed
1	1	Error

Pin 6 — SUSPND — Suspend. This input pin provides a low power state for the SP5301 while the USB bus is inactive. While the SUSPND pin is asserted HIGH, it will drive RCV pin LOW.

Pin 7 — GND — Ground.

Pin 8 — RSEO — Receive Single Ended Zero. This CMOS level output pin is forced HIGH when both D+ and D- are LOW to signal the end of packet (EOP) in signal transmission. **CAUTION**: Since RSEO is a CMOS output, care must be taken to ensure that RSEO is **NOT** connected to VCC or GND.

Pin 9 — SPEED — Speed. Edge rate control. This input pin determines edge rates, where a logic HIGH designates edge rates for "full speed" and logic LOW designates edge rates for "low speed."

Pin 10, 11 — D-, D+ — Data-, Data+. These differential data bus I/O pins conform to the Universal Serial Bus standard.

Pin 12, 13 — VPO, VMO — These are the logic inputs to the differential driver, typically connected to the outputs of the serial Interface Engine (SIE).

VPO	VMO	RESULT
0	0	SEO
0	1	Logic Low
1	0	Logic High
1	1	Undefined

Pin 14 — Vcc — +3.0V to +3.6V power supply

AC WAVEFORMS

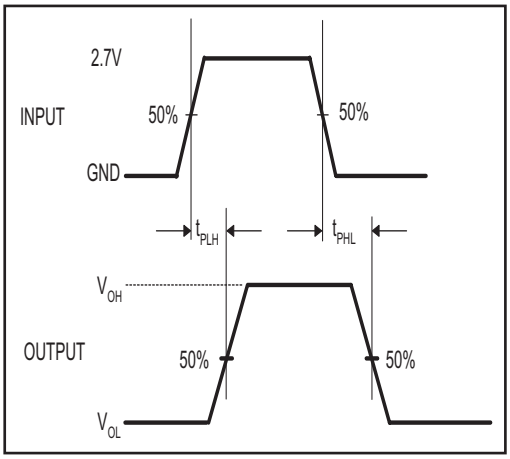


Figure 2. D+/D- to VP/VM or VPO/VMO to D+/D-

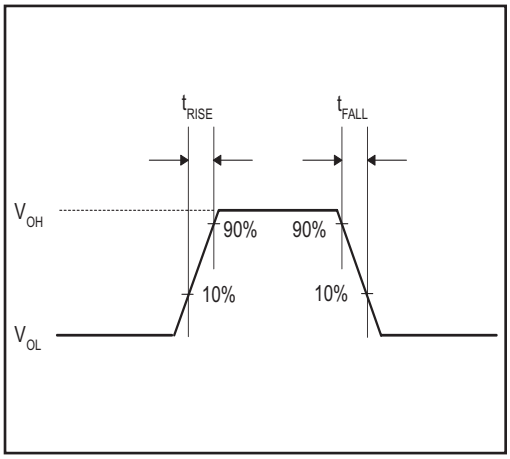


Figure 3. Rise and Fall Times

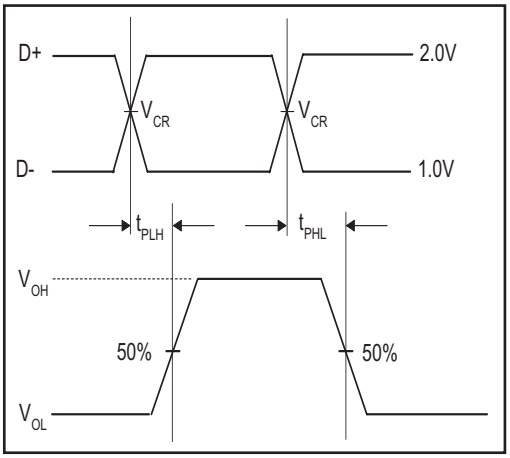


Figure 4. D+/D- to RCV

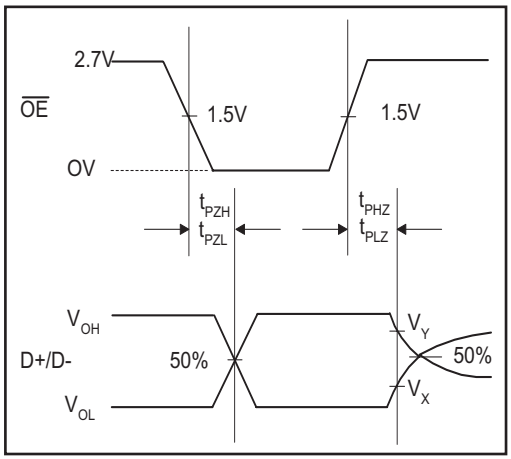


Figure 5. $\overline{OE}$ to D+/D-

NOTE: $V_X = V_{OL} + 0.3V$, $V_Y = V_{OH} - 0.3V$, Vcc ≥ +3.0V, V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.

AC WAVEFORMS (continued)

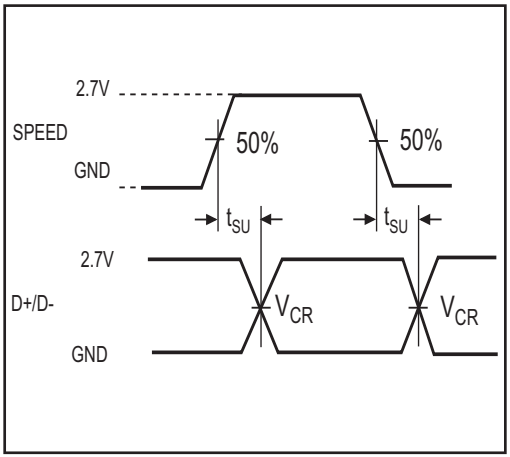


Figure 6. Setup for Speed

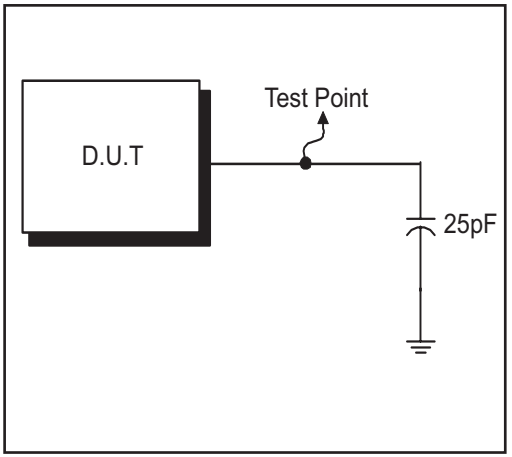


Figure 7. Load for VM, VP, RERR, RSEO and RCV

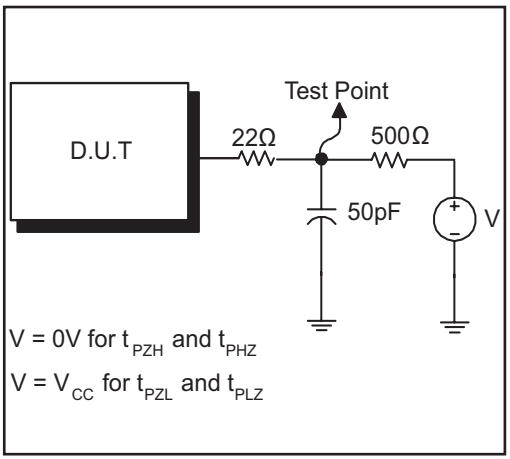


Figure 8. Load for Enable and Disable Times

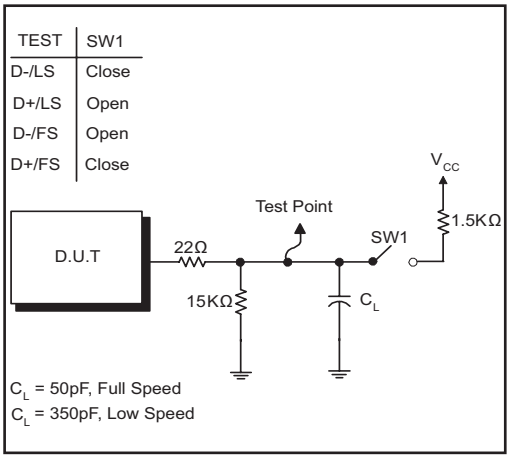


Figure 9. Load for D+/D-

AC WAVEFORMS (continued)

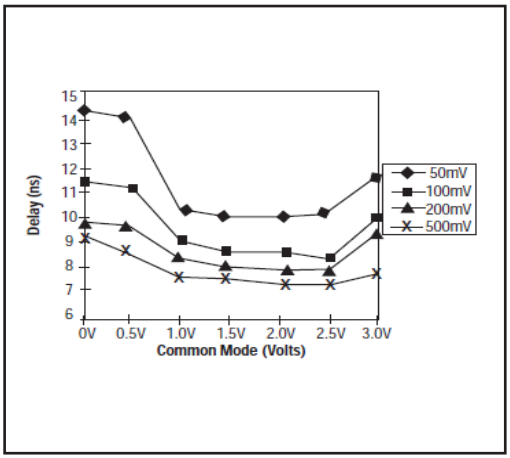


Figure 10. Receiver Delay VS. Common Mode Voltage (with peak to peak over-drive voltage as a parameter)

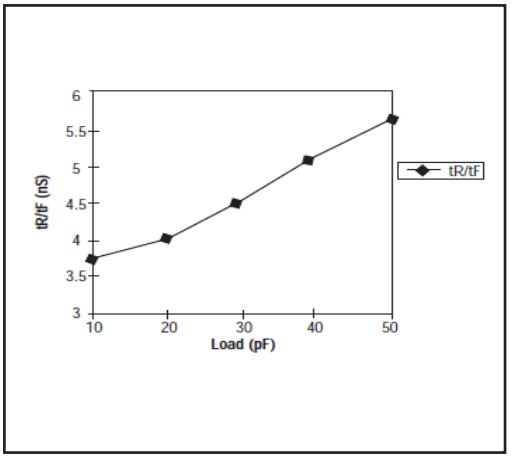


Figure 11. Transmitter Rise and Fall Time VS. Capacitive load (full speed)

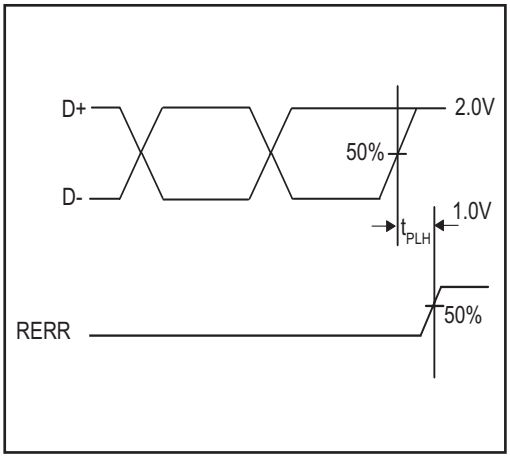


Figure 12. D+/D- to RERR Delay

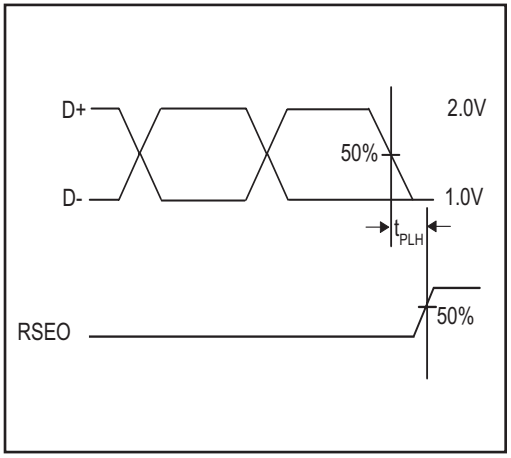
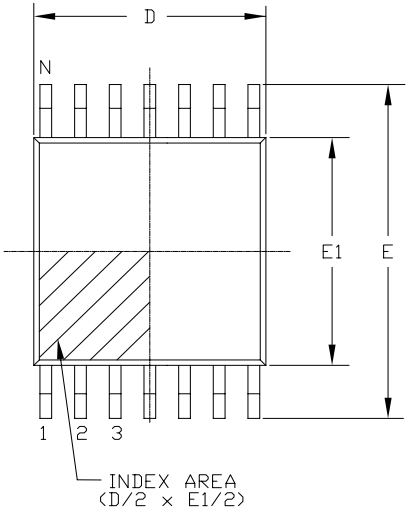
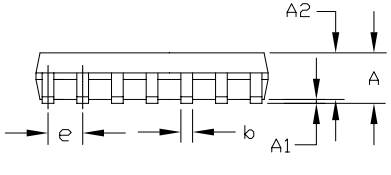


Figure 13. D+/D- to RSEO Delay

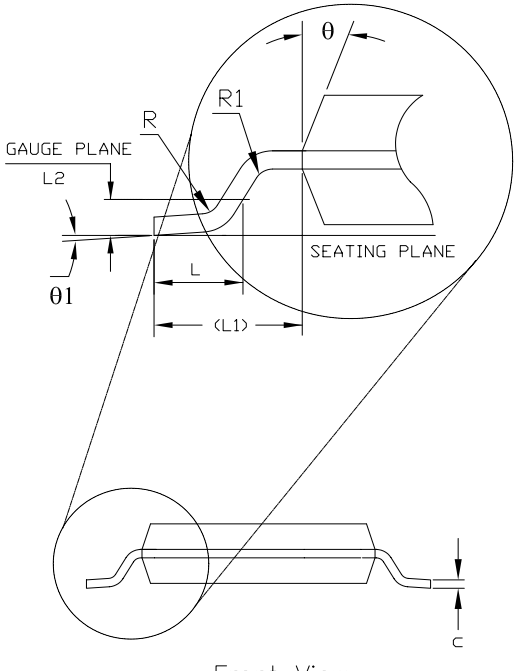
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/19/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

Top View





Side View



Front View

14 Pin TSSOP JEDEC MO-153 Variation AB-1						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	4.90	5.00	5.10	0.193	0.197	0.200
N	14			14		

EXAR Powering Connectivity

EXAR CORPORATION

14 PIN TSSOP PACKAGE OUTLINE

Packaging Approval:

By: JL Date: 11/21/07

Drawing No: 14-PIN TSSOP

Revision: B Sheet: 1 OF 1

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP5301CY-L	0°C to +70°C	14-pin TSSOP
SP5301CY-L/TR	0°C to +70°C	14-pin TSSOP

Note: /TR = Tape and Reel

REVISION HISTORY

DATE	REVISION	DESCRIPTION
--	--	Legacy Sipex Datasheet
08/17/10	1.0.0	Convert to Exar Format. Update ordering information as a result of discontinued NSOIC package option.

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