Sensor Signal Conditioning IC for Closed-Loop Magnetic Current Sensors

Check for Samples: DRV411

FEATURES

- **Optimized for Symmetric Hall-Elements (for example, AKM HW-322, HW-302, or similar)**
- **Spinning Current Hall Sensor Excitation**
  - **Elimination of Hall Sensor Offset and Drift**
  - **Elimination of 1/f Noise**
- **Extended Current Measurement Range**
  - **H-Bridge Drive Capability: 250 mA**
- **Precision Difference Amplifier:**
  - **Offset and Drift: 100 µV (max), 2 µV/°C (max)**
  - **System Bandwidth: 200 kHz**
- **Precision Reference:**
  - **Accuracy: 0.2% (max)**
  - **Drift: 50 ppm/°C (max)**
  - **Pin-Selectable for 2.5 V, 1.65 V, and Ratiometric Mode**
- **Overrange and Error Flags**
- **Supply: 2.7 V to 5.5 V**
- **Packages: 4-mm × 4-mm QFN and TSSOP-20 PowerPAD™**
- **Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Closed-Loop Current-Sensor Modules**
- **DC and AC Current Measurement**

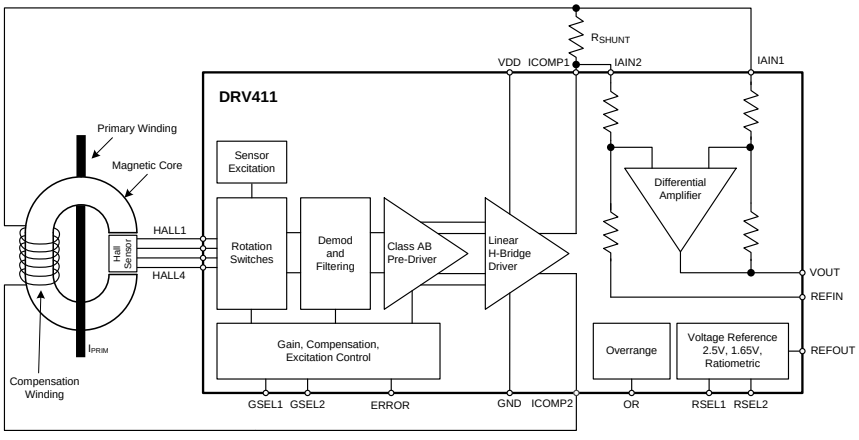
DESCRIPTION

The DRV411 is designed to condition InSb Hall elements for use in closed-loop current-sensor modules. The DRV411 provides precision excitation circuitry for the Hall-element effectively eliminating the offset and offset-drift of the Hall element. This device also provides a 250-mA H-bridge for driving the sensor compensation coil as well a precision differential amplifier to generate the output signal. The 250-mA drive capability of the H-bridge roughly doubles the current measurement range compared to conventional single-ended drive methods.

The Hall sensor front-end circuit and the differential amplifier employ proprietary offset cancelling techniques. These techniques, along with a high-accuracy voltage reference, significantly improve the accuracy of the overall current-sensor module. The output voltage is pin-selectable to support a 2.5-V output for use with a 5-V power supply, as well as 1.65-V for 3.3-V sensors.

For optimum heat dissipation, the DRV411 is available in thermally enhanced 4-mm × 4-mm QFN and TSSOP-20 with PowerPAD packages. The DRV411 is specified for operation over the full extended industrial temperature range of –40°C to +125°C.

BLOCK DIAGRAM



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Supply voltage (VDD to GND)			+7	V
Input voltage(2)		GND – 0.5	VDD + 0.5	V
Differential amplifier inputs		GND – 6	VDD + 6	V
Input current to input terminals(3)		–25	+25	mA
ICOMP short circuit(4)			300	mA
Junction temperature, T_J max		–50	+150	°C
Storage temperature range, T_{stg}		–65	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01	–2000	+2000	V
	Charged device model (CDM) JEDEC standard 22, test method C101	–1000	+1000	V
	Machine model (MM) JEDEC standard 22, test method A115	–150	+150	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited, except for the differential amplifier input pins.
(3) These inputs are not internally protected against overvoltage. The differential amplifier input pins must be limited to 5 mA (max) or ±1.5 V (max).
(4) Power-limited; observe maximum junction temperature.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV411		UNITS
		PWP (TSSOP)	RGP (QFN)	
		20 PINS	20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	37.2	33.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	24.3	34.6	
θ_{JB}	Junction-to-board thermal resistance	19.8	11.1	
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.4	
ψ_{JB}	Junction-to-board characterization parameter	19.6	11.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.0	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{DD} = +2.7 V to +5.5 V, and zero output current I_{COMP}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DRV411 MIN	DRV411 TYP	DRV411 MAX	UNIT
HALL ELEMENT EXCITATION / AMPLIFICATION						
V_{EX}	Hall sensor excitation voltage	T_A= –40°C to +125°C, GSEL [00,01,10]	0.7	0.8	0.95	V
		T_A= –40°C to +125°C, GSEL [1,1]	0.6	0.74	0.95	V
I_{EX}	Hall sensor excitation current	T_A= –40°C to +125°C			10	mA
f_{spin}	Excitation switching frequency			1		MHz
AOL_{FB}	Front-end open-loop flatband gain	GSEL [0,0](1), f_{Zero} = 3.8 kHz		250		V/V
		GSEL [0,1], f_{Zero} = 7.2 kHz		250		V/V
		GSEL [1,0], f_{Zero} = 3.8 kHz		1000		V/V
AOL	Front-end open-loop gain	T_A= –40°C to +125°C, GSEL [00,01,10,11]	94	120		dB
V_{OS_FE}	Front-end voltage offset	No Hall sensor, GSEL [00, 01, 10]		20	100	µV
		GSEL [1,1]		5	12	mV
dV_{OS_FE}/dT	Front-end voltage offset drift	T_A= –40°C to +125°C, no Hall sensor, GSEL [00,01,10]		0.2		µV/°C
		T_A= –40°C to +125°C, GSEL [1,1]		5		µV/°C
GBWP	Gain-bandwidth product	GSEL [1,1]		14		MHz
CMRR	Common-mode-rejection ratio	GSEL [1,1], V_{CM} = 0 V to VDD – 1.8 V		300		µV/V
	Error comparator threshold			75		mV
DIFFERENTIAL AMPLIFIER						
V_{OS}	Input offset voltage, RTO(2) (3)	V_{IN1} = V_{IN2} = V_{REFIN}		±0.01	±0.1	mV
dV_{OS}/dT	Input offset voltage drift, RTO	T_A= –40°C to +125°C		±0.4	±2	µV/°C
CMRR	vs common-mode voltage, RTO	V_{CM} = −1 V to V_{DD} + 1 V, V_{REF} = V_{DD} / 2		±50	±250	µV/V
PSRR	vs power-supply, RTO	V_{DD} = +2.7 V to +5.5 V, V_{CM} = V_{REFIN}		±4	±50	µV/V
V_{CM}	Common-mode input range		–1		V_{DD} + 1	V
	Differential impedance		16.5	20	23.5	kΩ
	Common-mode impedance		40	50	60	kΩ
	External reference input impedance		40	50	60	kΩ
G	Gain, V_{OUT}/V_{IN_DIFF}	T_A= –40°C to +125°C		4		V/V
G_{ERR}	Gain error			±0.02%	±0.3%	
	Gain error drift	T_A= –40°C to +125°C		±1	±5	ppm/°C
	Linearity error	R_L = 1 kΩ		12		ppm
	Voltage output swing from negative rail(3) (OR pin trip level)	I = +2.5 mA, V_{DD} = 5 V, comparator trip level		48	85	mV
	Voltage output swing from positive rail(3) (OR pin trip level)	I = –2.5 mA, V_{DD} = 5 V, comparator trip level	V_{DD} – 85	V_{DD} – 48		mV
I_{SC}	Short-circuit current(3)	V_{OUT} connected to GND		–18		mA
		V_{OUT} connected to V_{DD}		20		mA
	Signal overrange indication delay (OR pin)(3)	V_{IN} = 1-V step, see note (3)		2.5 to 3.5		µs
BW_{-3dB}	Bandwidth(3)			2		MHz
SR	Slew rate			6.5		V/µs
	Settling time large-signal(3)	ΔV = ± 2 V to 1%, no external filter		0.9		µs
	Settling time(3)	ΔV = ± 0.4 V to 0.01%		8		µs
e_n	Output voltage noise density, RTO(3)	f = 1 kHz, compensation loop disabled		170		nV/√Hz

(1) Note that the numbers in the brackets correspond to the GSEL number and its value. For example, in this case, GSEL [0,0] means that GSEL1 = 0 and GSEL2 = 0.
(2) Parameter value referred to output (RTO).
(3) See Typical Characteristic curves.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +2.7 V to +5.5 V, and zero output current I_{COMP}, unless otherwise noted.

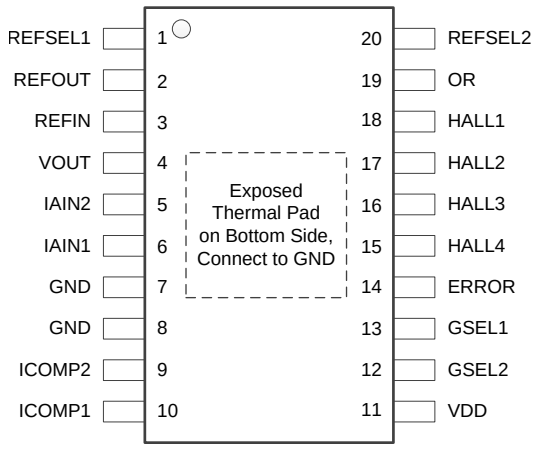
PARAMETER		TEST CONDITIONS	DRV411			UNIT
			MIN	TYP	MAX	
COMPENSATION COIL DRIVER, H-BRIDGE						
	Peak current	T_A= –40°C to +125°C, $V_{ICOMP1} – V_{ICOMP2}$ = 4.2 V_{PP}, V_{DD} = 5 V	210	250		mA
		T_A= –40°C to +125°C, $V_{ICOMP1} – V_{ICOMP2}$ = 2.5 V_{PP}, V_{DD} = 3.3 V	125	150		mA
	Voltage swing	20-Ω load, V_{DD} = 5 V	4.2			V_{PP}
		20-Ω load, V_{DD} = 3.3 V	2.5			V_{PP}
	Output common-mode			V_{DD} / 2		V
VOLTAGE REFERENCE						
V_{REF}	Reference voltage(4)	REFSEL [0,0](5), no load	2.495	2.5	2.505	V
		REFSEL [1,0], no load	1.647	1.65	1.653	V
		REFSEL [1,1], no load	49.6	50	50.4	% of V_{DD}
	Reference voltage drift(4)	T_A= –40°C to +125°C, REFSEL [00,10]		±5	±50	ppm/°C
	Voltage divider gain error drift	T_A= –40°C to +125°C, REFSEL [1,1]		±5	±50	ppm/°C
PSRR	Power-supply rejection ratio(4)	REFSEL [00,10], RGP package		±15	±200	µV/V
		REFSEL [00,10], PWP package		±15	±300	µV/V
	Load regulation	Load to GND or VDD, ΔI_{LOAD} = 0 mA to 5 mA		0.15	0.35	mV/mA
I_{SC}	Short-circuit current	REFOUT connected to VDD		20		mA
		REFOUT connected to GND		–18		mA
DIGITAL INPUT/OUTPUT						
Logic Inputs (GSEL, REFSEL pins)		**CMOS-type levels**				
	Input leakage current			0.01		µA
V_{IH}	High-level input voltage		0.7 × V_{DD}		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × V_{DD}	V
Logic Outputs (ERROR, OR pins)						
V_{OL}	Low-level output voltage	4-mA sink		0.3		V
V_{OH}	High-level output voltage			See (6)		V
POWER SUPPLY						
V_{DD}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A= –40°C to +125°C, I_{COMP} = 0 mA, no excitation			6	mA
V_{RST}	Power-on reset threshold	T_A= –40°C to +125°C		2.4		V
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–50		+150	°C

(4) See Typical Characteristic curves.
(5) Note that the numbers in the brackets correspond to the REFSEL number and its value. For example, in this case, REFSEL [0,0] means that REFSEL1 = 0 and REFSEL2 = 0.
(6) OR and ERROR are open-drain outputs. No internal pull-up resistor. Output voltage depends on the external pull up resistor that is used.

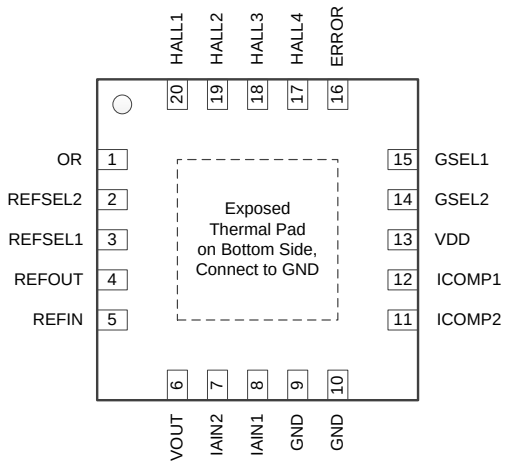
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PIN CONFIGURATION

PWP PACKAGE
TSSOP-20
(TOP VIEW)



RGP PACKAGE
QFN-20
(TOP VIEW)



PIN ASSIGNMENTS

PIN			DESCRIPTION
NAME	PWP (TSSOP)	RGP (QFN)	
ERROR	14	16	Open-drain output for error indication. See the Error Conditions section.
GND	7	9	Ground connection
GND	8	10	Ground connection
GSEL1	13	15	Input. Selects the gain of the Hall amplifier. See *Gain Selection and Compensation Frequency* section.
GSEL2	12	14	Input. Selects the gain of the Hall amplifier. See *Gain Selection and Compensation Frequency* section.
HALL1	18	20	Pin 1 of AKM HW322 / HW302 or similar
HALL2	17	19	Pin 2 of AKM HW322 / HW302 or similar
HALL3	16	18	Pin 3 of AKM HW322 / HW302 or similar
HALL4	15	17	Pin 4 of AKM HW322 / HW302 or similar
IAIN1	6	8	Inverting input of differential amplifier
IAIN2	5	7	Noninverting input of differential amplifier
ICOMP1	10	12	Output 1 of compensation coil driver
ICOMP2	9	11	Output 2 of compensation coil driver
OR	19	1	Open-drain output for overrange indication. See the *Error Conditions* section.
REFIN	3	5	Input for zero reference to differential amplifier
REFOUT	2	4	Output terminal for selected reference voltage
REFSEL1	1	3	Input. Sets reference mode. See the *Voltage Reference* section.
REFSEL2	20	2	Input. Sets reference mode. See the *Voltage Reference* section.
VDD	11	13	Supply voltage
VOUT	4	6	Output of differential amplifier
Thermal Pad			Connect to GND

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TYPICAL CHARACTERISTICS

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

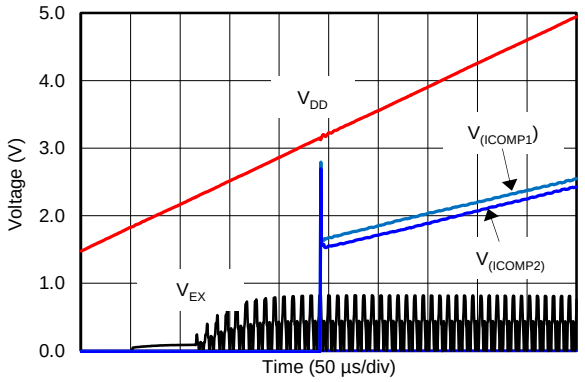


Figure 1. START-UP BEHAVIOR

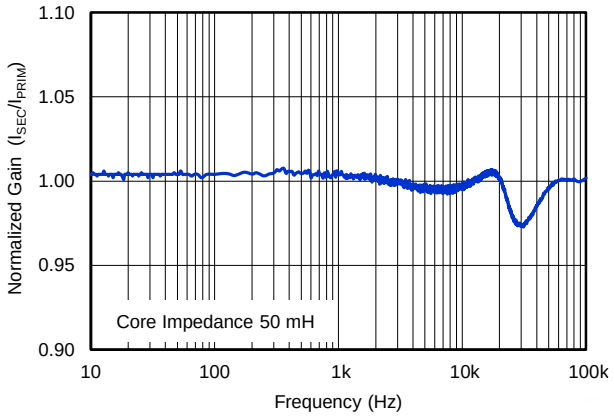


Figure 2. FRONT-END GAIN FLATNESS vs FREQUENCY

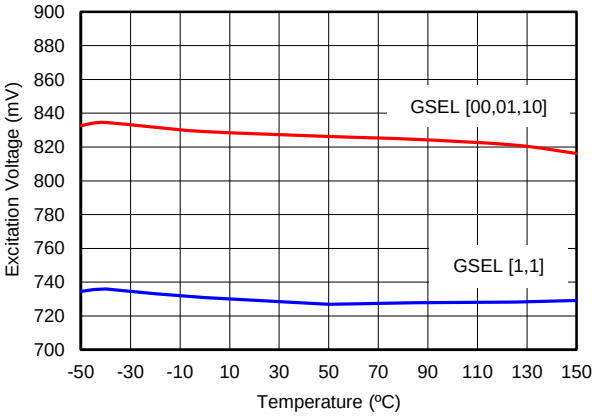


Figure 3. HALL SENSOR EXCITATION VOLTAGE vs TEMPERATURE

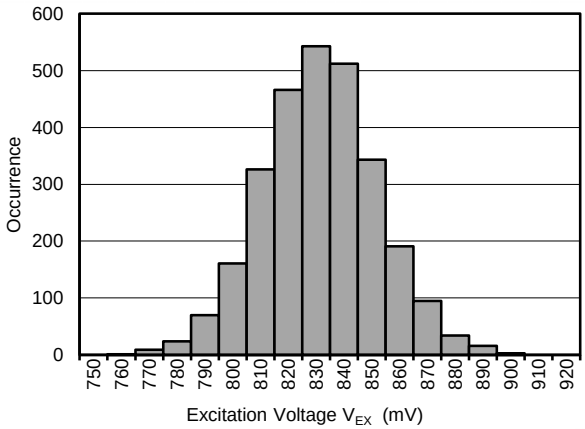


Figure 4. HALL SENSOR EXCITATION VOLTAGE HISTOGRAM

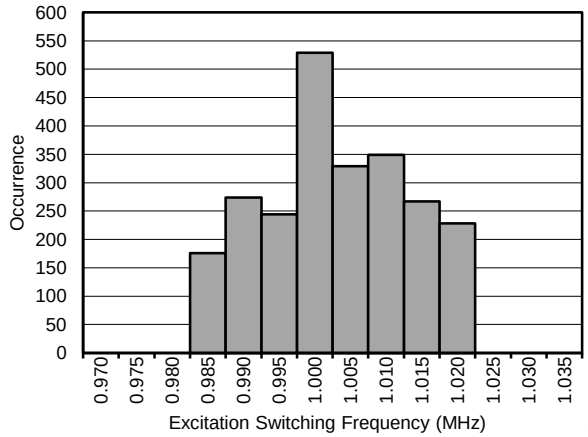


Figure 5. EXCITATION SWITCHING FREQUENCY HISTOGRAM

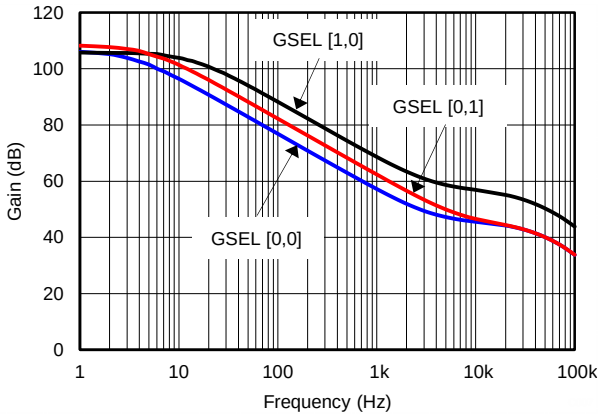


Figure 6. FRONT-END OPEN-LOOP GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

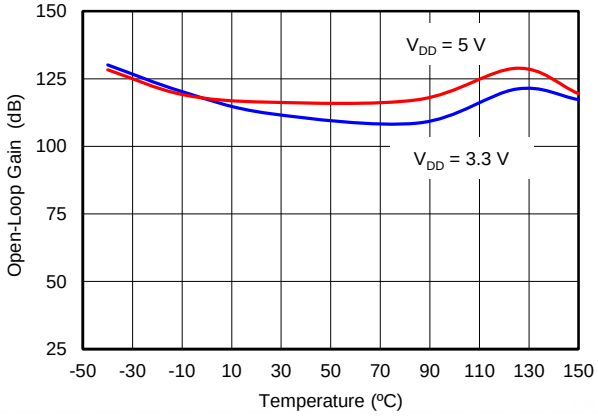


Figure 7. FRONT-END OPEN-LOOP GAIN vs TEMPERATURE

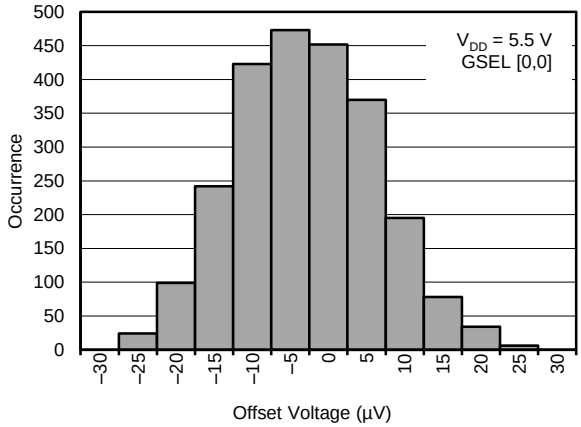


Figure 8. FRONT-END OFFSET VOLTAGE HISTOGRAM

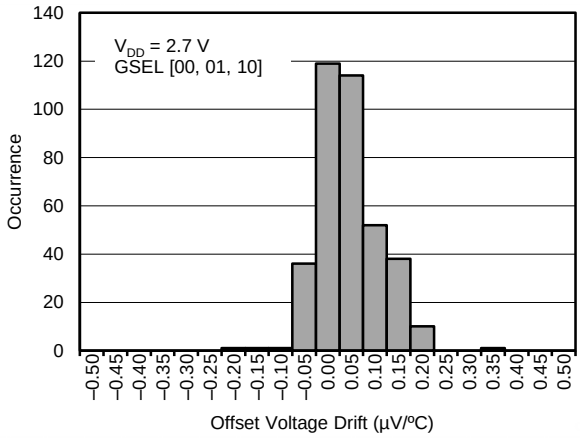


Figure 9. FRONT-END OFFSET VOLTAGE DRIFT HISTOGRAM

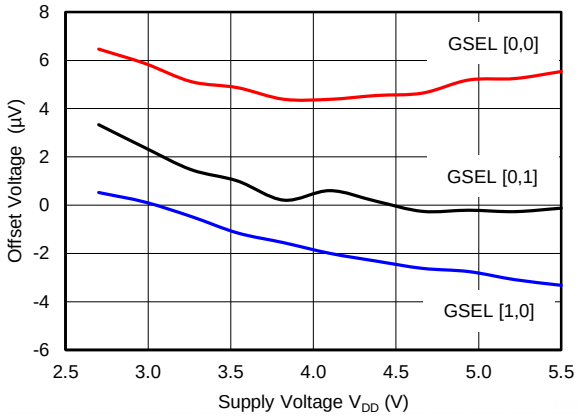


Figure 10. FRONT-END OFFSET VOLTAGE vs POWER SUPPLY

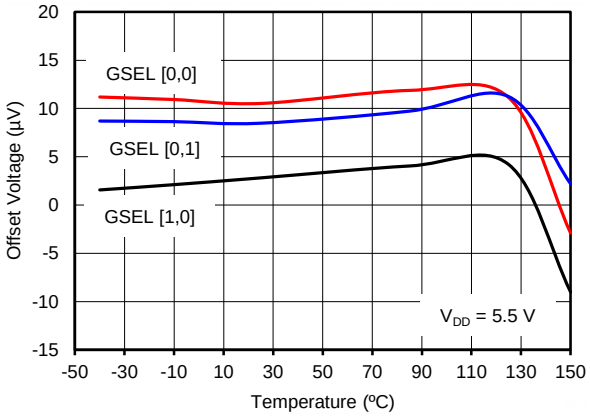


Figure 11. FRONT-END OFFSET VOLTAGE vs TEMPERATURE

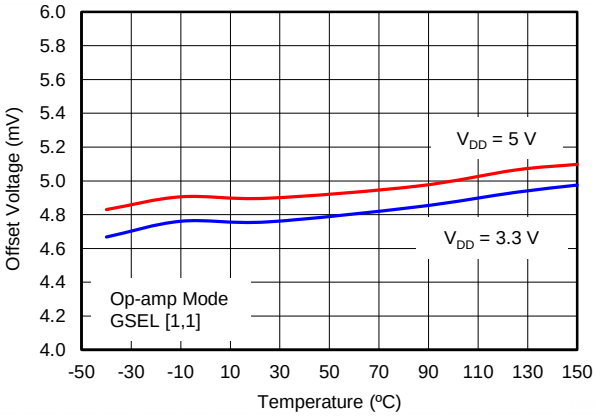


Figure 12. FRONT-END OFFSET VOLTAGE vs TEMPERATURE (OP-AMP MODE)

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

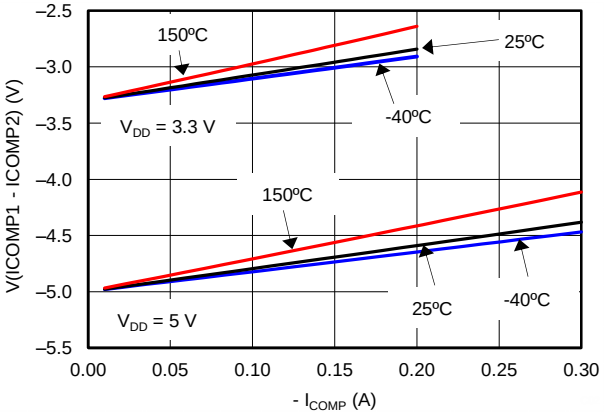


Figure 13. OUTPUT VOLTAGE SWING vs NEGATIVE OUTPUT CURRENT

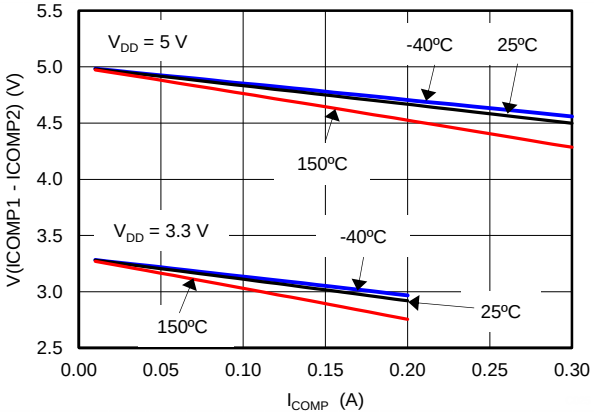


Figure 14. OUTPUT VOLTAGE SWING vs POSITIVE OUTPUT CURRENT

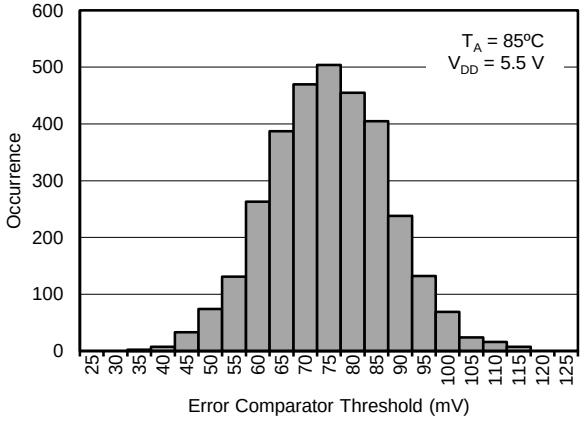


Figure 15. ERROR COMPARATOR THRESHOLD HISTOGRAM

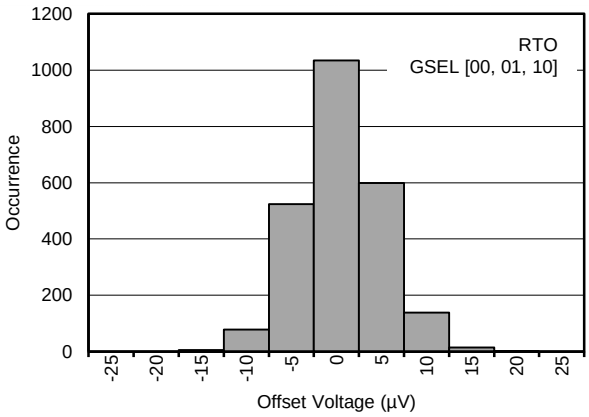


Figure 16. DIFFERENTIAL AMPLIFIER, OFFSET VOLTAGE HISTOGRAM

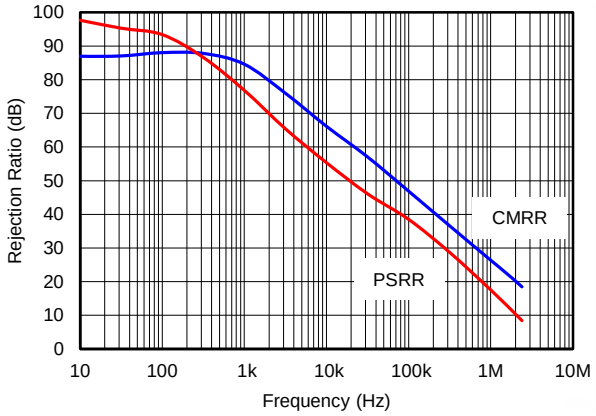


Figure 17. DIFFERENTIAL AMPLIFIER CMRR AND PSRR vs FREQUENCY

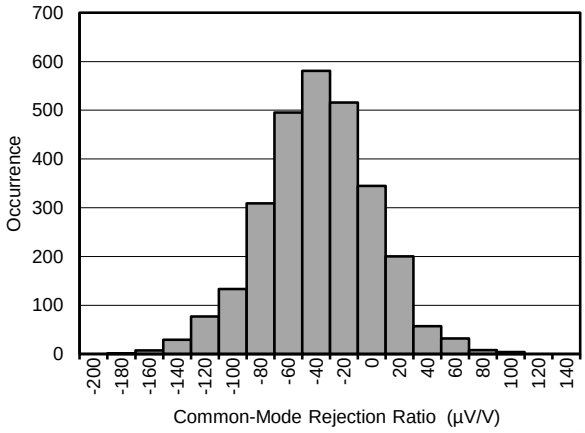


Figure 18. DIFFERENTIAL AMPLIFIER COMMON-MODE REJECTION RATIO HISTOGRAM

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

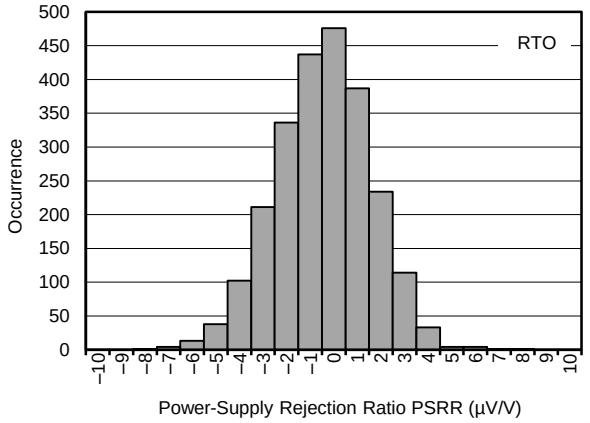


Figure 19. DIFFERENTIAL AMPLIFIER POWER-SUPPLY REJECTION RATIO HISTOGRAM

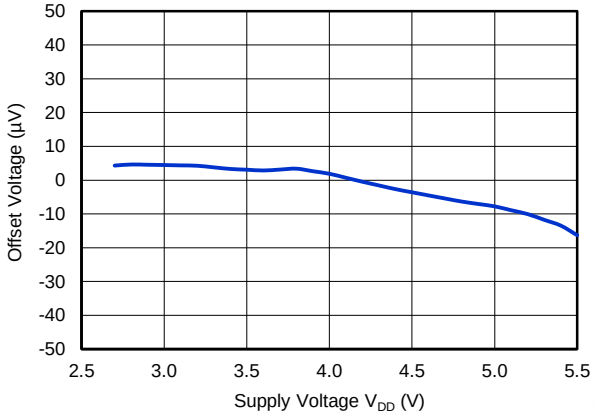


Figure 20. DIFFERENTIAL AMPLIFIER OFFSET VOLTAGE vs POWER SUPPLY

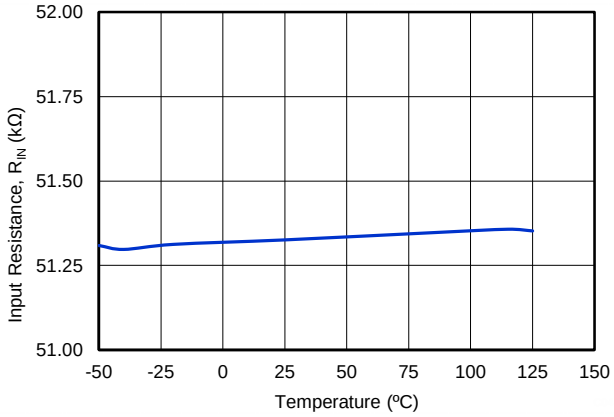


Figure 21. DIFFERENTIAL AMPLIFIER REFERENCE INPUT IMPEDANCE vs TEMPERATURE

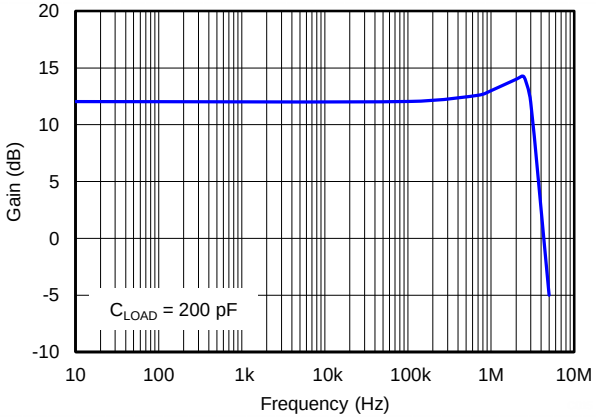


Figure 22. DIFFERENTIAL AMPLIFIER GAIN vs FREQUENCY

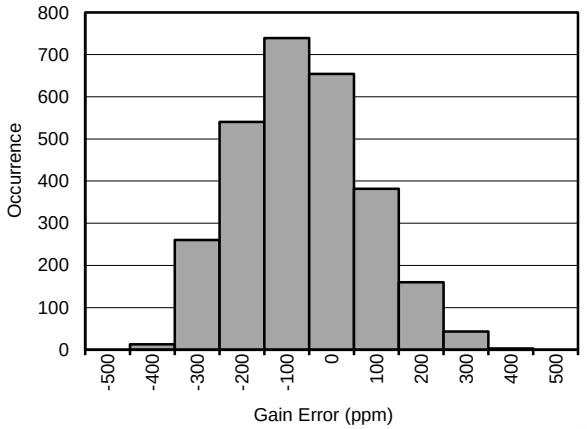


Figure 23. DIFFERENTIAL AMPLIFIER GAIN ERROR HISTOGRAM

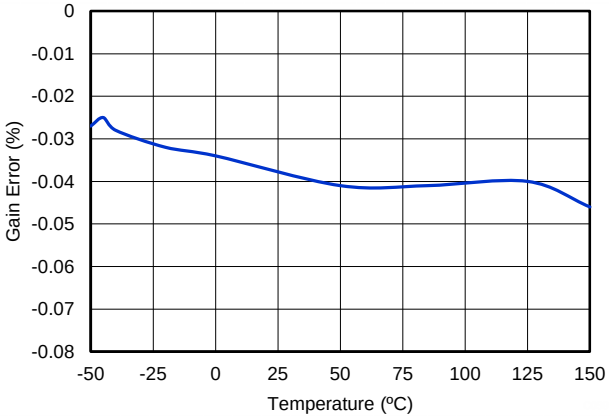


Figure 24. DIFFERENTIAL AMPLIFIER GAIN ERROR vs TEMPERATURE

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

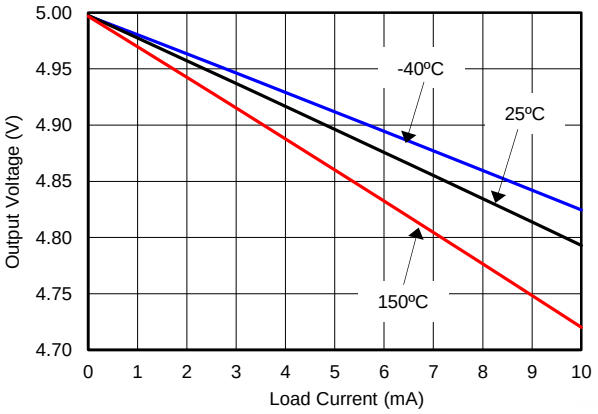


Figure 25. DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE vs OUTPUT CURRENT (POSITIVE RAIL)

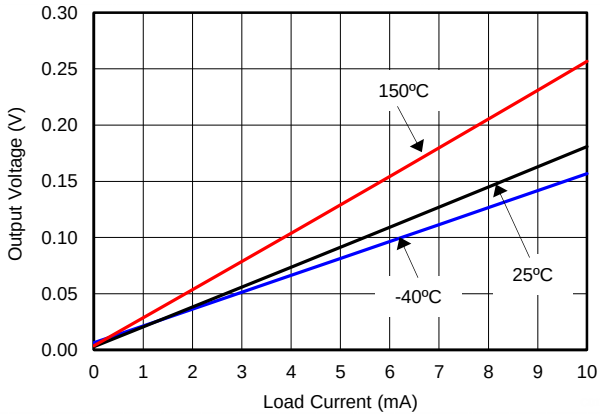


Figure 26. DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE vs OUTPUT CURRENT (NEGATIVE RAIL)

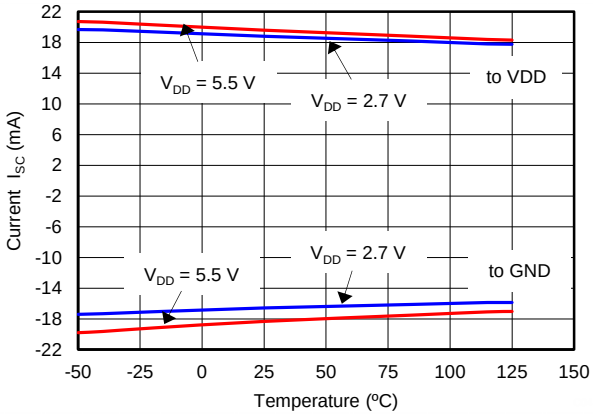


Figure 27. DIFFERENTIAL AMPLIFIER SHORT-CIRCUIT CURRENT vs TEMPERATURE

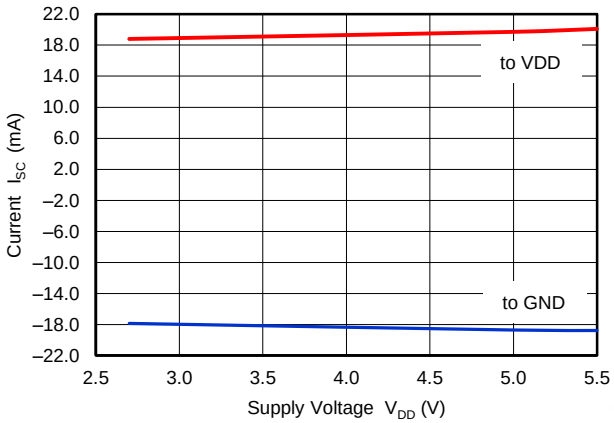


Figure 28. DIFFERENTIAL AMPLIFIER SHORT-CIRCUIT CURRENT vs POWER SUPPLY

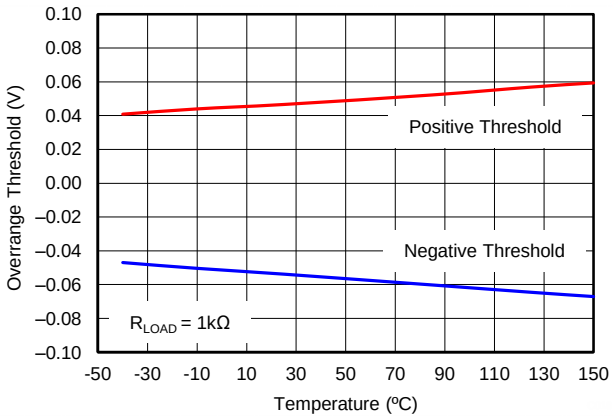


Figure 29. OVERRANGE TRIP LEVEL vs TEMPERATURE

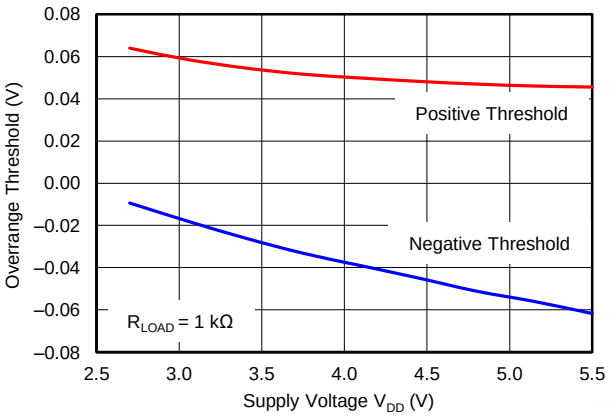


Figure 30. OVERRANGE TRIP LEVEL vs POWER SUPPLY

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

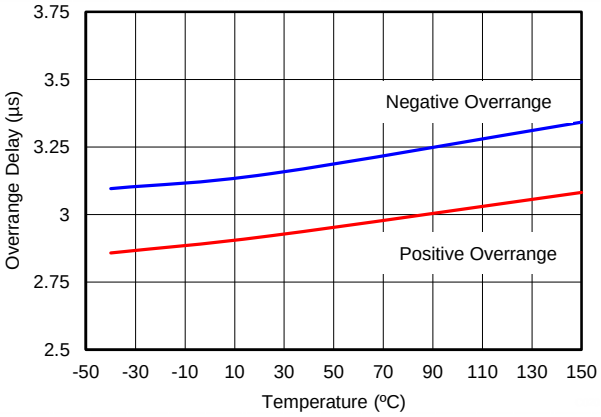


Figure 31. OVERRANGE DELAY vs TEMPERATURE

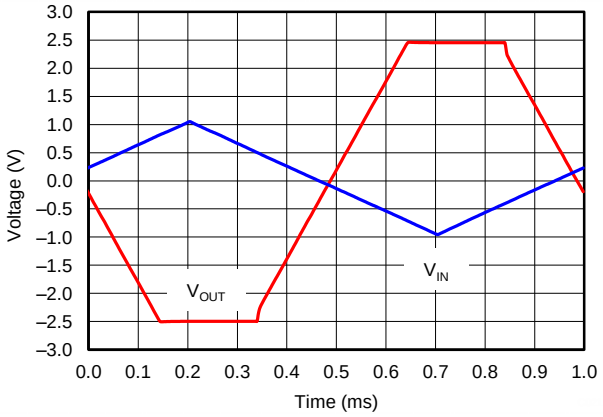


Figure 32. DIFFERENTIAL AMPLIFIER OVERLOAD RECOVERY

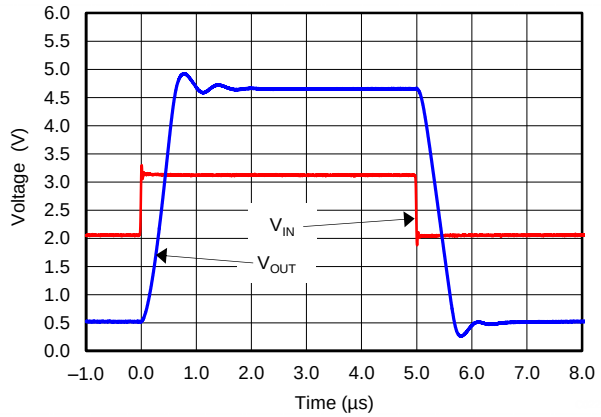


Figure 33. DIFFERENTIAL AMPLIFIER STEP RESPONSE

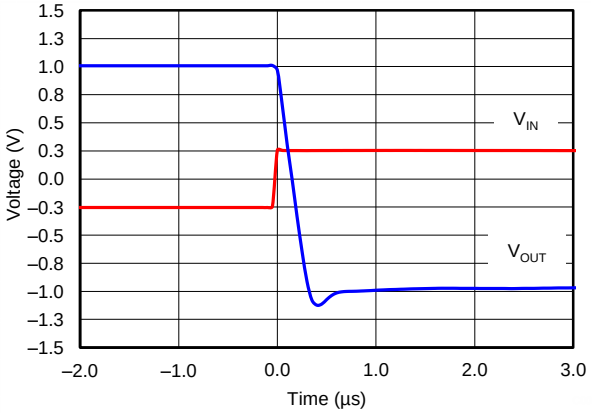


Figure 34. DIFFERENTIAL AMPLIFIER SETTLING TIME (RISING EDGE)

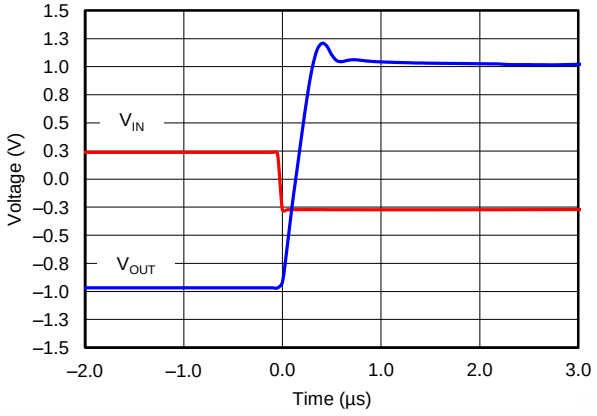


Figure 35. DIFFERENTIAL AMPLIFIER SETTLING TIME (FALLING EDGE)

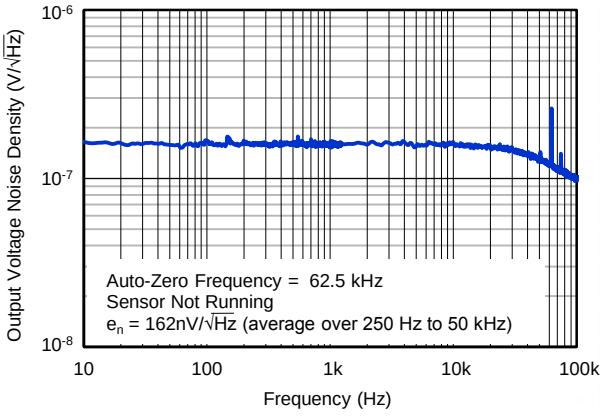


Figure 36. DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE NOISE DENSITY

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

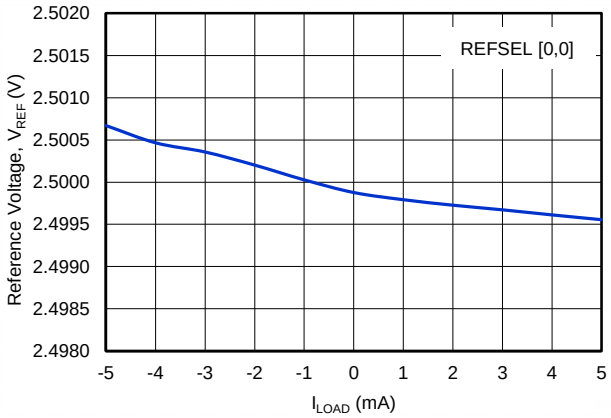


Figure 37. 2.5-V REFERENCE OUTPUT VOLTAGE vs LOAD CURRENT

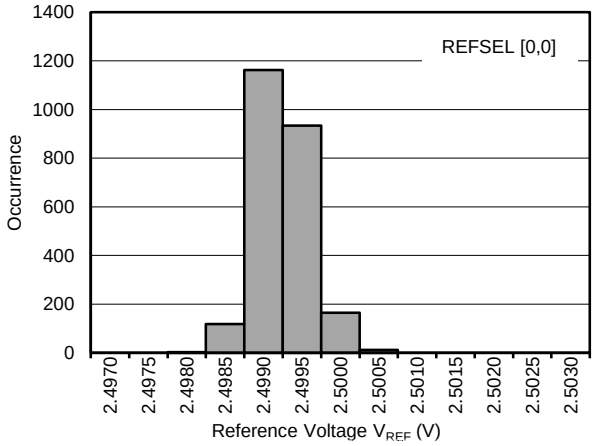


Figure 38. 2.5-V REFERENCE OUTPUT VOLTAGE HISTOGRAM

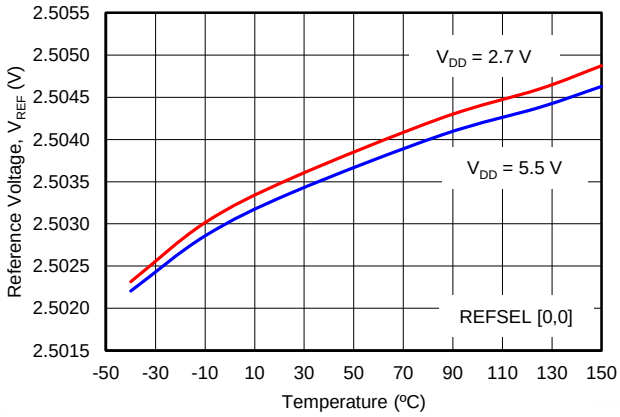


Figure 39. 2.5-V REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

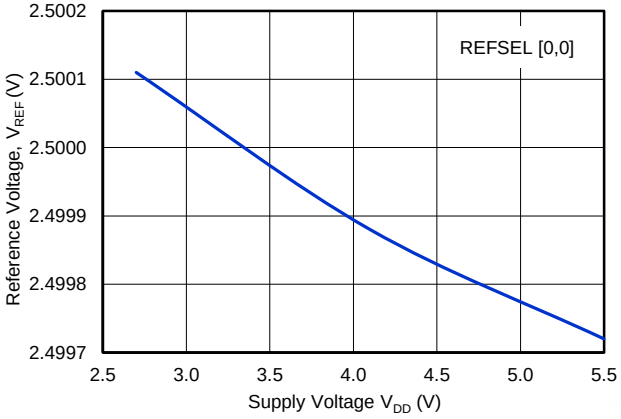


Figure 40. 2.5-V REFERENCE OUTPUT VOLTAGE vs POWER SUPPLY

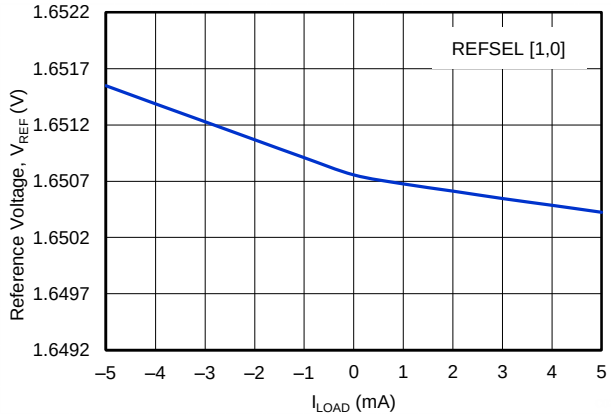


Figure 41. 1.65-V REFERENCE OUTPUT VOLTAGE vs LOAD CURRENT

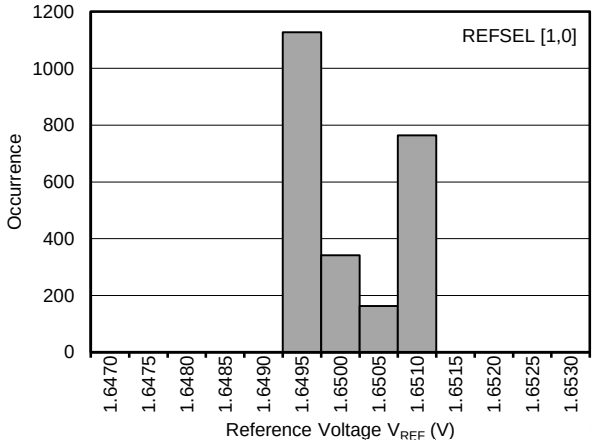


Figure 42. 1.65-V REFERENCE OUTPUT VOLTAGE HISTOGRAM

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TYPICAL CHARACTERISTICS (continued)

At V_{DD} = 5 V and T_A = +25 °C, unless otherwise noted.

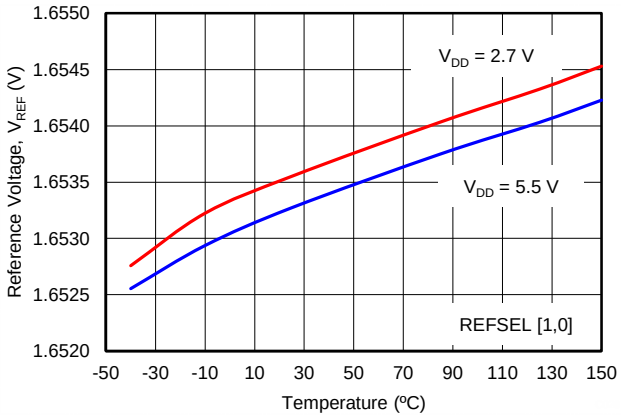


Figure 43. 1.65-V REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

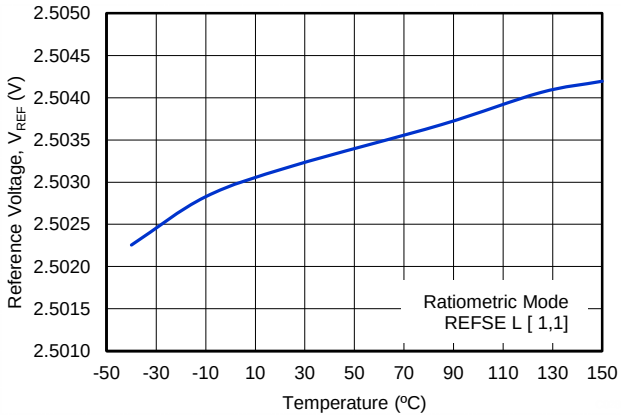


Figure 44. RATIOMETRIC REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

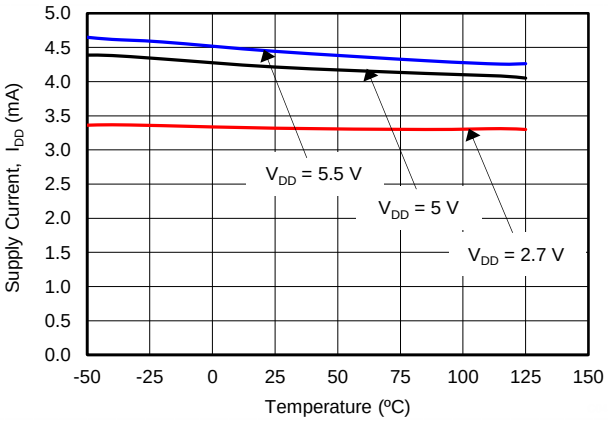


Figure 45. SUPPLY CURRENT vs TEMPERATURE

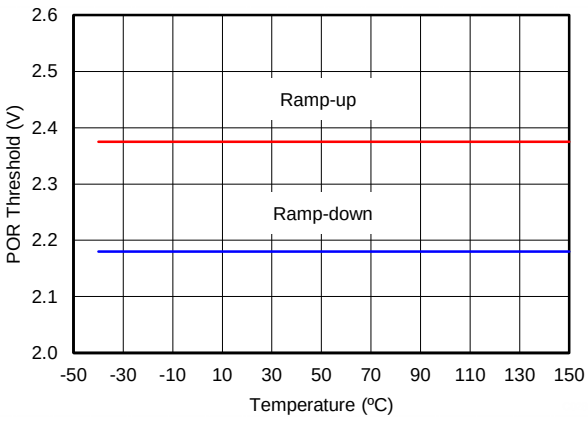


Figure 46. POWER-ON-RESET vs TEMPERATURE

FUNCTIONAL DESCRIPTION

OVERVIEW

The DRV411 is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation. The DRV411 operates from a single +2.7-V to +5.5-V supply, and provides magnetic field probe (Hall sensor) excitation, signal conditioning, and compensation-coil driver amplification. In addition, this device detects error conditions and handles overload situations. A precise differential amplifier allows translation of the compensation current into an output voltage using a small shunt resistor. A buffered voltage reference can be used for comparator, analog-to-digital converter (ADC), or bipolar zero reference voltages. Dynamic error correction ensures high dc precision over temperature and long-term accuracy.

The DRV411 uses analog signal conditioning circuitry; the internal loop filter and integrator are switched capacitor-based circuits. The DRV411 can be combined with high-precision sensors for exceptional accuracy and resolution. An internal clock and counter logic control power-up, overload detection and recovery, error, and time-out conditions. The DRV411 is built using a highly reliable CMOS process. Unique protection cells at critical connections enable the design to handle inductive energy.

HALL SENSOR INTERFACE

The DRV411 works best with symmetrical InSb Hall elements, such as the HW322 and HW302 from AKM or other vendors. Symmetrical Hall elements are Hall elements where input impedance and output impedance are closely matched. However, hall elements suffer from offset and offset drift across temperature that affects the accuracy and linearity of the current sensor. The DRV411 contains patented excitation and conditioning circuitry that significantly reduces offset and offset drift. The excitation circuit regulates the voltage across the hall element to a maximum voltage of 0.95 V. This voltage is very stable across the full temperature range. The excitation current varies with temperature in order to keep the hall sensitivity constant. A special current limiting circuit limits the current delivered to the hall element to a maximum current of 10 mA regardless of the temperature or the impedance of the hall element.

DYNAMIC OFFSET AND NOISE CANCELLATION USING SPINNING CURRENT METHOD

The DRV411 incorporates dynamic offset cancellation circuitry that helps eliminate offset drift and 1/f noise of the hall sensor. The excitation current is spun through the hall sensor in orthogonal directions at a fixed clock frequency using rotation multiplexer switches, as shown in Figure 47 (a) to (d). The excitation source ensures a constant current during each spin cycle but keeps the sensitivity of the hall sensor independent by varying the current across temperature for impedance variations from 100 Ω to 2 kΩ. The corresponding Hall output is averaged across the four orthogonal directions to effectively cancel the Hall offset and the 1/f noise. The DRV411 continuously monitors the offset of the Hall element and triggers an error flag if the offset remains > 50 mV as a result of any damage to the Hall sensor. Refer to the *Error Conditions* section for more details.

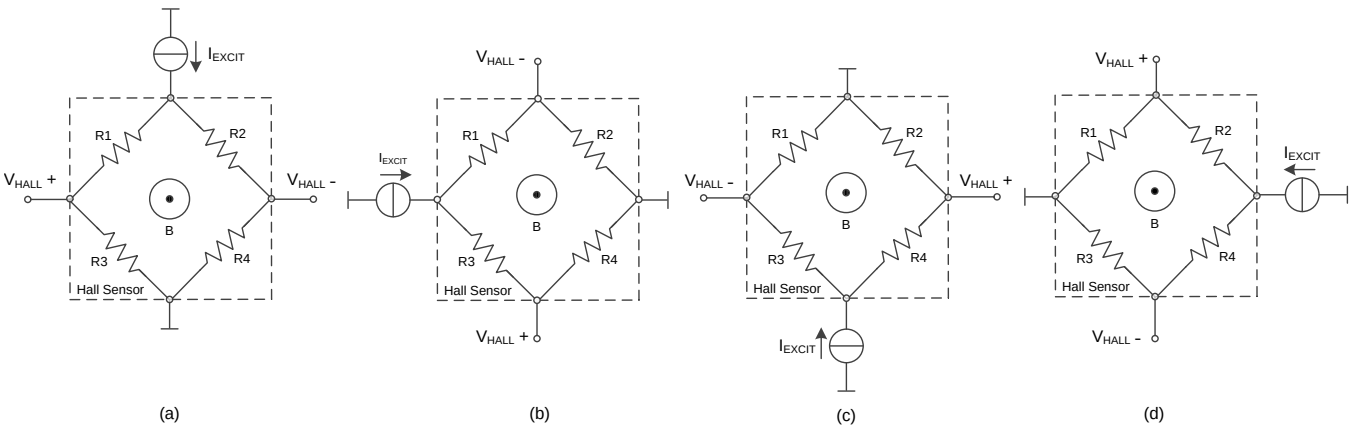


Figure 47. Hall Sensor Current Spinning Method

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Low-frequency noise can be a concern for Hall sensors with constant voltage and current excitation. The dynamic offset cancellation technique eliminates 1/f noise from the Hall sensor. Figure 48 shows the effect of current spinning on the Hall sensor, referred to primary current noise.

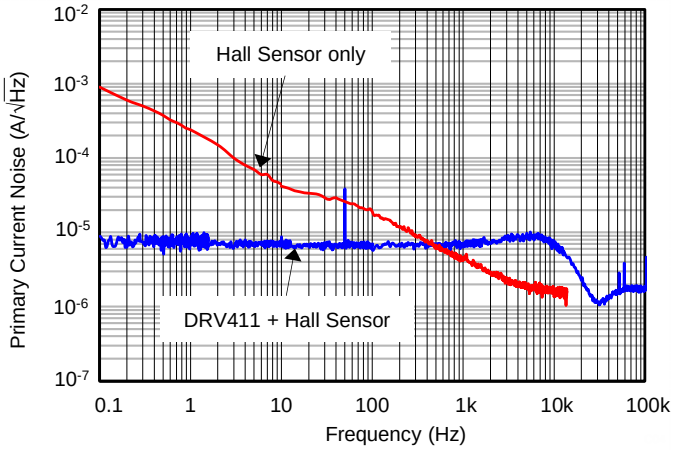


Figure 48. Effect of Noise Cancellation with Current Spinning

COMPENSATION COIL DRIVER

The compensation coil driver provides the driving current for the compensation coil. A fully differential driver stage offers the high-signal voltage to overcome the wire resistance of the coil with only a 5-V supply. The compensation coil is connected between ICOMP1 and ICOMP2, both generating an analog voltage across the coil (see Figure 51) that turns into current from the wire resistance (and eventually from the inductance). The compensation current represents the primary current transformed by the turns ratio. A shunt resistor is connected in this loop and the high precision differential amplifier translates the voltage from this shunt to an output voltage (see the *Functional Principle of Closed-Loop Current Sensors with a Hall Sensor* section).

Both compensation driver outputs provide low impedance over a wide frequency range that insures smooth transition between the closed-loop compensation frequency range and the high-frequency range, where the primary winding directly couples the primary current into the compensation coil according to the winding ratio (transformer effect).

The two compensation driver outputs are specially protected to handle inductive energy. However, it might be necessary to use high-current sensors to add external protection diodes (see the *Protection Recommendations* section).

GAIN SELECTION AND COMPENSATION FREQUENCY

Proper selection of the GSEL mode enables the sensor designer to create a sensor with stable gain over a wide frequency range and excellent loop stability. Modes Gain_1 to Gain_3 allow for different fixed gain and zero-frequency options to be selected according to the requirements of the individual sensor. See Table 1 for more information. Evaluate Gain_3 mode (GSEL [1,0]) first because it works with most common sensors.

Mode Selection

Gain_1 Mode For use with sensors with compensation coil inductance < 50 mH.

Gain_2 Mode For use with sensors with very small form factor (small core diameter), where the transformer effect starts to dominate the transfer function at frequencies significantly above 3.8 kHz. Typically the inductance of the compensation coil would be very small.

Gain_3 Mode Works well with a wide selection of sensors with compensation coil inductance typically ≥ 50 mH.

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Table 1. Gain Setting and Compensation Frequency

MODE	GSEL1	GSEL2	DESCRIPTION
Gain_1	0	0	G = 250 V/V. Compensation frequency set to 3.8 kHz.
Gain_2	0	1	G = 250 V/V. Compensation frequency set to 7.2 kHz.
Gain_3	1	0	G = 1000 V/V. Compensation frequency set to 3.8 kHz.
External gain and compensation (op-amp mode)	1	1	Current spinning and front-end chopping are turned off. Constant voltage excitation is enabled. Gain and compensation set by using external resistors and capacitors, such as in discrete designs.

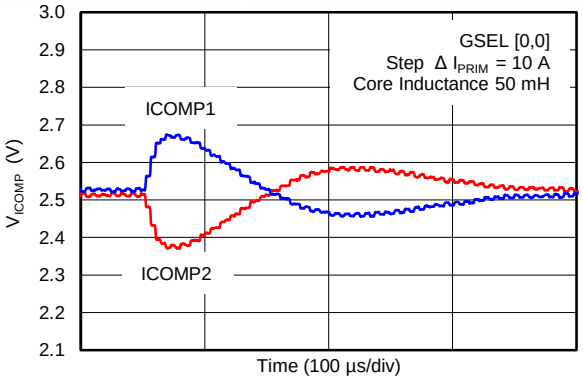


Figure 49. Settling of ICOMP1 and ICOMP2 (Mode Gain_1)

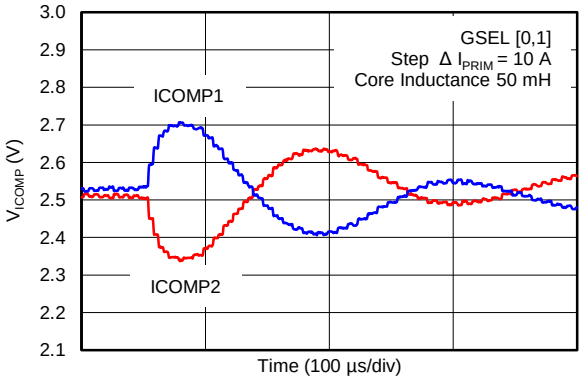


Figure 50. Settling of ICOMP1 and ICOMP2 (Mode Gain_2)

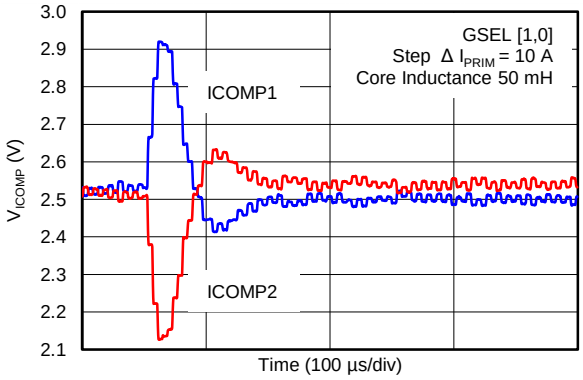


Figure 51. Settling of ICOMP1 and ICOMP2 (Mode Gain_3)

Along with symmetrical InSb Hall elements, the DRV411 can also be connected to symmetrical GaAs Hall elements. The advantage of GaAs Hall elements is that they provide an extended temperature range to +125°C. See the following section, *External Gain and Compensation (Op-amp Mode)* for more details. This type of Hall element has a lower sensitivity than InSb-type sensors. In order to compensate for this difference, TI recommends using gain setting mode Gain_3 with GaAs sensors. If the sensitivity is too low and the loop gain is insufficient, the loop can become unstable. In op-amp mode, gain can be set with external components.

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EXTERNAL GAIN AND COMPENSATION (OP-AMP MODE)

Op-amp mode allows several degrees of freedom for the sensor designer. In op-amp mode, the DRV411 functions like a conventional operation amplifier with high open loop gain (> 100 dB). The internal compensation is disconnected, so that the sensor gain and compensation can be set externally. The DRV411 still provides a stable excitation voltage of 0.74 V between terminals HALL1 and HALL3. The outputs of the Hall sensor must be connected to terminal HALL2 and HALL4. The maximum current is limited to 10 mA to protect the Hall element. The following list shows some ways to use op-amp mode:

- Op-amp mode can be used in cases where modes Gain_1 to Gain_3 do not lead to an acceptable frequency response from the sensor module. In this mode, external compensation must be designed in to suit the sensor requirements (see Figure 57).
- DRV411 can be used with symmetrical GaAs Hall sensors. However, because of the inherently low sensitivity of GaAs sensors, the internal gain (compensation) may not be sufficient. In such cases, use op-amp mode to make the system stable with external compensation. In op-amp mode, the excitation circuit provides a constant 0.74 V across the HALL1 and HALL3 outputs, with HALL3 referred to GND. Connect the Hall outputs to the HALL2 and HALL4 pins (see Figure 57). For Hall sensors with large input impedances, do not exceed the common-mode input range of the op-amp inputs (see the Electrical Characteristics section).
- Op-amp mode can also be used for interfacing to nonsymmetrical Hall elements, which are Hall elements where the input impedance and output impedance are not equal. Different Hall sensor input and output impedances lead to very large sensor offsets that might be outside the correction range of the DRV411 excitation circuit. In this mode, the ERROR pin is disabled (see the *Error Conditions* for more details). For Hall sensors with large input impedances, do not exceed the common-mode input range of the op amp inputs.
- If an external excitation circuit is required for the Hall sensor in op-amp mode, bypass the internal sensor by ignoring the HALL1 and HALL3 terminals. Connect the Hall sensor outputs to the HALL2 and HALL4 terminals. For Hall sensors with large input impedances, do not exceed the common-mode input range of the op amp inputs.

SHUNT SENSE AMPLIFIER

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal resistors.

For gains of 4 V/V:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3}$$

where:

- $R_2 / R_1 = R_4 / R_3 = 4$
- $R_5 = R_{SHUNT} \times 4$ (1)

Both inputs of the differential amplifier are normally connected to the current shunt resistor. This resistor adds to the internal 10-kΩ resistor, slightly reducing the gain in this signal path. For best common-mode rejection (CMR), a dummy shunt resistor (R_5 = 4 x R_{SHUNT}) is placed in series with the REF_{IN} pin to restore matching of both resistor dividers; see Figure 52.

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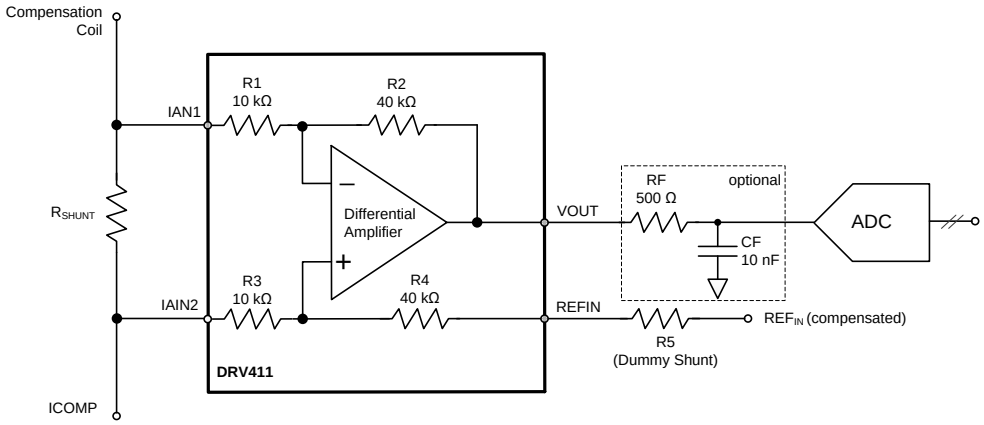


Figure 52. Internal Difference Amplifier with Example of a Decoupling Filter

Typically, the gain error resulting from the resistance of R_{SHUNT} is negligible; for 70 dB of common-mode rejection, however, the match of both divider ratios must be higher than 1/3000.

The amplifier output can drive close to the supply rails, and is designed to drive the input of a SAR-type ADC; adding an RC low-pass filter stage between the DRV411 and the ADC is recommended. This filter not only limits the signal bandwidth but also decouples the high-frequency component of the converter input sampling noise from the amplifier output. For R_F and C_F values, refer to the specific converter recommendations in the respective product data sheet. Empirical evaluation may be necessary to obtain optimum results.

The output drives 100 pF directly and shows 50% overshoot with approximately 1-nF capacitance. Adding R_F allows for much larger capacitive loads. Note that with an R_F of only 20 Ω, the load capacitor must be either less than 1 nF or more than 33 nF to avoid overshoot; with an R_F of 50 Ω, this transient area is avoided.

The reference input (REFIN) is the reference node for the exact output signal (VOUT). Connecting REFIN to the reference output (REFOUT) results in a live zero reference voltage that is user-selectable. Use the same reference for REFIN and the ADC to avoid mismatch errors that exist between the two reference sources.

OVERRANGE COMPARATOR

High peak current can overload the differential amplifier connected to the shunt. The OR pin, an open-drain output, indicates an overvoltage condition for the differential amplifier by pulling low. The output of this flag is suppressed for 3 µs, preventing unwanted triggering from transients and noise. This pin returns to high as soon as the overload condition is removed (an external pull-up is required to return the pin high).

This error flag not only provides a warning about a signal-clipping condition, but is also a window comparator output for actively shutting off circuits in the system. The value of the shunt resistor defines the operating window for the current and sets the ratio between the nominal signal and the trip level of the overrange flag. The trip current of this window comparator is calculated using the following example:

With a 5-V supply, the output voltage swing is approximately ±2.45 V (load and supply voltage-dependent).

The gain of 4 V/V enables an input swing of ±0.6125 V.

Thus, the clipping current is IMAX = 0.6125 V / R_{SHUNT}.

See Figure 13 and Figure 14 in the *Typical Characteristics* section for details.

The overrange condition is internally detected as soon as the amplifier exceeds its linear operating range, not just a preset voltage level. Therefore, the error of the overrange comparator level is reliably indicated in fault conditions such as output shorts, low load, or low-supply conditions. As soon as the output cannot drive the voltage higher, the flag is activated. This configuration is a safety improvement over a voltage-level comparator.

Note that the internal resistance of the compensation coil may prevent high compensation current from flowing because of ICOMP driver overload. Therefore, the differential amplifier may not overload with this current. However, a fast rate of change of the primary current is transmitted through transformer action and safely triggers the overload flag.

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VOLTAGE REFERENCE

The precision reference circuit offers low drift (typically 5 ppm/K) and is used for internal biasing; it is also connected to the REFOUT pin. The circuit is intended as the reference point of the output signal to allow a bipolar signal around it. This output is buffered for low impedance and tolerates sink and source currents of ±5 mA. Capacitive loads can be directly connected, but generate ringing on fast load transients. A small series resistor of a few ohms improves the response, especially for a capacitive load in the range of 1 µF.

Reference Output Voltage Selection

As shown in Table 2, the most common use-cases for the DRV411 are with 5-V and 3.3-V power supplies, where the sensor output must be centered at 2.5 V and 1.65 V, respectively. The internal reference provides very good accuracy and drift performance. See the *Electrical Characteristics* for detailed information.

Table 2. Reference Output Voltage Selection

MODE	REFSEL1	REFSEL2	DESCRIPTION
REF = 2.5 V	0	0	Used with sensor module supply of 5 V
REF = 1.65 V	1	0	Used with sensor module supply of 3.3 V
Ratiometric output	1	1	Provides output centered on V_S / 2

In the ratiometric output mode, the reference is bypassed and the power supply is divided by two. The internal resistor divider offers very tight tolerances and a temperature coefficient of less than 10 ppm/°C. In this case, the sensor module output is centered on V_S / 2.

For sensor modules with a reference pin, the DRV411 also allows overwriting the internal reference with an external reference voltage, as shown in Figure 53. When an external reference that has a significant voltage difference compared to the internal reference is connected, resistor R_5 limits the current flowing from the internal reference. In this case, the internal reference sources the current shown in Equation 2:

$$I_{int_ref} = \frac{V_{int_ref} - V_{ext_ref}}{600\ \Omega} \quad (2)$$

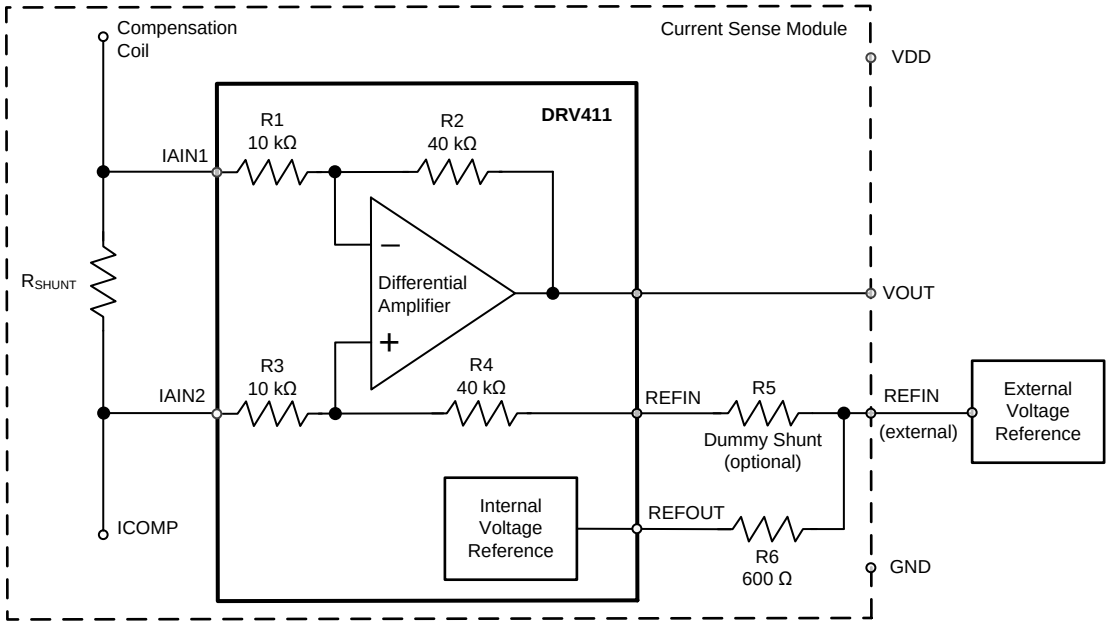


Figure 53. DRV411 with External Reference

The example of 600 Ω for R6 was chosen for illustration purposes; different values are possible. Note that if no external reference is connected, R6 has little impact on the common-mode rejection of the differential amplifier, and therefore, should be as small as possible.

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POWER-ON STARTUP AND BROWNOUT

Power-on is detected when the supply voltage exceeds 2.4 V at VDD. At this point, digital logic starts up and waits for 100 µs for the excitation source to settle to its final value. During this period, ICOMP1 and ICOMP2 outputs are pulled low, so that there is no undesired signal drive on the compensation coil. Also, the error conditions are suppressed and the ERROR pin is asserted low for 100 µs. This ensures that the excitation voltage has reached the final level and there is no false error triggered on the output. The output on the VOUT terminal is only valid 100 µs after power-on reset.

The DRV411 tests for low supply voltages with a brownout voltage level of +2.4 V. Good power-supply and low ESR bypass capacitors are required to maintain the supply voltage during the large current pulses driven by the DRV411. Supply voltage drops below the brown-out level lasting less than 25 µs are ignored. A supply drop lasting longer than 25 µs generates power-on reset. A voltage dip on VDD down to +1.8 V also initiates a power-on reset. After the power supply returns to 2.4 V (see the power-on reset threshold parameter in the Electrical Characteristics), the device initiates a startup cycle as previously described.

ERROR CONDITIONS

In addition to the overrange flag that indicates signal clipping in the output amplifier (differential amplifier), a system error flag is provided. The error flag indicates conditions when the output voltage does not represent the primary current. The error flag is active during a power fail or brown-out, or when the Hall sensor offset becomes greater than 50 mV, which usually means that the Hall sensor is not functioning within its normal operating range. The error flag also goes active with an open circuit in the Hall sensor connection. As soon as the error condition is no longer present and the circuit has returned to normal operation, the flag resets.

Both the error and overrange flags are open-drain logic outputs. They can be connected together for a wired-OR, and require an external pull-up resistor for proper operation.

The following conditions result in error flag activation (ERROR asserts low):

1. For 100 µs from power-up, or if a supply-voltage low (brown-out) condition lasts for more than 25 µs. Recovery is the same as power-up.
2. If the Hall sensor offset becomes greater than 50 mV.
3. If one or more of the Hall sensor terminals is disconnected.

PROTECTION RECOMMENDATIONS

The inputs IAIN1 and IAIN2 require external protection to limit the voltage swing below 6 V of the supply voltage. Driver outputs ICOMP1 and ICOMP2 can handle high-current pulses protected by internal clamp circuits to the supply voltage. If large magnitude overcurrents are expected, it is highly recommended to connect external Schottky diodes to the supply rails. This external protection prevents current flowing into the die and destroying the circuitry.

All other pins offer standard protection; see the *Absolute Maximum Ratings* table.

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APPLICATION INFORMATION

FUNCTIONAL PRINCIPLE OF CLOSED-LOOP CURRENT SENSORS WITH A HALL SENSOR

Closed-loop current sensors measure currents over wide frequency ranges, including dc currents. These types of devices offer a contact-free method, as well as excellent galvanic isolation performance combined with high resolution, accuracy, and reliability. At dc and in low-frequency ranges, the magnetic field induced from the current in the primary winding is compensated by a current driven through a compensation coil. A magnetic field probe (Hall sensor) located in the magnetic core loop detects the magnetic flux. This probe delivers the signal to the signal conditioning circuitry that drives the current through the compensation coil, bringing the magnetic flux back to zero. This compensation current is proportional to the primary current, relative to the winding ratio.

In higher frequency ranges, the compensation winding acts as the secondary winding in the current transformer, while the H-bridge compensation driver is rolled off and provides low output impedance.

A difference amplifier senses the voltage across a small shunt resistor that is connected to the compensation loop. This difference amplifier generates the output voltage that is proportional to the primary current. Figure Figure 54 shows the principle of a closed-loop current sensor.

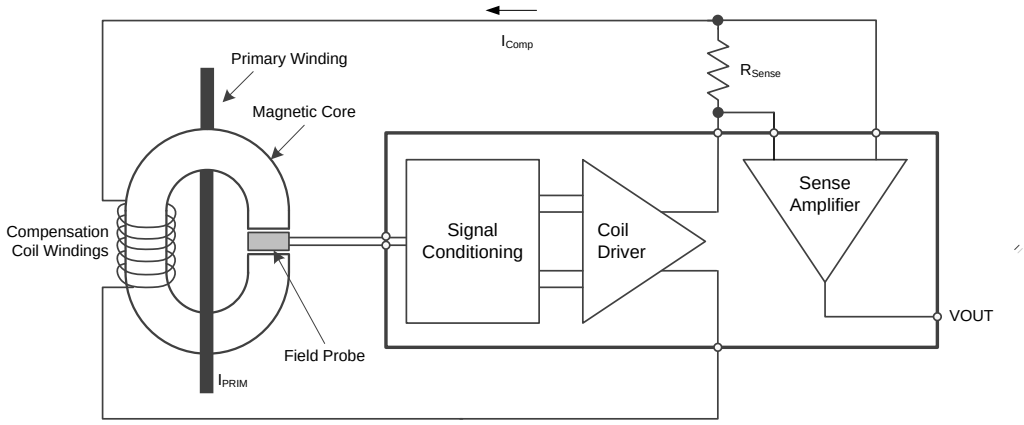


Figure 54. Principle of a Closed-Loop Current Sensor

USING DRV411 IN ±15-V SENSOR APPLICATIONS

To take advantage of the current spinning architecture for ±15-V sensor modules, the application circuit shown in Figure 55 can be used. The DRV411 max supply voltage is 5.5 V; therefore, the ±15V supplies must be externally regulated to less than 5.5 V across the power supply pins of the DRV411. In addition, an external power driver stage must be implemented that then drives the compensation coil. These techniques allow the design of exceptionally precise and stable ±15-V current-sense modules.

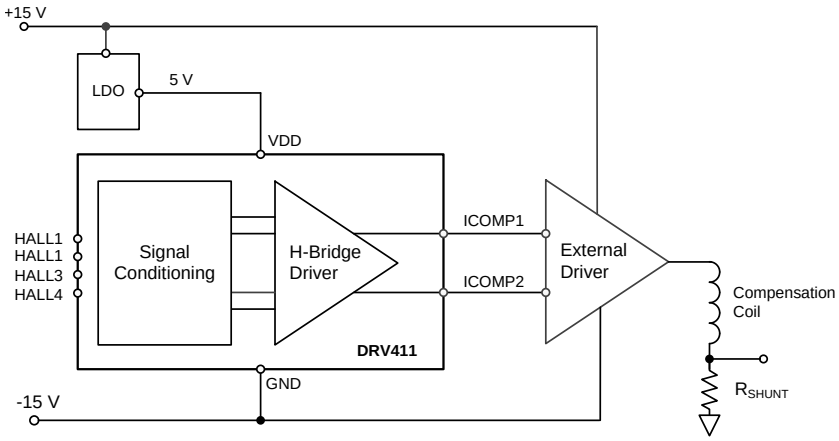


Figure 55. DRV411 Application Example: ±15-V Sensor Modules

ADDITIONAL APPLICATION EXAMPLES

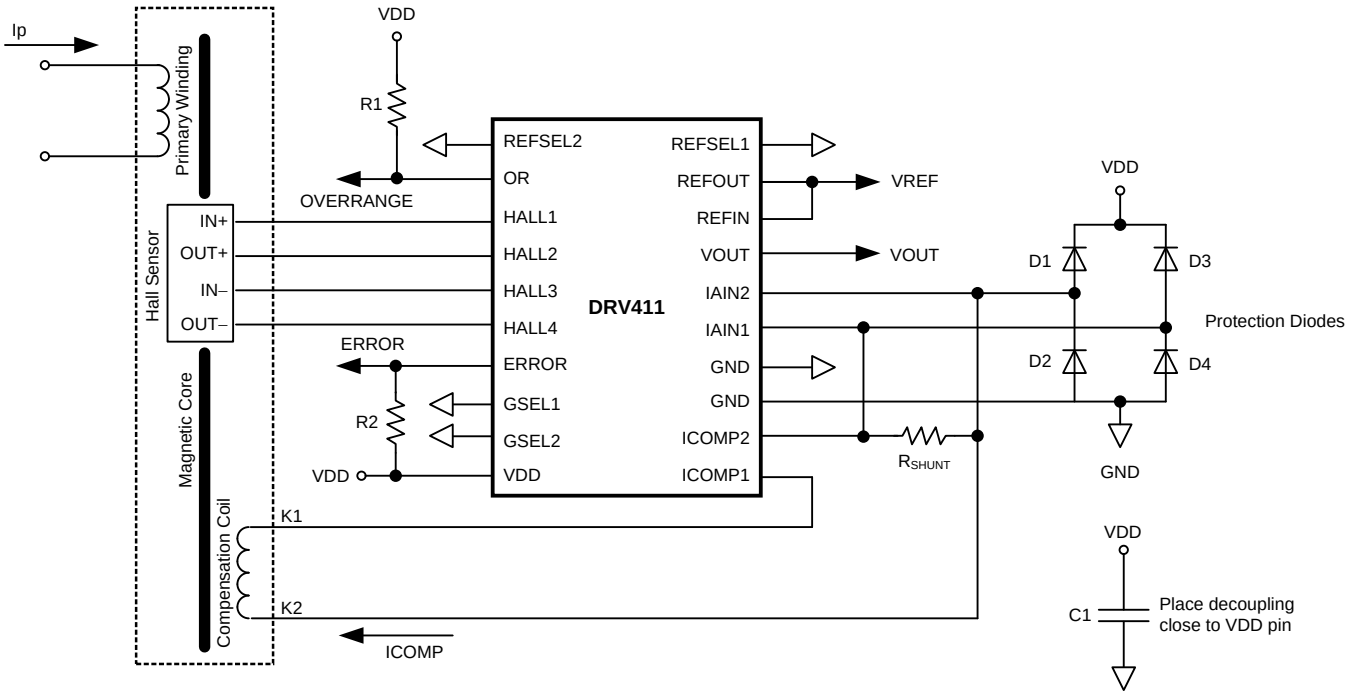


Figure 56. Typical Application Example with Gain_1 Setting (see Table 1)

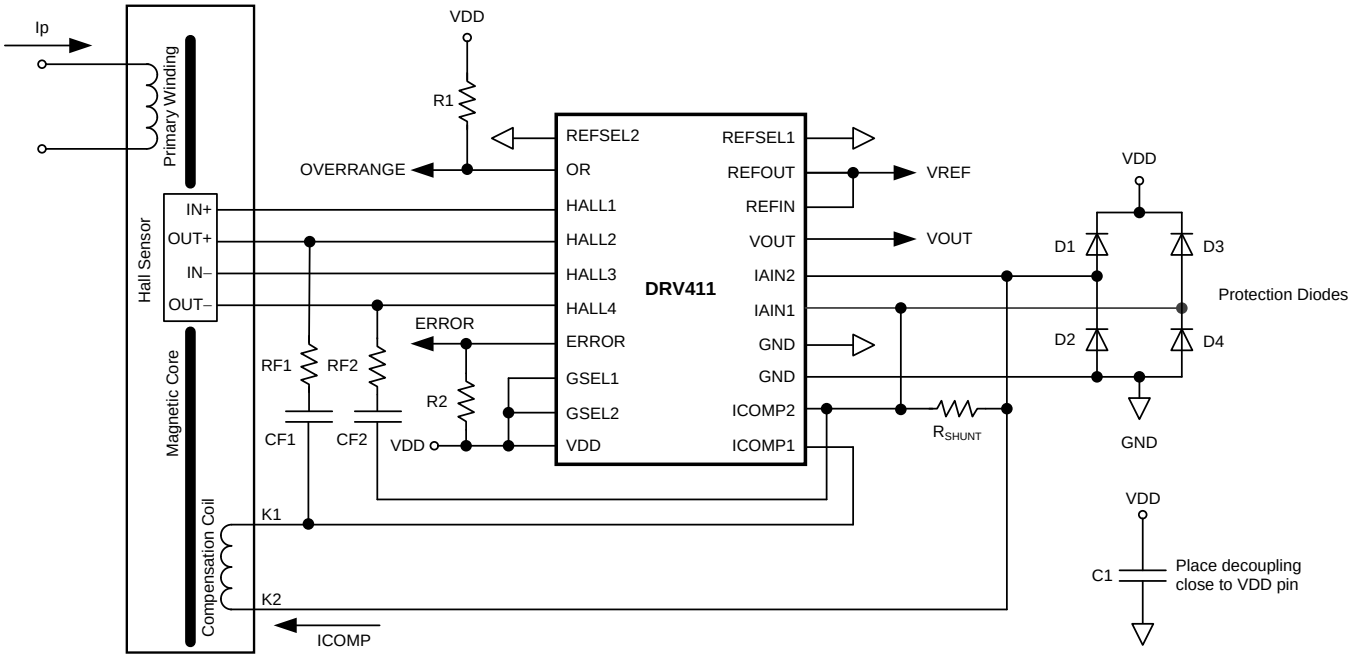


Figure 57. Application Example with External Gain and Compensation Setting (GSEL1 and GSEL2 set High), No Current Spinning

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LAYOUT CONSIDERATIONS

The DRV411 operates with relatively large currents and offers wide bandwidth. It is often exposed to large distortion energy from the primary signal and from the environment. Therefore, the wiring layout must provide shielding and low impedance connections between critical points. Power-supply decoupling requires low-ESR capacitors, and eventually a combination of a 4.7-nF NP0-type capacitor and a second capacitor of 1 µF or larger. Use low-impedance tracks to connect the capacitors to the pins. Avoid plated through-hole connectors; use multiple plated through-holes instead. The ground (GND) should be connected to a local ground plane. Best supply decoupling is achieved with ferrite beads in series to the main supply. The ferrite beads decouple the DRV411, and thus reduce interaction with other circuits powered from the same supply voltage source.

The reference output (REFOUT) is referred to GND. A low-impedance and star-type connection is required to avoid the driver current and the probe current modulating the voltage drop on the ground track. The REFOUT and VOUT outputs can drive some capacitive load, but avoid large direct capacitive loading because it increases internal pulse currents. Given the wide bandwidth of the differential amplifier, isolate large capacitive loads with a small series resistor. Using a small capacitor of some pF improves the transient response on high resistive loads.

The exposed thermal pad, or PowerPAD, on the bottom of the package must be soldered to GND because it is internally connected to the substrate that must be connected to the most negative potential.

POWER DISSIPATION

The use of the thermally-enhanced PowerPAD SOIC and QFN packages dramatically reduces the thermal impedance from junction to case. These packages are constructed using a down-set lead frame that the die is mounted on. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. The PowerPAD has direct thermal contact with the die; therefore, excellent thermal performance can be achieved as a result of providing a good thermal path away from the thermal pad.

The two outputs, ICOMP1 and ICOMP2, are linear outputs, and therefore the power dissipation on each output is proportional to the current multiplied by the internal voltage drop on the active transistor. For ICOMP1 and ICOMP2, it is the voltage drop to VDD or GND according to the current-conducting side of the output.

CAUTION

Output short-circuit conditions are particularly critical for the ICOMP driver because the full supply voltage can be seen across the conducting transistor and the current is not limited other than by the current density limitation of the FET; permanent damage can occur. The DRV411 does not feature temperature protection or thermal shut-down.

Thermal Pad

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences the overall heat dissipation. Technical details are described in Application Report SLMA002, *PowerPad Thermally Enhanced Package,* available for download at www.ti.com.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in this version.

Changes from Revision A (August 2013) to Revision B **Page**

- Changed ESD parameter in Absolute Maximum Ratings table: deleted first human body model row, added machine model row 2
- Changed Hall Element Excitation, *Error comparator threshold* parameter typical specification in Electrical Characteristics table 3
- Changed Voltage Reference, *PSRR* parameter: added second row to PSRR parameter, added RGP package to test conditions of first row 4
- Changed Digital Input/Output, V_{OL} and V_{OH} parameters: swapped symbols and parameter names 4
- Changed Figure 15 8
- Changed Figure 36: changed units in y-axis 11
- Changed last paragraph of *Gain Selection and Compensation Frequency* section 16

Changes from Original (August 2013) to Revision A **Page**

- Changed Figure 14 to show correct image 8
- Changed Figure 25 to show correct image 10
- Changed Figure 34 to show correct image 11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV411AIPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV411	Samples
DRV411AIPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV411	Samples
DRV411AIRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV411	Samples
DRV411AIRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV411	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

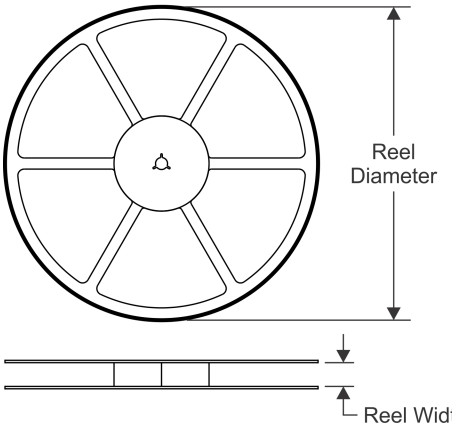
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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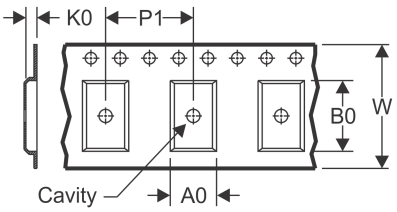
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

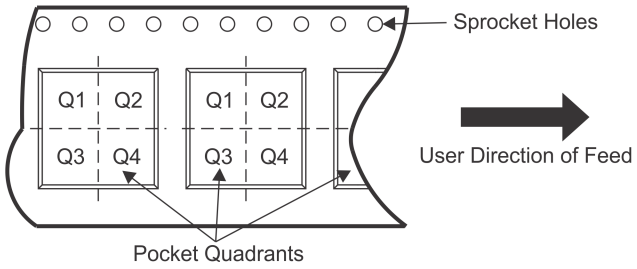


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

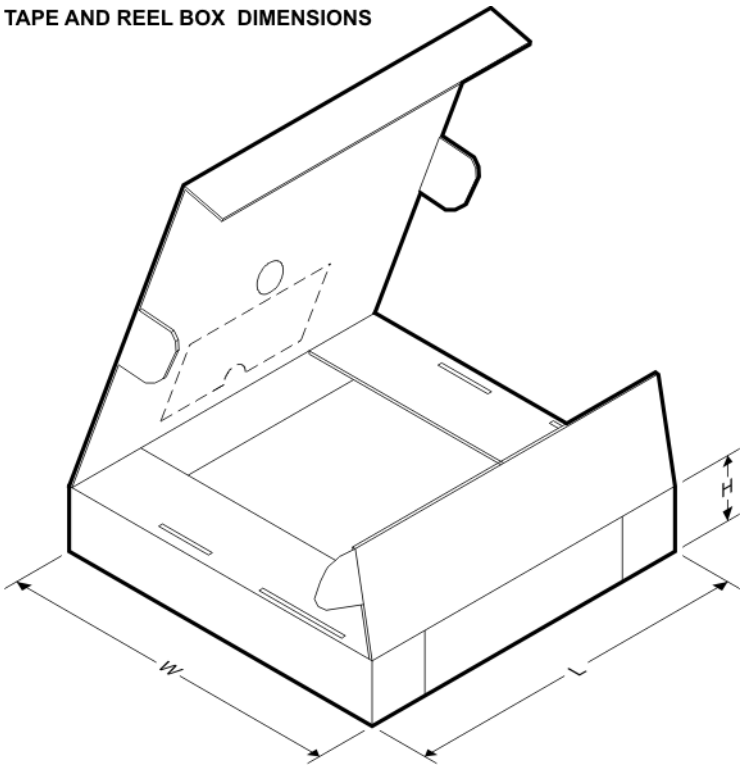
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV411AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
DRV411AIRGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV411AIRGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

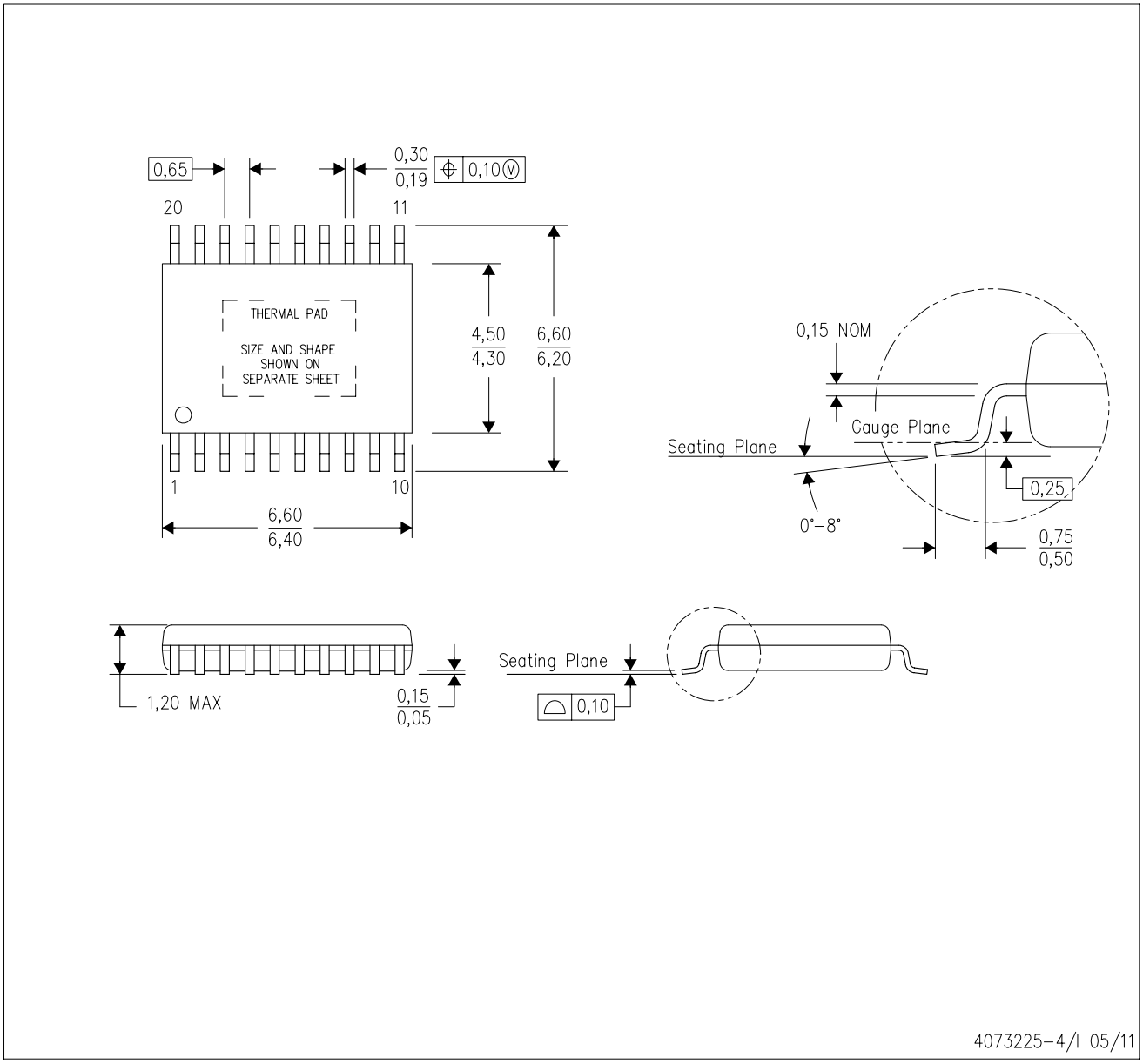
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV411AIPWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0
DRV411AIRGPR	QFN	RGP	20	3000	367.0	367.0	35.0
DRV411AIRGPT	QFN	RGP	20	250	210.0	185.0	35.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

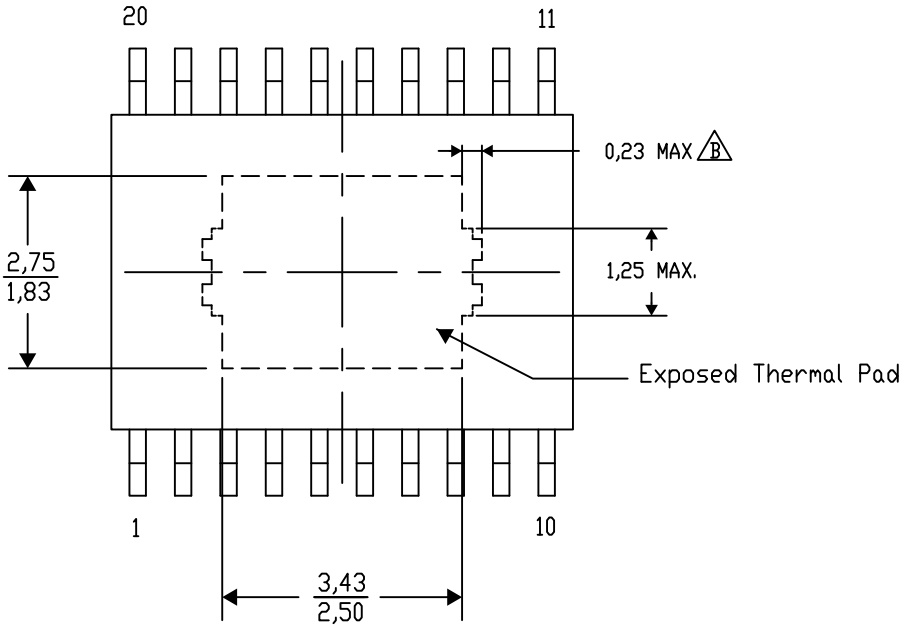
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

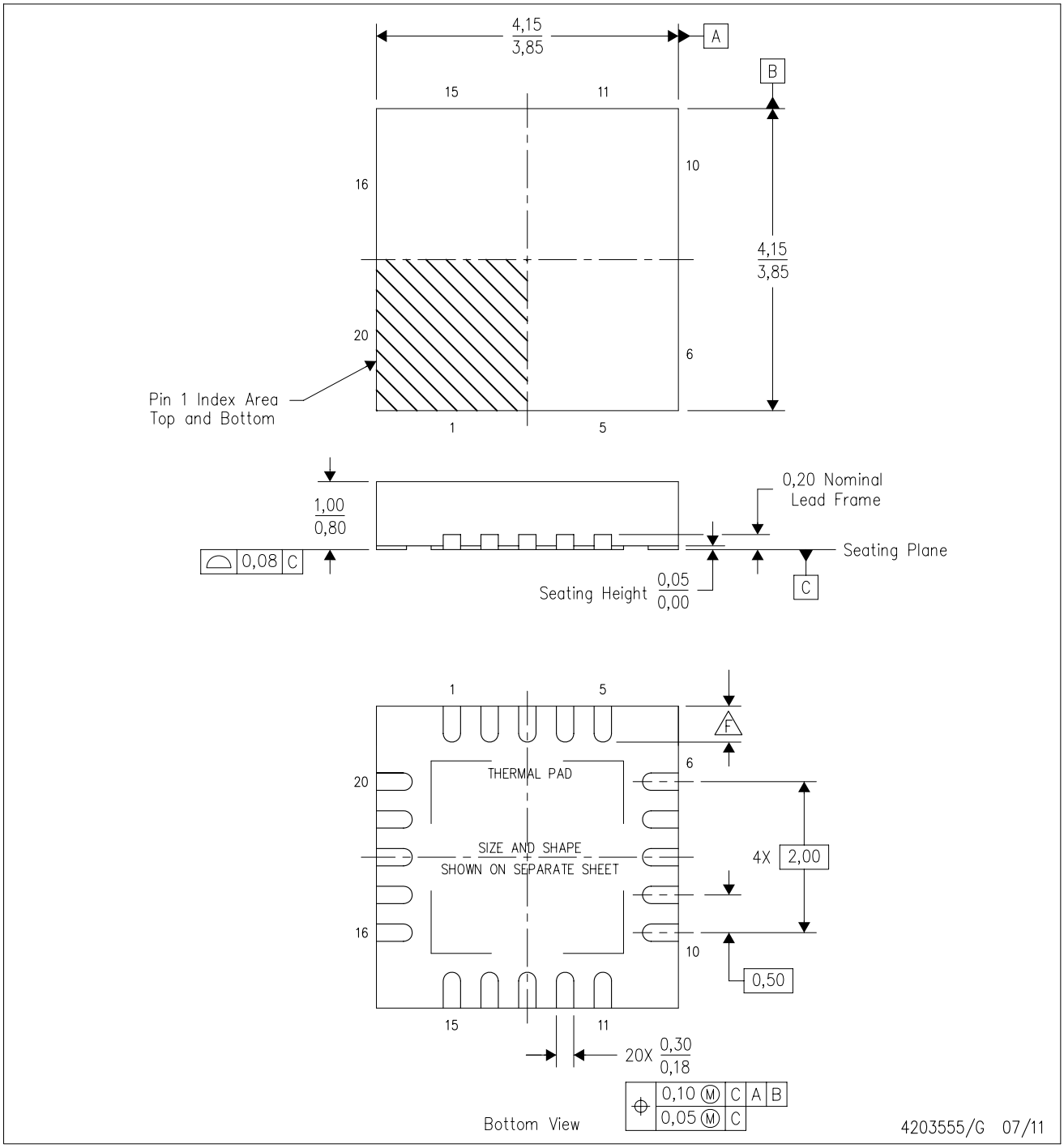
4206332–41/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

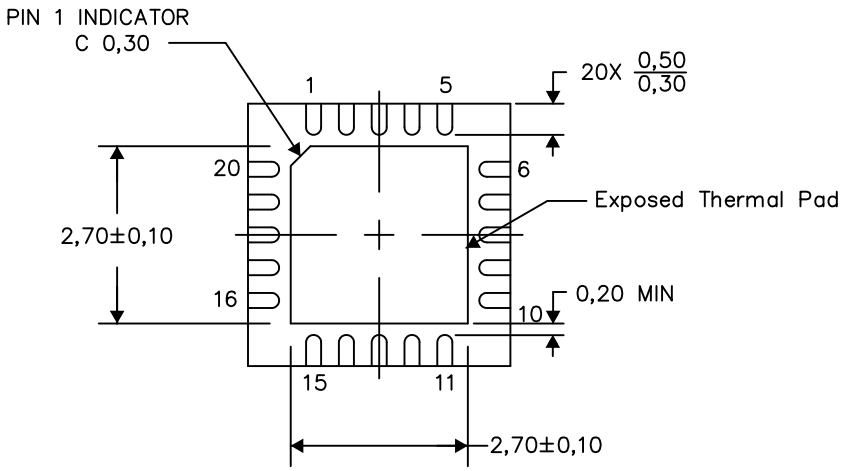
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



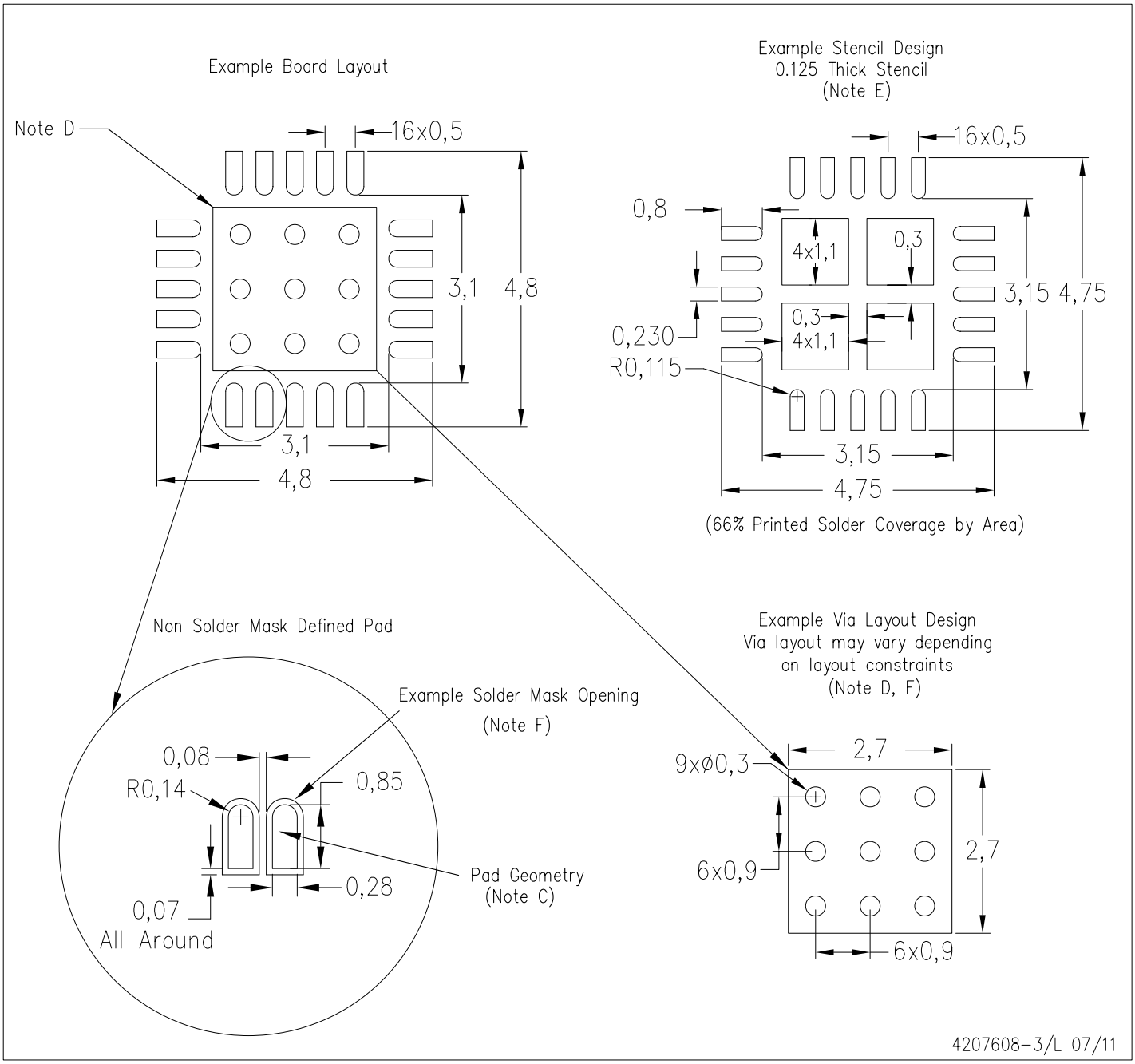
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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