Platform Flash In-System Programmable Configuration PROMs

DS123 (v2.18) May 19, 2010 **Product Specification**

Features

- In-System Programmable PROMs for Configuration of Xilinx® FPGAs
- Low-Power Advanced CMOS NOR Flash Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Industrial Temperature Range (–40°C to +85°C)
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply (V_{CCJ})
- I/O Pins Compatible with Voltage Levels Ranging From 1.8V to 3.3V
- Design Support Using the Xilinx ISE® Alliance and Foundation™ Software Packages
- XCF01S/XCF02S/XCF04S
  - 3.3V Supply Voltage
  - Serial FPGA Configuration Interface
  - Available in Small-Footprint VO20 and VOG20 Packages
- XCF08P/XCF16P/XCF32P
  - 1.8V Supply Voltage
  - Serial or Parallel FPGA Configuration Interface
  - Available in Small-Footprint VOG48, FS48, and FSG48 Packages
  - Design Revision Technology Enables Storing and Accessing Multiple Design Revisions for Configuration
  - Built-In Data Decompressor Compatible with Xilinx Advanced Compression Technology

Description

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs. Available in 1 to 32 Mb densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM series includes both the 3.3V XCFxxS PROM and the 1.8V XCFxxP PROM. The XCFxxS version includes 4 Mb, 2 Mb, and 1 Mb PROMs that support Master Serial and Slave Serial FPGA configuration modes (Figure 1, page 2). The XCFxxP version includes 32 Mb, 16 Mb, and 8 Mb PROMs that support Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes (Figure 2, page 2).

When driven from a stable, external clock, the PROMs can output data at rates up to 33 MHz. Refer to "AC Electrical Characteristics," page 16 for timing considerations.

A summary of the Platform Flash PROM family members and supported features is shown in Table 1.

Table 1: **Platform Flash PROM Features**

Device	Density (Mb)	V_{CCINT} (V)	V_{CCO} Range (V)	V_{CCJ} Range (V)	Packages	Program In-system via JTAG	Serial Config.	Parallel Config.	Design Revisioning	Compression
XCF01S	1	3.3	1.8 – 3.3	2.5 – 3.3	VO20/VOG20	✓	✓			
XCF02S	2	3.3	1.8 – 3.3	2.5 – 3.3	VO20/VOG20	✓	✓			
XCF04S	4	3.3	1.8 – 3.3	2.5 – 3.3	VO20/VOG20	✓	✓			
XCF08P	8	1.8	1.8 – 3.3	2.5 – 3.3	VO48/VOG48 FS48/FSG48	✓	✓	✓	✓(1)	✓
XCF16P	16	1.8	1.8 – 3.3	2.5 – 3.3	VO48/VOG48 FS48/FSG48	✓	✓	✓	✓	✓
XCF32P	32	1.8	1.8 – 3.3	2.5 – 3.3	VO48/VOG48 FS48/FSG48	✓	✓	✓	✓	✓

Notes:
1. XCF08P supports storage of a design revision only when cascaded with another XCFxxP PROM. See "Design Revisioning," page 8 for details.

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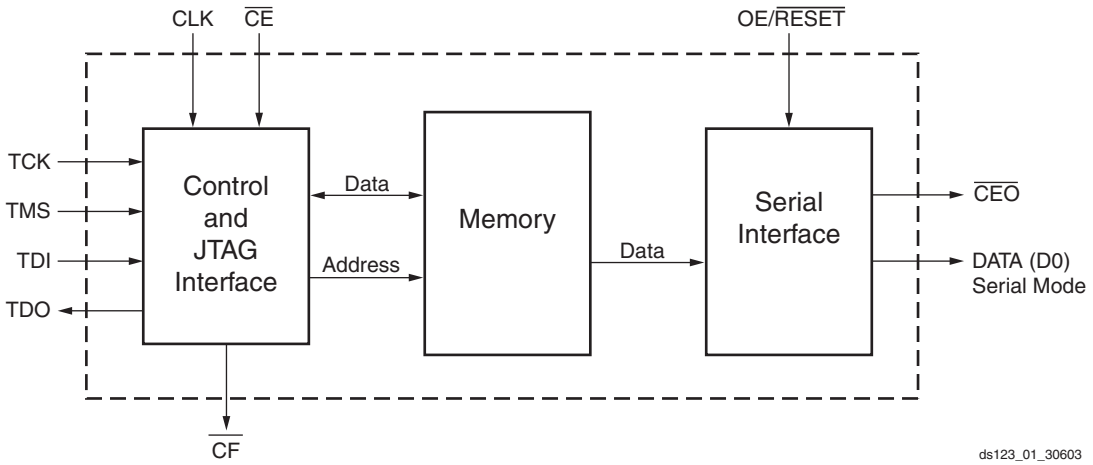


Figure 1: **XCFxxS Platform Flash PROM Block Diagram**

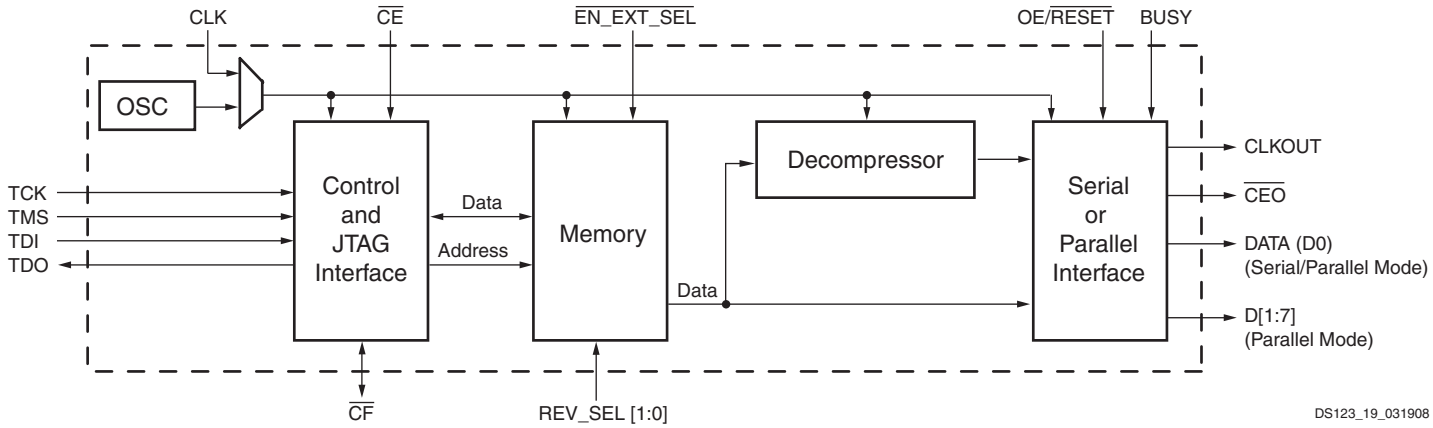


Figure 2: **XCFxxP Platform Flash PROM Block Diagram**

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. With $\overline{CF}$ High, a short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source, or optionally, for the XCFxxP PROM only, the PROM can be used to drive the FPGA's configuration clock.

The XCFxxP version of the Platform Flash PROM also supports Master SelectMAP and Slave SelectMAP (or Slave Parallel) FPGA configuration modes. When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave SelectMAP Mode, either an external oscillator generates the configuration clock that drives the PROM and the FPGA, or optionally, the XCFxxP PROM can be used to drive the FPGA's configuration clock. With BUSY Low and $\overline{CF}$ High, after $\overline{CE}$ and OE are enabled, data is available on the PROMs DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel/Slave SelectMAP mode.

The XCFxxP version of the Platform Flash PROM provides additional advanced features. A built-in data decompressor supports utilizing compressed PROM files, and design revisioning allows multiple design revisions to be stored on a single PROM or stored across several PROMs. For design revisioning, external pins or internal control bits are used to select the active design revision.

Multiple Platform Flash PROM devices can be cascaded to support the larger configuration files required when targeting larger FPGA devices or targeting multiple FPGAs daisy chained together. When utilizing the advanced features for the XCFxxP Platform Flash PROM, such as design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced XCFxxP features are not enabled, then the cascaded chain can include both XCFxxP and XCFxxS PROMs.

See UG161, *Platform Flash PROM User Guide*, for detailed guidelines on PROM-to-FPGA configuration hardware connections, for software usage, for a reference list of Xilinx FPGAs, and for the respective compatible Platform Flash PROMs. Table 2 lists the Platform Flash PROMs and their capacities.

Table 2: **Platform Flash PROM Capacity**

Platform Flash PROM	Configuration Bits	Platform Flash PROM	Configuration Bits
XCF01S	1,048,576	XCF08P	8,388,608
XCF02S	2,097,152	XCF16P	16,777,216
XCF04S	4,194,304	XCF32P	33,554,432

Programming

The Platform Flash PROM is a reprogrammable NOR flash device (refer "Quality and Reliability Characteristics," page 14 for the program/erase specifications). Reprogramming requires an erase followed by a program operation. A verify operation is recommended after the program operation to validate the correct transfer of data from the programmer source to the Platform Flash PROM.

Several programming solutions are available.

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 3.

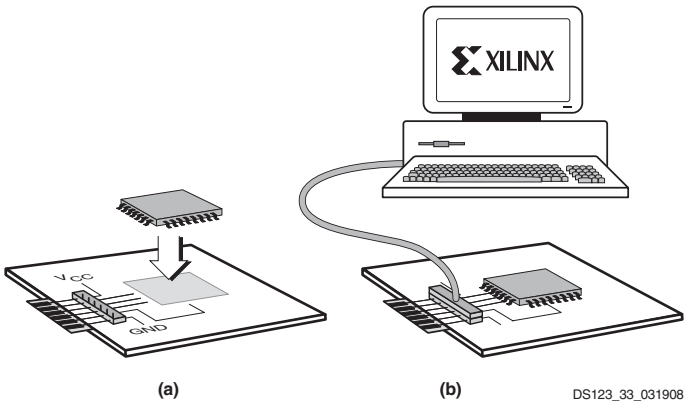


Figure 3: **JTAG In-System Programming Operation**
(a) Solder Device to PCB
(b) Program Using Download Cable

In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the $\overline{CEO}$ output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. All non-JTAG input pins are ignored during in-system programming, including CLK, CE, CF, OE/RESET, BUSY, EN_EXT_SEL, and REV_SEL[1:0]. In-system programming is fully supported across the recommended operating voltage and temperature ranges.

Embedded, in-system programming reference designs, such as XAPP058, *Xilinx In-System Programming Using an Embedded Microcontroller*, are available on the Xilinx web page for PROM Programming and Data Storage Application Notes. See UG161, *Platform Flash PROM User Guide,* for an advanced update methodology that uses the Design Revisioning feature in the Platform Flash XCFxxP PROMs.

OE/$\overline{RESET}$

The 1/2/4 Mb XCFxxS Platform Flash PROMs in-system programming algorithm results in issuance of an internal device reset that causes OE/$\overline{RESET}$ to pulse Low.

External Programming

In traditional manufacturing environments, third-party device programmers can program Platform Flash PROMs with an initial memory image before the PROMs are assembled onto boards. Contact a preferred third-party programmer vendor for Platform Flash PROM support information. A sample list of third-party programmer vendors with Platform Flash PROM support is available on the Xilinx web page for Third-Party Programmer Device Support. See UG161, *Platform Flash PROM User Guide*, for the PROM data file format required for programmers.

Pre-programmed PROMs can be assembled onto boards using the typical soldering process guidelines in UG112, *Device Package User Guide*. A pre-programmed PROM's memory image can be updated after board assembly using an in-system programming solution.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program-erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

See UG116, *Xilinx Device Reliability Report,* for device quality, reliability, and process node information.

Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. The XCFxxP PROMs can also be programmed to prevent inadvertent writing via JTAG. Table 3 and Table 4 show the security settings available for the XCFxxS PROM and XCFxxP PROM, respectively.

Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XCFxxS PROM, the read protect security bit is set for the entire device, and resetting the read protect security bit requires erasing the entire device. For the XCFxxP PROM the read protect security bit can be set for individual design revisions, and resetting the read protect bit requires erasing the particular design revision.

Write Protection

The XCFxxP PROM device also allows the user to write protect (or lock) a particular design revision or PROM option settings. Write protection helps to prevent an inadvertent JTAG instruction from modifying an area by write protecting the area and by locking the erase instruction. The write-protection setting can be cleared by erasing the protected area. However, an XSC_UNLOCK instruction must first be issued to the XCFxxP PROM to unlock the ISC_ERASE instruction. Refer to the XCFxxP PROM BSDL file for the XSC_UNLOCK and ISC_ERASE instructions.

> ***Caution!*** The iMPACT software always issues a XSC_UNLOCK when performing an Erase operation on an XCFxxP PROM and, thus, always unlocks the write protection.

Table 3: **XCFxxS Device Data Security Options**

Read Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)			
Set	✓		

Table 4: **XCFxxP Design Revision Data Security Options**

Read Protect	Write Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)	Reset (default)			
Reset (default)	Set		✓	✓
Set	Reset (default)	✓		
Set	Set	✓	✓	✓

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is compatible with the IEEE 1149.1 Boundary-Scan standard and the IEEE 1532 in-system configuration standard. A Test Access Port (TAP) and registers are provided to support all required Boundary-Scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 5 lists the required and optional Boundary-Scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of Boundary-Scan architecture and the required and optional instructions.

Caution! The XCFxxP JTAG TAP pause states are not fully compliant with the JTAG 1149.1 specification. If a temporary pause of a JTAG shift operation is required, then stop the JTAG TCK clock and maintain the JTAG TAP within the JTAG Shift-IR or Shift-DR TAP state. Do not transition the XCFxxP JTAG TAP through the JTAG Pause-IR or Pause-DR TAP state to temporarily pause a JTAG shift operation.

Table 5: **Platform Flash PROM Boundary-Scan Instructions**

Boundary-Scan Command	XCFxxS IR[7:0] (hex)	XCFxxP IR[15:0] (hex)	Instruction Description
Required Instructions			
BYPASS	FF	FFFF	Enables BYPASS
SAMPLE/PRELOAD	01	0001	Enables Boundary-Scan SAMPLE/PRELOAD operation
EXTEST	00	0000	Enables Boundary-Scan EXTEST operation
Optional Instructions			
CLAMP	FA	00FA	Enables Boundary-Scan CLAMP operation
HIGHZ	FC	00FC	Places all outputs in high-impedance state simultaneously
IDCODE	FE	00FE	Enables shifting out 32-bit IDCODE
USERCODE	FD	00FD	Enables shifting out 32-bit USERCODE
Platform Flash PROM Specific Instructions			
CONFIG	EE	00EE	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once. (For the XCFxxP this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits.)(1)

Notes:

1. For more information see "Initiating FPGA Configuration," page 10.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

XCFxxS Instruction Register (8 bits wide)

The Instruction Register (IR) for the XCFxxS PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 6, page 6. The instruction capture pattern shifted out of the XCFxxS device includes IR[7:0]. IR[7:5] are reserved bits and are set to a logic 0. The ISC Status field, IR[4], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The Security field, IR[3], contains logic 1 if the device has been programmed with the security option turned on; otherwise, it contains logic 0. IR[2] is unused, and is set to '0'. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

XCFxxP Instruction Register (16 bits wide)

The Instruction Register (IR) for the XCFxxP PROM is sixteen bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 7, page 6.

The instruction capture pattern shifted out of the XCFxxP device includes IR[15:0]. IR[15:9] are reserved bits and are set to a logic 0. The ISC Error field, IR[8:7], contains a 10 when an ISC operation is a success; otherwise a 01 when an In-System Configuration (ISC) operation fails. The Erase/Program (ER/PROG) Error field, IR[6:5], contains a 10 when an erase or program operation is a success; otherwise a 01 when an erase or program operation fails. The Erase/Program (ER/PROG) Status field, IR[4], contains a logic 0 when the device is busy performing an erase or programming operation; otherwise, it contains a logic 1. The ISC Status field, IR[3], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The DONE field, IR[2], contains logic 1 if the sampled design revision has been successfully programmed; otherwise, a logic 0 indicates incomplete programming. The remaining bits IR[1:0] are set to 01 as defined by IEEE Std. 1149.1.

Table 6: **XCFxxS Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

TDI →	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Status	Security	0	0 1	

Table 7: **XCFxxP Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

TDI →	IR[15:9]	IR[8:7]	IR[6:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Error	ER/PROG Error	ER/PROG Status	ISC Status	DONE	0 1	

Boundary-Scan Register

The Boundary-Scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the Boundary-Scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the Boundary-Scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See Table 12, page 24 and Table 13, page 26 for the Boundary-Scan bit order for all connected device pins, or see the appropriate BSDL file for the complete Boundary-Scan bit order description under the “attribute BOUNDARY_REGISTER” section in the BSDL file. The bit assigned to Boundary-Scan cell 0 is the LSB in the Boundary-Scan register, and is the register bit closest to TDO.

Identification Registers

IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG. Table 8 lists the IDCODE register values for the Platform Flash PROMs.

The IDCODE register has the following binary format:

`vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1`

where

- `v` = the die version number
- `f` = the PROM family code
- `a` = the specific Platform Flash PROM product ID
- `c` = the Xilinx manufacturer's ID

The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1.

Table 8: **IDCODES Assigned to Platform Flash PROMs**

Device	IDCODE (1) (hex)
XCF01S	<*v*>5044093
XCF02S	<*v*>5045093
XCF04S	<*v*>5046093
XCF08P	<*v*>5057093
XCF16P	<*v*>5058093
XCF32P	<*v*>5059093

Notes:

1. The <*v*> in the IDCODE field represents the device’s revision code (in hex) and can vary.

USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains `FFFFFFFFh`.

Customer Code Register

For the XCFxxP Platform Flash PROM, in addition to the USERCODE, a unique 32-byte Customer Code can be assigned to each design revision enabled for the PROM. The Customer Code is set during programming, and is typically used to supply information about the design revision contents. A private JTAG instruction is required to read the Customer Code. If the PROM is blank, or the Customer Code for the selected design revision was not loaded during programming, or if the particular design revision is erased, the Customer Code contains all ones.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 Boundary-Scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both Boundary-Scan and ISP operations.

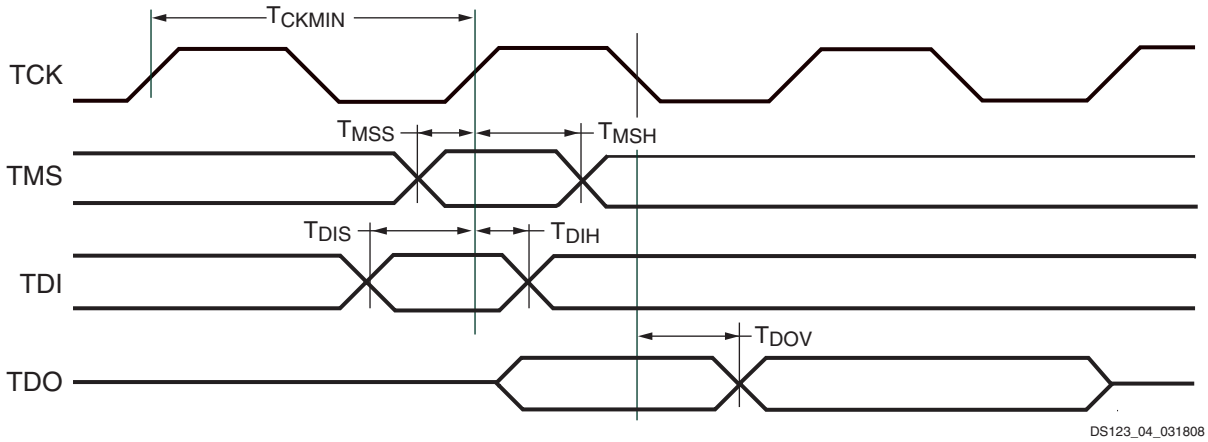


Figure 4: **Test Access Port Timing**

TAP AC Parameters

Table 9 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 9: **Test Access Port Timing Parameters**

Symbol	Description	Min	Max	Units
T_{CKMIN}	TCK minimum clock period when V_{CCJ} = 2.5V or 3.3V	67	–	ns
T_{MSS}	TMS setup time when V_{CCJ} = 2.5V or 3.3V	8	–	ns
T_{MSH}	TMS hold time when V_{CCJ} = 2.5V or 3.3V	25	–	ns
T_{DIS}	TDI setup time when V_{CCJ} = 2.5V or 3.3V	8	–	ns
T_{DIH}	TDI hold time when V_{CCJ} = 2.5V or 3.3V	25	–	ns
T_{DOV}	TDO valid delay when V_{CCJ} = 2.5V or 3.3V	–	22	ns

Additional Features for the XCFxxP

Internal Oscillator

The 8/16/32 Mb XCFxxP Platform Flash PROMs include an optional internal oscillator which can be used to drive the CLKOUT and DATA pins on FPGA configuration interface. The internal oscillator can be enabled when programming the PROM, and the oscillator can be set to either the default frequency or to a slower frequency. Refer to the “XCFxxP Decompression and Clock Options” chapter of UG161, *Platform Flash PROM User Guide*, for internal oscillator recommendations.

CLKOUT

The 8/16/32 Mb XCFxxP Platform Flash PROMs include the programmable option to enable the CLKOUT signal which allows the PROM to provide a source synchronous clock aligned to the data on the configuration interface. The CLKOUT signal is derived from one of two clock sources: the CLK input pin or the internal oscillator. The input clock source is selected during the PROM programming sequence. Output data is available on the rising edge of CLKOUT.

The CLKOUT signal is enabled during programming, and is active when $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High. On $\overline{CE}$ rising edge transition, if OE/$\overline{RESET}$ is High and the PROM terminal count has not been reached, then CLKOUT remains active for an additional eights clock cycles before being disabled. On a OE/$\overline{RESET}$ falling edge transition, CLKOUT is immediately disabled. When disabled, the CLKOUT pin is put into a high-impedance state and should be pulled High externally to provide a known state.

When cascading Platform Flash PROMs with CLKOUT enabled, after completing it's data transfer, the first PROM disables CLKOUT and drives the $\overline{CEO}$ pin enabling the next PROM in the PROM chain. The next PROM begins driving the CLKOUT signal once that PROM is enabled and data is available for transfer.

During high-speed parallel configuration without compression, the FPGA drives the BUSY signal on the configuration interface. When BUSY is asserted High, the PROMs internal address counter stops incrementing, and the current data value is held on the data outputs. While BUSY is High, the PROM continues driving the CLKOUT signal to the FPGA, clocking the FPGA’s configuration logic. When the FPGA deasserts BUSY, indicating that it is ready to receive additional configuration data, the PROM begins driving new data onto the configuration interface.

Decompression

The 8/16/32 Mb XCFxxP Platform Flash PROMs include a built-in data decompressor compatible with Xilinx advanced compression technology. Compressed Platform Flash PROM files are created from the target FPGA bitstream(s) using the iMPACT software. Only Slave Serial and Slave SelectMAP (parallel) configuration modes are supported for FPGA configuration when using a XCFxxP PROM programmed with a compressed bitstream. Compression rates vary depending on several factors, including the target device family and the target design contents.

The decompression option is enabled during the PROM programming sequence. The PROM decompresses the stored data before driving both clock and data onto the FPGA's configuration interface. If Decompression is enabled, then the Platform Flash clock output pin (CLKOUT) must be used as the clock signal for the configuration interface, driving the target FPGA's configuration clock input pin (CCLK). Either the PROM's CLK input pin or the internal oscillator must be selected as the source for CLKOUT. Any target FPGA connected to the PROM must operate as slave in the configuration chain, with the configuration mode set to Slave Serial mode or Slave SelectMap (parallel) mode.

When decompression is enabled, the CLKOUT signal becomes a controlled clock output with a reduced maximum frequency. When decompressed data is not ready, the CLKOUT pin is put into a high-Z state and must be pulled High externally to provide a known state.

The BUSY input is automatically disabled when decompression is enabled.

See the "Decompression Setups" section in the *Platform Flash PROM User Guide* for setup details.

Design Revisioning

Design Revisioning allows the user to create up to four unique design revisions on a single PROM or stored across multiple cascaded PROMs. Design Revisioning is supported for the 8/16/32 Mb XCFxxP Platform Flash PROMs in both serial and parallel modes. Design Revisioning can be used with compressed PROM files, and also when the CLKOUT feature is enabled. The PROM programming files along with the revision information files (`.cfi`) are created using the iMPACT software. The `.cfi` file is required to enable design revision programming in iMPACT.

A single design revision is composed of from 1 to *n* 8 Mb memory blocks. If a single design revision contains less than 8 Mb of data, then the remaining space is padded with all ones. A larger design revision can span several 8 Mb memory blocks, and any space remaining in the last 8 Mb memory block is padded with all ones.

- A single 32 Mb PROM contains four 8 Mb memory blocks, and can therefore store up to four separate design revisions: one 32 Mb design revision, two 16 Mb design revisions, three 8 Mb design revisions, four 8 Mb design revisions, and so on.

- Because of the 8 Mb minimum size requirement for each revision, a single 16 Mb PROM can only store up to two separate design revisions: one 16 Mb design revision, one 8 Mb design revision, or two 8 Mb design revisions.
- A single 8 Mb PROM can store only one 8 Mb design revision.

Larger design revisions can be split over several cascaded PROMs. For example, two 32 Mb PROMs can store up to four separate design revisions: one 64 Mb design revision, two 32 Mb design revisions, three 16 Mb design revisions, four 16 Mb design revisions, and so on. When cascading one 16 Mb PROM and one 8 Mb PROM, there are 24 Mb of available space, and therefore up to three separate design revisions can be stored: one 24 Mb design revision, two 8 Mb design revisions, or three 8 Mb design revisions.

See Figure 5 for a few basic examples of how multiple revisions can be stored. The design revision partitioning is handled automatically during file generation in iMPACT.

During the PROM file creation, each design revision is assigned a revision number:

Revision 0 = '00'
Revision 1 = '01'
Revision 2 = '10'
Revision 3 = '11'

After programming the Platform Flash PROM with a set of design revisions, a particular design revision can be selected using the external REV_SEL[1:0] pins or using the internal programmable design revision control bits. The $\overline{\text{EN_EXT_SEL}}$ pin determines if the external pins or internal bits are used to select the design revision. When $\overline{\text{EN_EXT_SEL}}$ is Low, design revision selection is controlled by the external Revision Select pins, REV_SEL[1:0]. When $\overline{\text{EN_EXT_SEL}}$ is High, design revision selection is controlled by the internal programmable Revision Select control bits. During power up, the design revision selection inputs (pins or control bits) are sampled internally. After power up, the design revision selection inputs are sampled again when any of the following events occur:

- On the rising edge of $\overline{\text{CE}}$.
- On the falling edge of OE/$\overline{\text{RESET}}$ (when $\overline{\text{CE}}$ is Low).
- On the rising edge of $\overline{\text{CF}}$ (when $\overline{\text{CE}}$ is Low).
- When reconfiguration is initiated by using the JTAG CONFIG instruction.

The data from the selected design revision is then presented on the FPGA configuration interface.

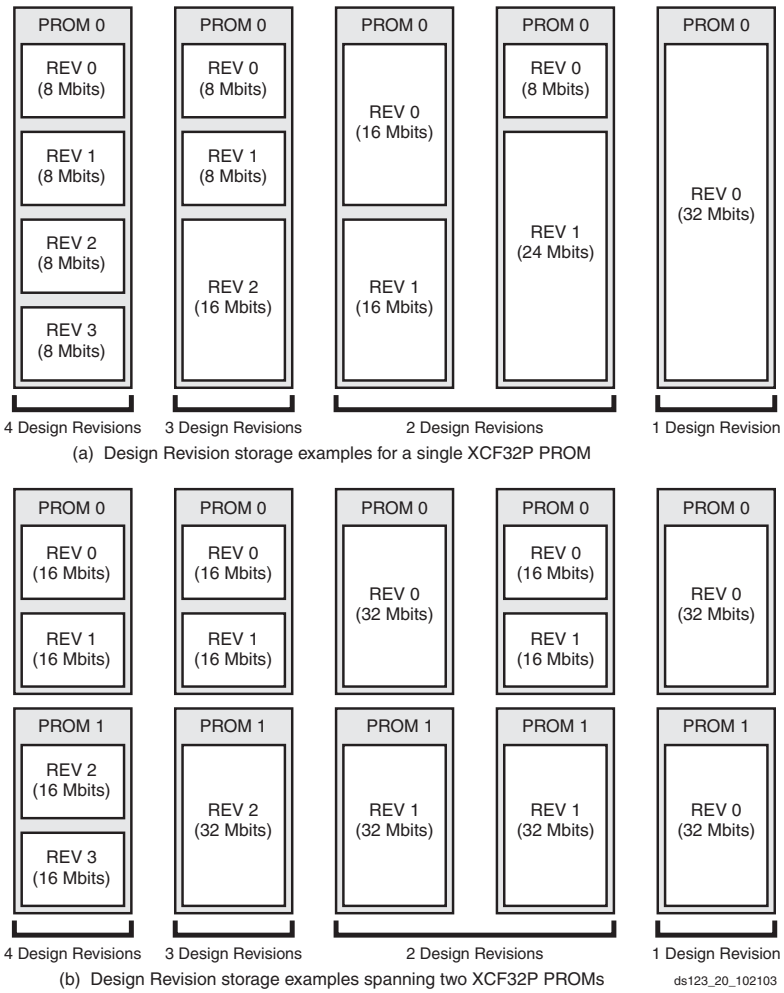


Figure 5: **Design Revision Storage Examples**

Initiating FPGA Configuration

The options for initiating FPGA configuration via the Platform Flash PROM include:

- Automatic configuration on power up
- Applying an external pulse to the FPGA PROGRAM_B pin
- Applying the JTAG CONFIG instruction to the PROM

Following the FPGA's power-on sequence or the assertion of the PROGRAM_B pin, the FPGA's configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROGRAM_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a $\overline{CF}$ pin that can be tied to the FPGA's PROGRAM_B pin. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ output Low once for 300-500 ns, resetting the FPGA and initiating configuration. The iMPACT software can issue the JTAG CONFIG command to initiate FPGA configuration by setting the "Load FPGA" option.

When using the XCFxxP Platform Flash PROM with design revisioning enabled, the $\overline{CF}$ pin should always be connected to the PROGRAM_B pin on the FPGA to ensure that the current design revision selection is sampled when the FPGA is reset. The XCFxxP PROM samples the current design revision selection from the external REV_SEL pins or the internal programmable Revision Select bits on the rising edge of $\overline{CF}$. When the JTAG CONFIG command is executed, the XCFxxP samples the new design revision selection before initiating the FPGA configuration sequence. When using the XCFxxP Platform Flash PROM without design revisioning, if the $\overline{CF}$ pin is not connected to the FPGA PROGRAM_B pin, then the XCFxxP $\overline{CF}$ pin must be tied High.

Reset and Power-On Reset Activation

At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/$\overline{RESET}$ is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/$\overline{RESET}$ release is delayed (T_{OER} minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/$\overline{RESET}$ pin is connected to an external 4.7 kΩ pull-up resistor and also to the target FPGA's INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/$\overline{RESET}$ pin Low. When OE/$\overline{RESET}$ is released, the FPGA's INIT pin is pulled High allowing the FPGA's configuration sequence to begin. If the power drops below the power-down threshold (V_{CCPD}), the PROM resets and OE/$\overline{RESET}$ is again held Low until the after the POR threshold is reached. OE/$\overline{RESET}$ polarity is not programmable. These power-up requirements are shown graphically in Figure 6.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/$\overline{RESET}$ is asserted (Low) or $\overline{CE}$ is deasserted (High). The address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state.

Note:

1. The XCFxxS PROM only requires V_{CCINT} to rise above its POR threshold before releasing OE/$\overline{RESET}$.
2. The XCFxxP PROM requires both V_{CCINT} to rise above its POR threshold and for V_{CCO} to reach the recommended operating voltage level before releasing OE/$\overline{RESET}$.

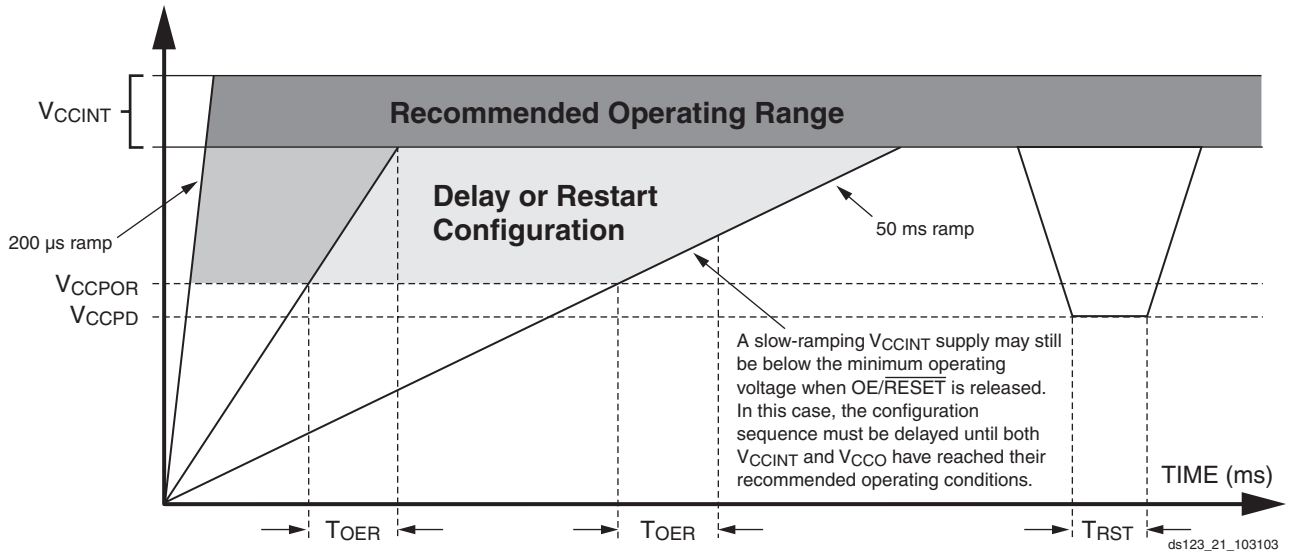


Figure 6: **Platform Flash PROM Power-Up Requirements**

I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V-tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The core power supply (V_{CCINT}), JTAG pin power supply (V_{CCJ}), output power supply (V_{CCO}), and external 3V CMOS I/O signals can be applied in any order.

Additionally, for the XCFxxS PROM only, when V_{CCO} is supplied at 2.5V or 3.3V and V_{CCINT} is supplied at 3.3V, the I/Os are 5V-tolerant. This allows 5V CMOS signals to connect directly to the inputs on a powered XCFxxS PROM without damage. Failure to power the PROM correctly while supplying a 5V input signal can result in damage to the XCFxxS device.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is deasserted (High). In standby mode, the address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the OE/$\overline{RESET}$ input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

When using the FPGA DONE signal to drive the PROM $\overline{CE}$ pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330Ω pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and is also connected to the PROM $\overline{CE}$ pin to enable low-power standby mode, then an external buffer should be used to drive the LED circuit to ensure valid transitions on the PROM's $\overline{CE}$ pin. If low-power standby mode is not required for the PROM, then the $\overline{CE}$ pin should be connected to ground.

Table 10: **Truth Table for XCFxxS PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/$\overline{RESET}$	$\overline{CE}$		DATA	$\overline{CEO}$	ICC
High	Low	If address < TC(2) : increment	Active	High	Active
		If address = TC(2) : don't change	High-Z	Low	Reduced
Low	Low	Held reset	High-Z	High	Active
X(1)	High	Held reset	High-Z	High	Standby

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value.

Table 11: **Truth Table for XCFxxP PROM Control Inputs**

Control Inputs				Internal Address	Outputs			
OE/$\overline{RESET}$	$\overline{CE}$	$\overline{CF}$	BUSY(5)		DATA	$\overline{CEO}$	CLKOUT	ICC
High	Low	High	Low	If address < TC(2) and address < EA(3) : increment	Active	High	Active	Active
				If address < TC(2) and address = EA(3) : don't change	High-Z	High	High-Z	Reduced
				Else If address = TC(2) : don't change	High-Z	Low	High-Z	Reduced
High	Low	High	High	Unchanged	Active and Unchanged	High	Active	Active
High	Low	↑	X(1)	Reset(4)	Active	High	Active	Active
Low	Low	X	X	Held reset(4)	High-Z	High	High-Z	Active
X	High	X	X	Held reset(4)	High-Z	High	High-Z	Standby

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value.
3. For the XCFxxP with Design Revisioning enabled, EA = end address (last address in the selected design revision).
4. For the XCFxxP with Design Revisioning enabled, Reset = address reset to the beginning address of the selected bank. If Design Revisioning is not enabled, then Reset = address reset to address 0.
5. The BUSY input is only enabled when the XCFxxP is programmed for parallel data output and decompression is not enabled.

DC Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description		XCF01S, XCF02S, XCF04S	XCF08P, XCF16P, XCF32P	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to +4.0	–0.5 to +2.7	V
V_{CCO}	I/O supply voltage relative to GND		–0.5 to +4.0	–0.5 to +4.0	V
V_{CCJ}	JTAG I/O supply voltage relative to GND		–0.5 to +4.0	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	$V_{CCO} < 2.5V$	–0.5 to +3.6	–0.5 to +3.6	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	–0.5 to +3.6	V
V_{TS}	Voltage applied to High-Z output	$V_{CCO} < 2.5V$	–0.5 to +3.6	–0.5 to +3.6	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	–0.5 to +3.6	V
T_{STG}	Storage temperature (ambient)		–65 to +150	–65 to +150	°C
T_J	Junction temperature		+125	+125	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
3. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at www.xilinx.com.

Supply Voltage Requirements for Power-On Reset and Power-Down

Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(2)	0.2	50	0.2	50	ms
V_{CCPOR}	POR threshold for the V_{CCINT} supply	1	–	0.5	–	V
T_{OER}	OE/$\overline{RESET}$ release delay following POR(3)	0.5	3	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	–	1	–	0.5	V
T_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	–	10	–	ms

Notes:

1. V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
2. At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, page 11.
3. If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{RESET}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

Recommended Operating Conditions

Symbol	Description		XCF01S, XCF02S, XCF04S			XCF08P, XCF16P, XCF32P			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CCINT}	Internal voltage supply		3.0	3.3	3.6	1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	3.3V Operation	3.0	3.3	3.6	3.0	3.3	3.6	V
		2.5V Operation	2.3	2.5	2.7	2.3	2.5	2.7	V
		1.8V Operation	1.7	1.8	1.9	1.7	1.8	1.9	V
V_{CCJ}	Supply voltage for JTAG output drivers	3.3V Operation	3.0	3.3	3.6	3.0	3.3	3.6	V
		2.5V Operation	2.3	2.5	2.7	2.3	2.5	2.7	V
V_{IL}	Low-level input voltage	3.3V Operation	0	–	0.8	0	–	0.8	V
		2.5V Operation	0	–	0.7	0	–	0.7	V
		1.8V Operation	–	–	20% V_{CCO}	–	–	20% V_{CCO}	V
V_{IH}	High-level input voltage	3.3V Operation	2.0	–	5.5	2.0	–	3.6	V
		2.5V Operation	1.7	–	5.5	1.7	–	3.6	V
		1.8V Operation	70% V_{CCO}	–	3.6	70% V_{CCO}	–	3.6	V
T_{IN}	Input signal transition time(1)		–	–	500	–	–	500	ns
V_O	Output voltage		0	–	V_{CCO}	0	–	V_{CCO}	V
T_A	Operating ambient temperature		–40	–	85	–40	–	85	°C

Notes:

1. Input signal transition time measured between 10% V_{CCO} and 90% V_{CCO}.

Quality and Reliability Characteristics

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	–	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	–	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	–	Volts

DC Characteristics Over Operating Conditions

Symbol	Description	XCF01S, XCF02S, XCF04S			XCF08P, XCF16P, XCF32P			Units
		Test Conditions	Min	Max	Test Conditions	Min	Max	
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	–	I_{OH} = –4 mA	2.4	–	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	V_{CCO} – 0.4	–	I_{OH} = –500 µA	V_{CCO} – 0.4	–	V
	High-level output voltage for 1.8V outputs	I_{OH} = –50 µA	V_{CCO} – 0.4	–	I_{OH} = –50 µA	V_{CCO} – 0.4	–	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 4 mA	–	0.4	I_{OL} = 4 mA	–	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	–	0.4	I_{OL} = 500 µA	–	0.4	V
	Low-level output voltage for 1.8V outputs	I_{OL} = 50 µA	–	0.4	I_{OL} = 50 µA	–	0.4	V
I_{CCINT}	Internal voltage supply current, active mode	33 MHz	–	10	33 MHz	–	10	mA
I_{CCO}(1)	Output driver supply current, active serial mode	33 MHz	–	10	33 MHz	–	10	mA
	Output driver supply current, active parallel mode	–	–	–	33 MHz	–	40	mA
I_{CCJ}	JTAG supply current, active mode	Note (2)	–	5	Note (2)	–	5	mA
I_{CCINTS}	Internal voltage supply current, standby mode	Note (3)	–	5	Note (3)	–	1	mA
I_{CCOS}	Output driver supply current, standby mode	Note (3)	–	1	Note (3)	–	1	mA
I_{CCJS}	JTAG supply current, standby mode	Note (3)	–	1	Note (3)	–	1	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current	V_{CCJ} = max V_{IN} = GND	–	100	V_{CCJ} = max V_{IN} = GND	–	100	µA
I_{IL}	Input leakage current	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–10	10	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–10	10	µA
I_{IH}	Input and output High-Z leakage current	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–10	10	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–10	10	µA
I_{ILP}	Source current through internal pull-ups on $\overline{EN_EXT_SEL}$, REV_SEL0, REV_SEL1	–	–	–	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–	100	µA
I_{IHP}	Sink current through internal pull-down on BUSY	–	–	–	V_{CCINT} = max V_{CCO} = max V_{IN} = GND or V_{CCO}	–100	–	µA
C_{IN}	Input capacitance	V_{IN} = GND f = 1.0 MHz	–	8	V_{IN} = GND f = 1.0 MHz	–	8	pF
C_{OUT}	Output capacitance	V_{IN} = GND f = 1.0 MHz	–	14	V_{IN} = GND f = 1.0 MHz	–	14	pF

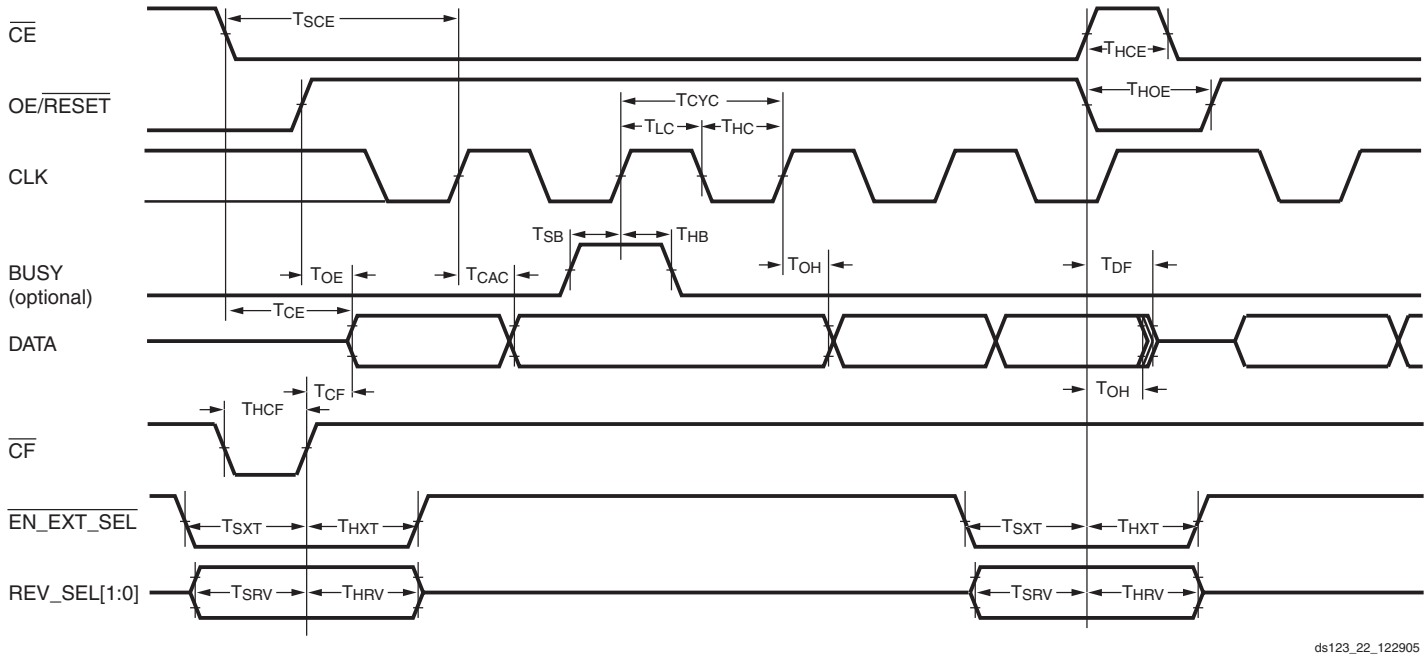
Notes:

1. Output driver supply current specification based on no load conditions.
2. TDI/TMS/TCK non-static (active).
3. $\overline{CE}$ High, OE Low, and TMS/TDI/TCK static.

AC Electrical Characteristics

AC Characteristics Over Operating Conditions

XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source



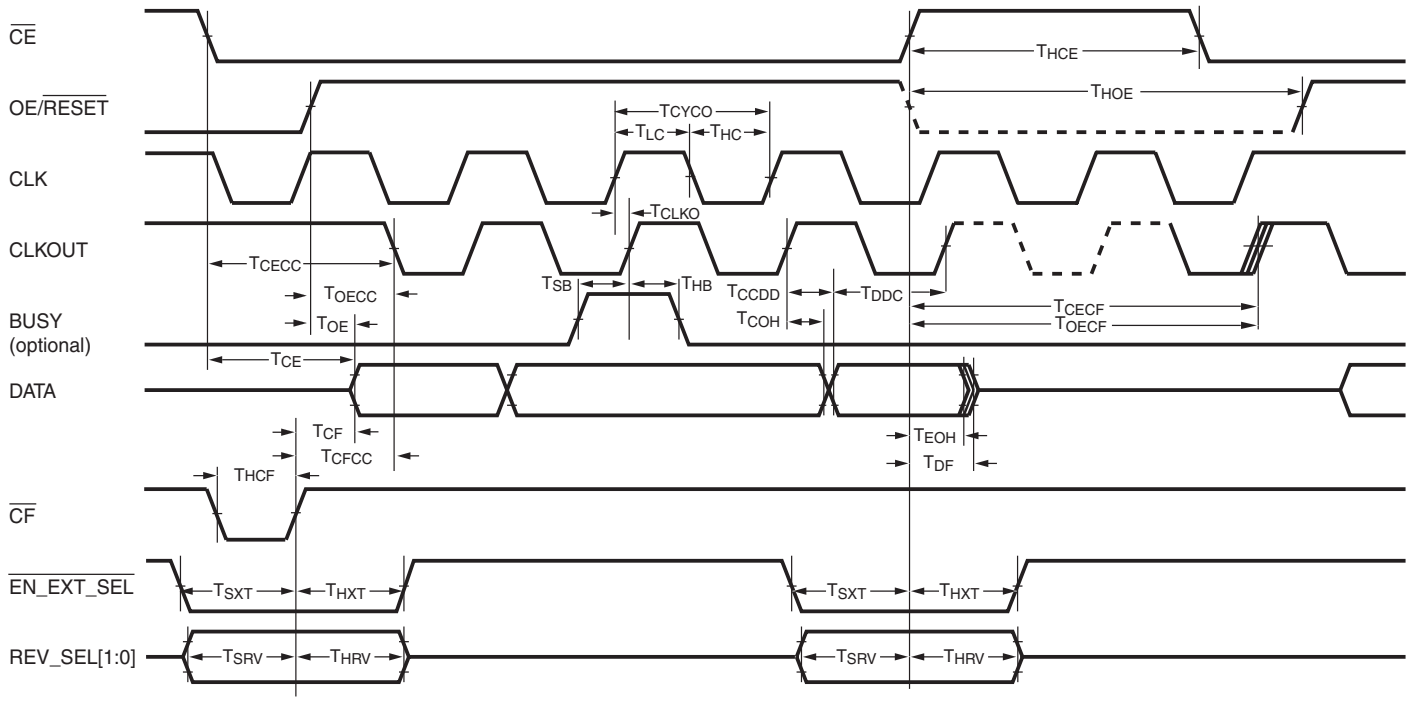
Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{HCF}	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(9)	300		300		ns
	$\overline{CF}$ hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(9)	300		300		ns
T_{CF}	$\overline{CF}$ to data delay when VCCO = 3.3V or 2.5V(8)	–	–	–	25	ns
	$\overline{CF}$ to data delay when VCCO = 1.8V(8)	–	–	–	25	ns
T_{OE}	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 3.3V or 2.5V	–	10	–	25	ns
	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 1.8V	–	30	–	25	ns
T_{CE}	$\overline{CE}$ to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	15	–	25	ns
	$\overline{CE}$ to data delay(5) when V_{CCO} = 1.8V	–	30	–	25	ns
T_{CAC}	CLK to data delay(7) when V_{CCO} = 3.3V or 2.5V	–	15	–	25	ns
	CLK to data delay(7) when V_{CCO} = 1.8V	–	30	–	25	ns
T_{OH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, CLK, or $\overline{CF}$ when V_{CCO} = 3.3V or 2.5V(8)	0	–	5	–	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, CLK, or $\overline{CF}$ when V_{CCO} = 1.8V(8)	0	–	5	–	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	25	–	45	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 1.8V	–	30	–	45	ns

Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{CYC}	Clock period(6) (serial mode) when V_{CCO} = 3.3V or 2.5V	30	–	25	–	ns
	Clock period(6) (serial mode) when V_{CCO} = 1.8V	67	–	25	–	ns
	Clock period(6) (parallel mode) when V_{CCO} = 3.3V or 2.5V	–	–	30	–	ns
	Clock period(6) (parallel mode) when V_{CCO} = 1.8V	–	–	30	–	ns
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	10	–	12	–	ns
	CLK Low time(3) when V_{CCO} = 1.8V	15	–	12	–	ns
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	10	–	12	–	ns
	CLK High time(3) when V_{CCO} = 1.8V	15	–	12	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 3.3V or 2.5V	20	–	30	–	ns
	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 1.8V	30		30	–	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	250	–	2000	–	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	250	–	2000	–	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	250	–	2000	–	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	250	–	2000	–	ns
T_{SB}	BUSY setup time to CLK when V_{CCO} = 3.3V or 2.5V(8)	–	–	12	–	ns
	BUSY setup time to CLK when V_{CCO} = 1.8V(8)	–	–	12	–	ns
T_{HB}	BUSY hold time to CLK when V_{CCO} = 3.3V or 2.5V(8)	–	–	8	–	ns
	BUSY hold time to CLK when V_{CCO} = 1.8V(8)	–	–	8	–	ns
T_{SXT}	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	–	–	300	–	ns
	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	–	–	300	–	ns
T_{HXT}	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	–	–	300	–	ns
	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	–	–	300	–	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	–	–	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	–	–	300	–	ns
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V(8)	–	–	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$ or OE/$\overline{RESET}$ when V_{CCO} = 1.8V(8)	–	–	300	–	ns

Notes:

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
4. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
5. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
6. This is the minimum possible T_{CYC}. Actual T_{CYC} = T_{CAC} + FPGA Data setup time. Example: With the XCF32P in serial mode with V_{CCO} at 3.3V, if FPGA data setup time = 15 ns, then the actual T_{CYC} = 25 ns +15 ns = 40 ns.
7. Guaranteed by design; not tested.
8. $\overline{CF}$, $\overline{EN_EXT_SEL}$, REV_SEL[1:0], and BUSY are inputs for the XCFxxP PROM only.
9. When JTAG CONFIG command is issued, PROM drives $\overline{CF}$ Low for at least the T_{HCF} minimum.

XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source



Note: Typically, 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.

ds123_25_110707

Symbol	Description	XCF08P, XCF16P, XCF32P		Units
		Min	Max	
T_{HCF}	CF hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(11)	300		300
	CF hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(11)	300		300
T_{CF}	CF to data delay when VCCO = 3.3V or 2.5V	–		ns
	CF to data delay when VCCO = 1.8V	–		ns
T_{OE}	OE/RESET to data delay(6) when V_{CCO} = 3.3V or 2.5V	–	25	ns
	OE/RESET to data delay(6) when V_{CCO} = 1.8V	–	25	ns
T_{CE}	CE to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	25	ns
	CE to data delay(5) when V_{CCO} = 1.8V	–	25	ns
T_{EOH}	Data hold from CE, OE/RESET, or CF when V_{CCO} = 3.3V or 2.5V	5	–	ns
	Data hold from CE, OE/RESET, or CF when V_{CCO} = 1.8V	5	–	ns
T_{DF}	CE or OE/RESET to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	45	ns
	CE or OE/RESET to data float delay(2) when V_{CCO} = 1.8V	–	45	ns
T_{OECF}	OE/RESET to CLKOUT float delay(2) when V_{CCO} = 3.3V or 2.5V	–		ns
	OE/RESET to CLKOUT float delay(2) when V_{CCO} = 1.8V	–		ns
T_{CECF}	CE to CLKOUT float delay(2) when V_{CCO} = 3.3V or 2.5V	–		ns
	CE to CLKOUT float delay(2) when V_{CCO} = 1.8V	–		ns

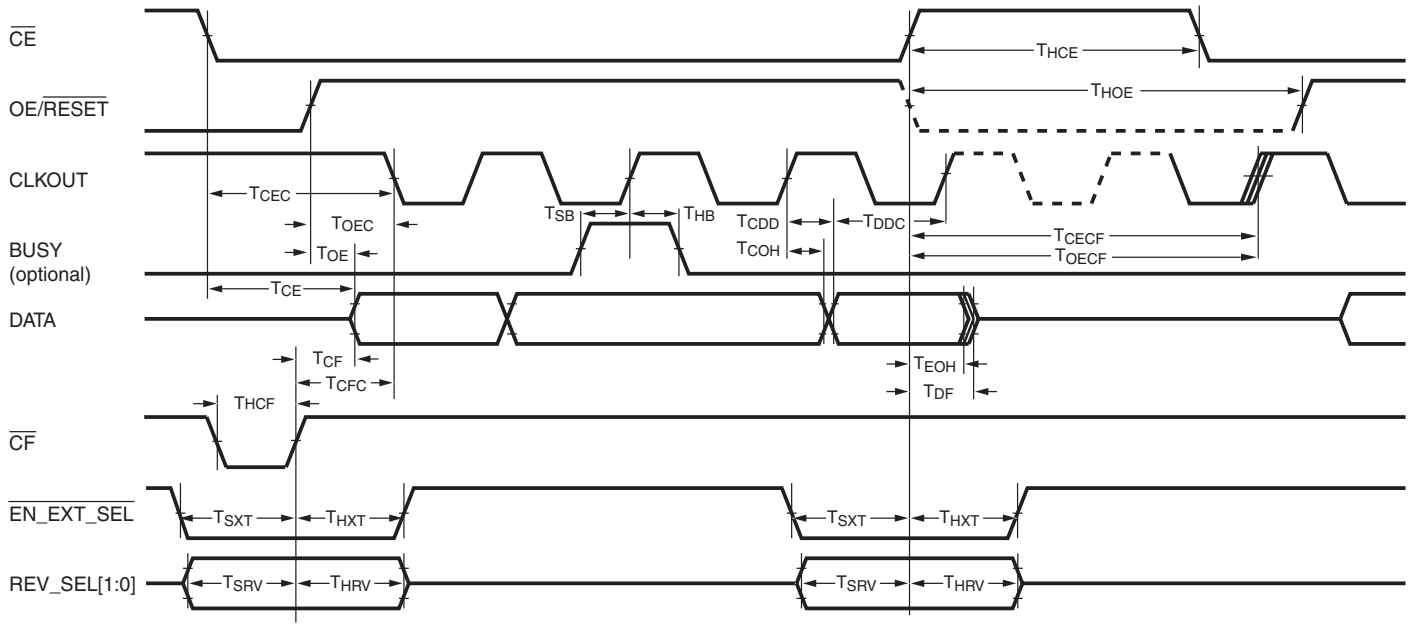
Symbol	Description	XCF08P, XCF16P, XCF32P		Units
		Min	Max	
T_{CYCO}	Clock period(7) (serial mode) when V_{CCO} = 3.3V or 2.5V	30	–	ns
	Clock period(7) (serial mode) when V_{CCO} = 1.8V	30	–	ns
	Clock period(7) (parallel mode) when V_{CCO} = 3.3V or 2.5V	35	–	ns
	Clock period(7) (parallel mode) when V_{CCO} = 1.8V	35	–	ns
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK Low time(3) when V_{CCO} = 1.8V	12	–	ns
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	12	–	ns
	CLK High time(3) when V_{CCO} = 1.8V	12	–	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	2000	–	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	2000	–	ns
T_{SB}	BUSY setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V	12	–	ns
	BUSY setup time to CLKOUT when V_{CCO} = 1.8V	12	–	ns
T_{HB}	BUSY hold time to CLKOUT when V_{CCO} = 3.3V or 2.5V	8	–	ns
	BUSY hold time to CLKOUT when V_{CCO} = 1.8V	8	–	ns
T_{CLKO}	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V with decompression(12)	–	35	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V with decompression(12)	–	35	ns
T_{CECC}	$\overline{CE}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0	2 CLK cycles	–
	$\overline{CE}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0	2 CLK cycles	–
T_{OECC}	OE/$\overline{RESET}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0	2 CLK cycles	–
	OE/$\overline{RESET}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0	2 CLK cycles	–
T_{CFCC}	$\overline{CF}$ to CLKOUT delay(8) when V_{CCO} = 3.3V or 2.5V	0		–
	$\overline{CF}$ to CLKOUT delay(8) when V_{CCO} = 1.8V	0		–
T_{CCDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V(9)	–	30	ns
	CLKOUT to data delay when V_{CCO} = 1.8V(9)	–	30	ns
T_{DDC}	Data setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(9)(12)	5		ns
	Data setup time to CLKOUT when V_{CCO} = 1.8V with decompression(9)(12)	5		ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(12)	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V with decompression(12)	3	–	ns
T_{SXT}	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns

Symbol	Description	XCF08P, XCF16P, XCF32P		Units
		Min	Max	
T_{HXT}	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns

Notes:

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads.Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. This is the minimum possible T_{CYCO}. Actual T_{CYCO} = T_{CCDD} + FPGA Data setup time. *Example:* With the XCF32P in serial mode with V_{CCO} at 3.3V, if FPGA Data setup time = 15 ns, then the actual T_{CYCO} = 25 ns +15 ns = 40 ns.
8. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
9. Slower CLK frequency option might be required to meet the FPGA data sheet setup time.
10. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7 kΩ pull-up to V_{CCO}.
11. When JTAG CONFIG command is issued, PROM drives $\overline{CF}$ Low for at least the T_{HCF} minimum.

XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source



Note: Typically, 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.

ds123_26_110707

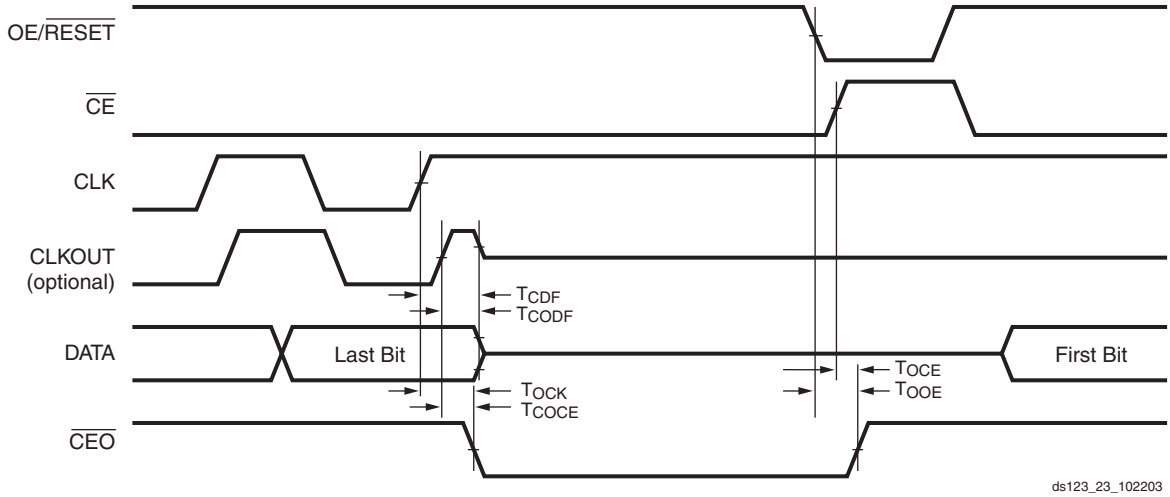
Symbol	Description	XCF08P, XCF16P, XCF32P		Units
		Min	Max	
T_{HCF}	CF hold time to guarantee design revision selection is sampled when V_{CCO} = 3.3V or 2.5V(12)	300		300
	CF hold time to guarantee design revision selection is sampled when V_{CCO} = 1.8V(12)	300		300
T_{CF}	CF to data delay when VCCO = 3.3V or 2.5V	–		ns
	CF to data delay when VCCO = 1.8V	–		ns
T_{OE}	OE/RESET to data delay(6) when V_{CCO} = 3.3V or 2.5V	–	25	ns
	OE/RESET to data delay(6) when V_{CCO} = 1.8V	–	25	ns
T_{CE}	CE to data delay(5) when V_{CCO} = 3.3V or 2.5V	–	25	ns
	CE to data delay(5) when V_{CCO} = 1.8V	–	25	ns
T_{EOH}	Data hold from CE, OE/RESET, or CF when V_{CCO} = 3.3V or 2.5V	5	–	ns
	Data hold from CE, OE/RESET, or CF when V_{CCO} = 1.8V	5	–	ns
T_{DF}	CE or OE/RESET to data float delay(2) when V_{CCO} = 3.3V or 2.5V	–	45	ns
	CE or OE/RESET to data float delay(2) when V_{CCO} = 1.8V	–	45	ns
T_{OECF}	OE/RESET to CLKOUT float delay(2) when V_{CCO} = 3.3V or 2.5V	–		ns
	OE/RESET to CLKOUT float delay(2) when V_{CCO} = 1.8V	–		ns
T_{CECF}	CE to CLKOUT float delay(2) when V_{CCO} = 3.3V or 2.5V	–		ns
	CE to CLKOUT float delay(2) when V_{CCO} = 1.8V	–		ns
T_{HCE}	CE hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	CE hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	2000	–	ns
T_{HOE}	OE/RESET hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	2000	–	ns
	OE/RESET hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	2000	–	ns

Symbol	Description	XCF08P, XCF16P, XCF32P		Units
		Min	Max	
T_{SB}	BUSY setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V	12	–	ns
	BUSY setup time to CLKOUT when V_{CCO} = 1.8V	12	–	ns
T_{HB}	BUSY hold time to CLKOUT when V_{CCO} = 3.3V or 2.5V	8	–	ns
	BUSY hold time to CLKOUT when V_{CCO} = 1.8V	8	–	ns
T_{CEC}	$\overline{CE}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0	1	µs
	$\overline{CE}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0	1	µs
T_{OEC}	OE/$\overline{RESET}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0	1	µs
	OE/$\overline{RESET}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0	1	µs
T_{CFC}	$\overline{CF}$ to CLKOUT delay(7) when V_{CCO} = 3.3V or 2.5V	0		–
	$\overline{CF}$ to CLKOUT delay(7) when V_{CCO} = 1.8V	0		–
T_{CDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V(8)	–	30	ns
	CLKOUT to data delay when V_{CCO} = 1.8V(8)	–	30	ns
T_{DDC}	Data setup time to CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(8)(11)	5		ns
	Data setup time to CLKOUT when V_{CCO} = 1.8V with decompression(8)(11)	5		ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V with decompression(11)	3	–	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V with decompression(11)	3	–	ns
T_{SXT}	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN_EXT_SEL}$ setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HXT}	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	$\overline{EN_EXT_SEL}$ hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL setup time to $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
T_{HRV}	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 3.3V or 2.5V	300	–	ns
	REV_SEL hold time from $\overline{CF}$, $\overline{CE}$, or OE/$\overline{RESET}$ when V_{CCO} = 1.8V	300	–	ns
F_F	CLKOUT default (fast) frequency(9)	25	50	MHz
	CLKOUT default (fast) frequency with decompression(11)	12.5	25	MHz
F_S	CLKOUT alternate (slower) frequency(10)	12.5	25	MHz
	CLKOUT alternate (slower) frequency with decompression(11)	6	12.5	MHz

Notes:

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
8. Slower CLK frequency option might be required to meet the FPGA data sheet setup time.
9. Typical CLKOUT default (fast) period = 25 ns (40 MHz).
10. Typical CLKOUT alternate (slower) period = 50 ns (20 MHz).
11. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7 kΩ pull-up to V_{CCO}.
12. When JTAG CONFIG command is issued, PROM drives $\overline{CF}$ Low for at least the T_{HCF} minimum.

AC Characteristics Over Operating Conditions When Cascading



Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{CDF}	CLK to output float delay(2,3) when V_{CCO} = 2.5V or 3.3V	–	25	–	20	ns
	CLK to output float delay(2,3) when V_{CCO} = 1.8V	–	35	–	20	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 2.5V or 3.3V	–	20	–	20	ns
	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 1.8V	–	35	–	20	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3,6) when V_{CCO} = 2.5V or 3.3V	–	20	–	80	ns
	$\overline{CE}$ to $\overline{CEO}$ delay(3,6) when V_{CCO} = 1.8V	–	35	–	80	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	–	20	–	80	ns
	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	–	35	–	80	ns
T_{COCE}	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 2.5V or 3.3V	–	–	–	20	ns
	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 1.8V	–	–	–	20	ns
T_{CODF}	CLKOUT to output float delay when V_{CCO} = 2.5V or 3.3V	–	–	–	25	ns
	CLKOUT to output float delay when V_{CCO} = 1.8V	–	–	–	25	ns

Notes:

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins are set to persist as configuration pins, the minimum period is increased based on the CLK to $\overline{CEO}$ and $\overline{CE}$ to data propagation delays:
   - T_{CYC} minimum = T_{OCK} + T_{CE} + FPGA Data setup time
   - T_{CAC} maximum = T_{OCK} + T_{CE}
6. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins become general I/O pins after configuration; to allow for the disable to propagate to the cascaded PROMs and to avoid contention on the data lines following configuration, the minimum period is increased based on the $\overline{CE}$ to $\overline{CEO}$ and $\overline{CE}$ to data propagation delays:
   - T_{CYC} minimum = T_{OCE} + T_{CE}
   - T_{CAC} maximum = T_{OCK} + T_{CE}

Pinouts and Pin Descriptions

The XCFxxS Platform Flash PROM is available in the VO20 and VOG20 packages. The XCFxxP Platform Flash PROM is available in the VO48, VOG48, FS48, and FSG48 packages. For package drawings, specifications, and additional information, see UG112, *Device Package User Guide*, or the Xilinx Package Specifications.

Note:

1. VO20/VOG20 denotes a 20-pin (TSSOP) Plastic Thin Shrink Small Outline Package.
2. VO48/VOG48 denotes a 48-pin (TSOP) Plastic Thin Small Outline Package.
3. FS48/FSG48 denotes a 48-pin (TFBGA) Plastic Thin Fine Pitch Ball Grid Array (0.8 mm pitch).

XCFxxS Pinouts and Pin Descriptions

XCFxxS VO20/VOG20 Pin Names and Descriptions

Table 12 provides a list of the pin names and descriptions for the XCFxxS 20-pin VO20/VOG20 package.

Table 12: **XCFxxS Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary-Scan Function	Pin Description	20-pin TSSOP (VO20/VOG20)
D0	4	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).	1
	3	Output Enable		
CLK	0	Data In	Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High.	3
OE/$\overline{RESET}$	20	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.	8
	19	Data Out		
	18	Output Enable		
$\overline{CE}$	15	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.	10
$\overline{CF}$	22	Data Out	Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	7
	21	Output Enable		
$\overline{CEO}$	12	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	13
	11	Output Enable		
TMS	–	Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	5
TCK	–	Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	6
TDI	–	Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	4

Table 12: **XCFxxS Pin Names and Descriptions *(Cont'd)***

Pin Name	Boundary Scan Order	Boundary-Scan Function	Pin Description	20-pin TSSOP (VO20/VOG20)
TDO	–	Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the system if the pin is not driven.	17
VCCINT	–	–	+3.3V Supply. Positive 3.3V supply voltage for internal logic.	18
VCCO	–	–	+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	19
VCCJ	–	–	+3.3V or 2.5V JTAG I/O Supply. Positive 3.3V or 2.5V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	20
GND	–	–	Ground	11
DNC	–	–	Do not connect. (These pins must be left unconnected.)	2, 9, 12, 14, 15, 16

XCFxxS VO20/VOG20 Pinout Diagram

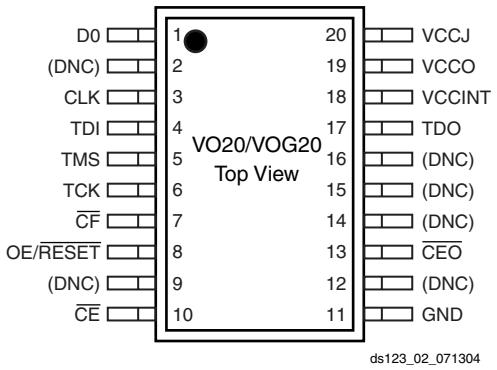


Figure 11: **VO20/VOG20 Pinout Diagram (Top View) with Pin Names**

XCFxxP Pinouts and Pin Descriptions

XCFxxP VO48/VOG48 and FS48/FSG48 Pin Names and Descriptions

Table 13 provides a list of the pin names and descriptions for the XCFxxP 48-pin VO48/VOG48 and 48-pin FS48/FSG48 packages.

Table 13: **XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48)**

Pin Name	Boundary-Scan Order	Boundary-Scan Function	Pin Description	48-pin TSOP (VO48/VOG48)	48-pin TFBGA (FS48/FSG48)
D0	28	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. D0-D7 are the DATA output pins to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped). The D1-D7 outputs are set to a high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. The D1-D7 pins can be left unconnected when the PROM is used in serial mode.	28	H6
	27	Output Enable			
D1	26	Data Out		29	H5
	25	Output Enable			
D2	24	Data Out		32	E5
	23	Output Enable			
D3	22	Data Out		33	D5
	21	Output Enable			
D4	20	Data Out		43	C5
	19	Output Enable			
D5	18	Data Out		44	B5
	17	Output Enable			
D6	16	Data Out		47	A5
	15	Output Enable			
D7	14	Data Out		48	A6
	13	Output Enable			
CLK	01	Data In	Configuration Clock Input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, OE/$\overline{RESET}$ is High, BUSY is Low (parallel mode only), and $\overline{CF}$ is High.	12	B3
OE/$\overline{RESET}$	04	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.	11	A3
	03	Data Out			
	02	Output Enable			
$\overline{CE}$	00	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high-impedance state.	13	B4
$\overline{CF}$	11	Data In	Configuration Pulse (Open-Drain I/O). As an output, this pin allows the JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain signal that is pulsed Low by the JTAG CONFIG command. As an input, on the rising edge of $\overline{CF}$, the current design revision selection is sampled and the internal address counter is reset to the start address for the selected revision. If unused, the $\overline{CF}$ pin must be pulled High using an external 4.7 kΩ pull-up to V_{CCO}.	6	D1
	10	Data Out			
	09	Output Enable			

Table 13: **XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) *(Cont'd)***

Pin Name	Boundary-Scan Order	Boundary-Scan Function	Pin Description	48-pin TSOP (VO48/VOG48)	48-pin TFBGA (FS48/FSG48)
$\overline{CEO}$	06	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value or the PROM does not contain any blocks that correspond to the selected revision. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	10	D2
	05	Output Enable			
$\overline{EN_EXT_SEL}$	31	Data In	Enable External Selection Input. When this pin is Low, design revision selection is controlled by the Revision Select pins. When this pin is High, design revision selection is controlled by the internal programmable Revision Select control bits. $\overline{EN_EXT_SEL}$ has an internal 50 kΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pin is not driven.	25	H4
REV_SEL0	30	Data In	Revision Select[1:0] Inputs. When the $\overline{EN_EXT_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmable Revision Select control bits. The Revision Select[1:0] inputs have an internal 50 kΩ resistive pull-up to V_{CCO} to provide a logic 1 to the device if the pins are not driven.	26	G3
REV_SEL1	29	Data In		27	G4
BUSY	12	Data In	Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge of CLK after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50 kΩ resistive pull-down to GND to provide a logic 0 to the device if the pin is not driven.	5	C1
CLKOUT	08	Data Out	Configuration Clock Output. An internal Programmable control bit enables the CLKOUT signal, which is sourced from either the internal oscillator or the CLK input pin. Each rising edge of the selected clock source increments the internal address counter if data is available, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High. Output data is available on the rising edge of CLKOUT. CLKOUT is disabled if $\overline{CE}$ is High or OE/$\overline{RESET}$ is Low. If decompression is enabled, CLKOUT is parked High when decompressed data is not ready. When CLKOUT is disabled, the CLKOUT pin is put into a high-Z state. If CLKOUT is used, then it must be pulled High externally using a 4.7 kΩ pull-up to V_{CCO}.	9	C2
	07	Output Enable			
TMS	–	Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	21	E2
TCK	–	Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	20	H3
TDI	–	Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the device if the pin is not driven.	19	G1
TDO	–	Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 kΩ resistive pull-up to V_{CCJ} to provide a logic 1 to the system if the pin is not driven.	22	E6

Table 13: **XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) *(Cont'd)***

Pin Name	Boundary-Scan Order	Boundary-Scan Function	Pin Description	48-pin TSOP (VO48/VOG48)	48-pin TFBGA (FS48/FSG48)
VCCINT	–	–	+1.8V Supply. Positive 1.8V supply voltage for internal logic.	4, 15, 34	B1, E1, G6
VCCO	–	–	+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	8, 30, 38, 45	B2, C6, D6, G5
VCCJ	–	–	+3.3V or 2.5V JTAG I/O Supply. Positive 3.3V or 2.5V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	24	H2
GND	–	–	Ground	2, 7, 17, 23, 31, 36, 46	A1, A2, B6, F1, F5, F6, H1
DNC	–	–	Do Not Connect. (These pins must be left unconnected.)	1, 3, 14, 16, 18, 35, 37, 39, 40, 41, 42	A4, C3, C4, D3, D4, E3, E4, F2, F3, F4, G2

XCFxxP VO48/VOG48 Pinout Diagram

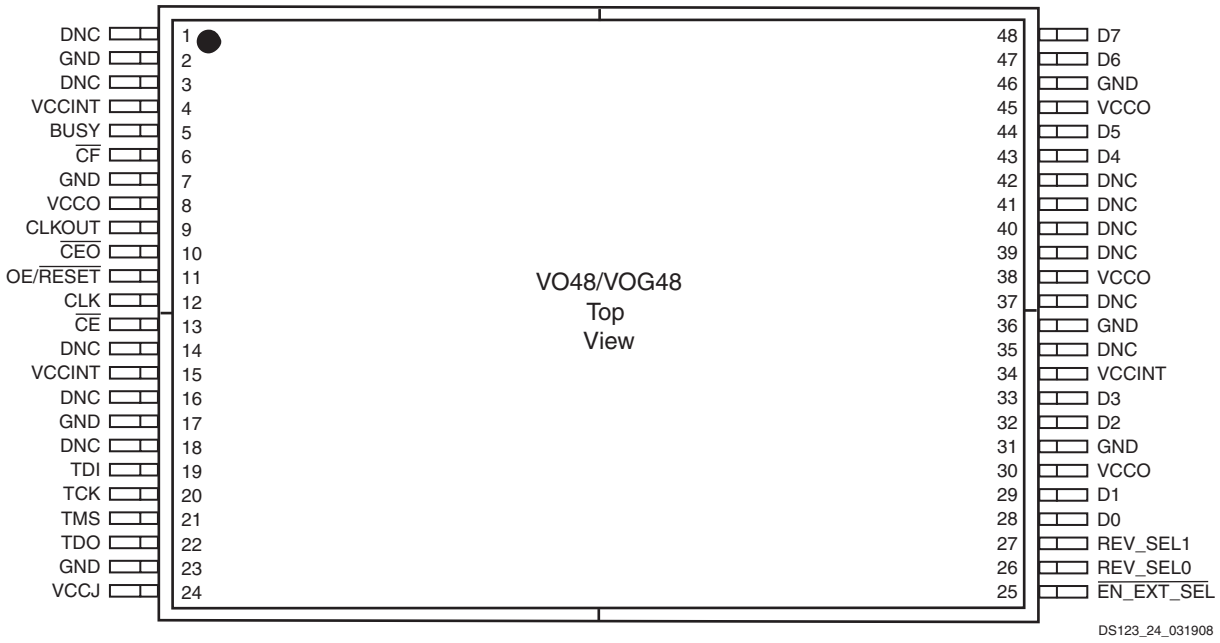


Figure 12: **VO48/VOG48 Pinout Diagram (Top View) with Pin Names**

XCFxxP FS48/FSG48 Pin Names

Table 14: **XCFxxP Pin Names (FS48/FSG48)**

Pin Number	Pin Name	Pin Number	Pin Name
A1	GND	E1	VCCINT
A2	GND	E2	TMS
A3	OE/$\overline{\text{RESET}}$	E3	DNC
A4	DNC	E4	DNC
A5	D6	E5	D2
A6	D7	E6	TDO
B1	VCCINT	F1	GND
B2	VCCO	F2	DNC
B3	CLK	F3	DNC
B4	$\overline{\text{CE}}$	F4	DNC
B5	D5	F5	GND
B6	GND	F6	GND
C1	BUSY	G1	TDI
C2	CLKOUT	G2	DNC
C3	DNC	G3	REV_SEL0
C4	DNC	G4	REV_SEL1
C5	D4	G5	VCCO
C6	VCCO	G6	VCCINT
D1	$\overline{\text{CF}}$	H1	GND
D2	$\overline{\text{CEO}}$	H2	VCCJ
D3	DNC	H3	TCK
D4	DNC	H4	$\overline{\text{EN_EXT_SEL}}$
D5	D3	H5	D1
D6	VCCO	H6	D0

XCFxxP FS48/FSG48 Pinout Diagram

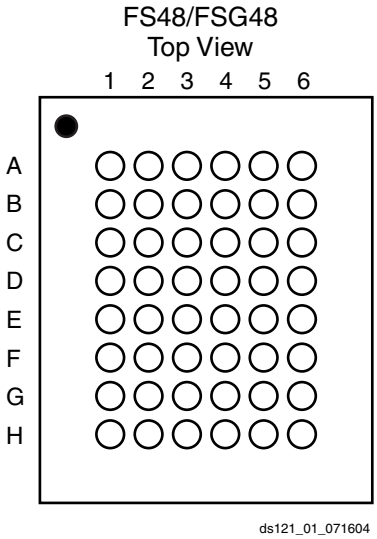


Figure 13: **FS48/FSG48 Pinout Diagram (Top View)**

Ordering Information

XCF04S VO20 C

Device Number
XCF01S
XCF02S
XCF04S

Package Type
VO20 = 20-pin TSSOP Package
VOG20 = 20-pin TSSOP Package, Pb-free

Operating Range/Processing
C = Industrial (T_A = –40°C to +85°C)

DS123_27_112407

XCF32P FS48 C

Device Number
XCF08P
XCF16P
XCF32P

Package Type
VO48 = 48-pin TSOP Package
VOG48 = 48-pin TSOP Package, Pb-free
FS48 = 48-pin TFBGA Package
FSG48 = 48-pin TFBGA Package, Pb-free

Operating Range/Processing
C = Industrial (T_A = –40°C to +85°C)

DS123_28_112407

Valid Ordering Combinations

XCF01SVO20C	XCF08PFS48C	XCF01SVOG20C	XCF08PVOG48C	XCF08PFSG48C
XCF02SVO20C	XCF16PFS48C	XCF02SVOG20C	XCF16PVOG48C	XCF16PFSG48C
XCF04SVO20C	XCF32PFS48C	XCF04SVOG20C	XCF32PVOG48C	XCF32PFSG48C

Marking Information

XCF04S V

Device Number
XCF01S
XCF02S
XCF04S
XCF08P
XCF16P
XCF32P

Package Type
V = 20-pin TSSOP Package (VO20)
VG = 20-pin TSSOP Package, Pb-free (VOG20)
VO48 = 48-pin TSOP Package (VO48)
VOG48 = 48-pin TSOP Package, Pb-free (VOG48)
F48 = 48-pin TFBGA Package (FS48)
FG48 = 48-pin TFBGA Package, Pb-free (FSG48)

Operating Range/Processing
[No Mark] = Industrial (T_A = –40°C to +85°C)

DS123_29_112407

Figure 14 through Figure 16 illustrate the part markings for each available package.

Note: Package types can differ from the samples shown.

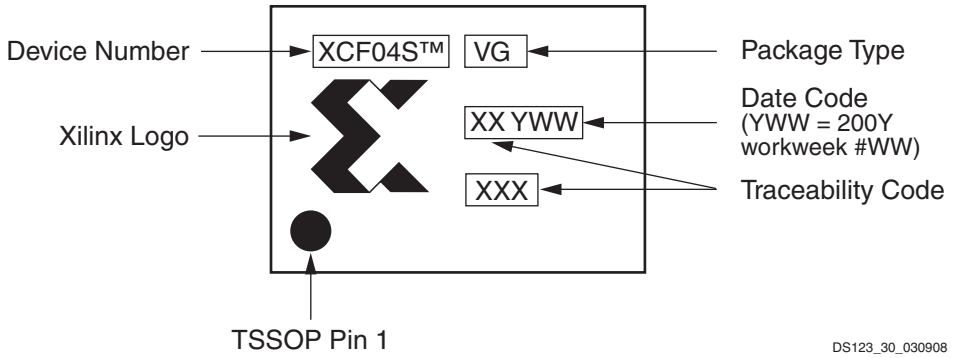


Figure 14: **20-Pin TSSOP Marking**

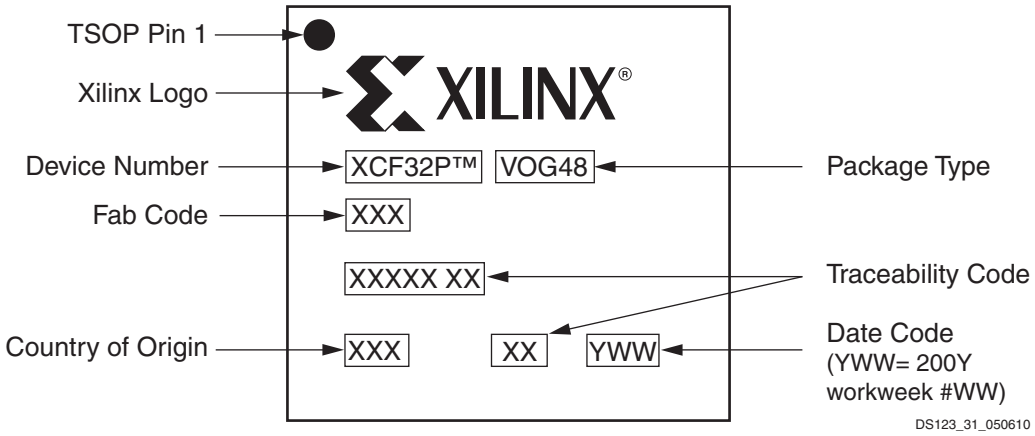


Figure 15: **48-Pin TSOP Marking**

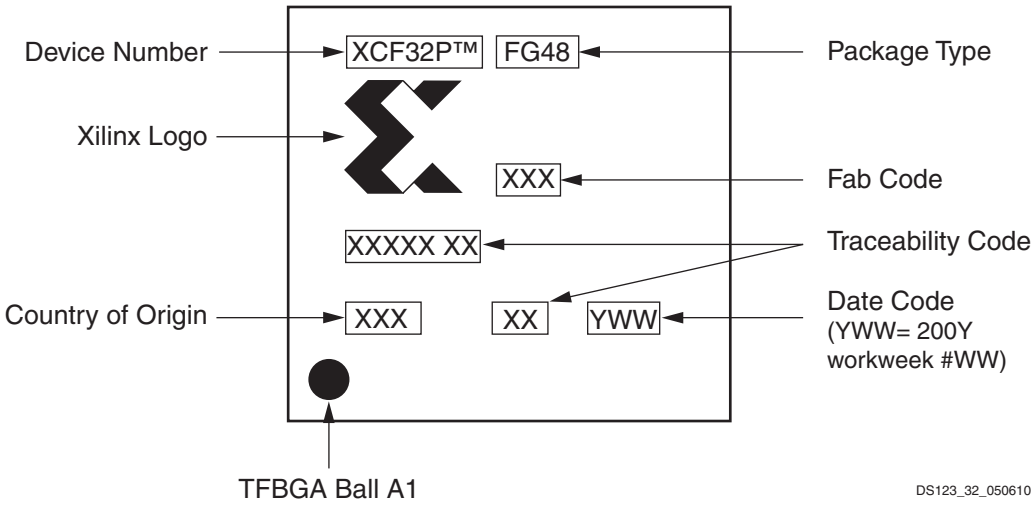


Figure 16: **48-Pin TFBGA Marking**

Note: In Figure 15 and Figure 16, the two-digit traceability code on the bottom line between the country of origin and date code is not present on all devices.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/29/03	1.0	Xilinx Initial Release.
06/03/03	1.1	Made edits to all pages.
11/05/03	2.0	Major revision.

11/18/03	2.1	Pinout corrections as follows:
		• Table 13:
		  • For VO48 package, removed 38 from VCCINT and added it to VCCO.
		  • For FS48 package, removed pin D6 from VCCINT and added it to VCCO.
		• Table 14 (FS48 package):
		  • For pin D6, changed name from VCCINT to VCCO.
		  • For pin A4, changed name from GND to DNC.
		• Figure 8 (VO48 package): For pin 38, changed name from VCCINT to VCCO.

12/15/03	2.2	• Added specification (4.7kΩ) for recommended pull-up resistor on OE/$\overline{\text{RESET}}$ pin to section "Reset and Power-On Reset Activation," page 11. • Added paragraph to section "Standby Mode," page 12, concerning use of a pull-up resistor and/or buffer on the DONE pin.

05/07/04	2.3	• Section "Features," page 1: Added package styles and 33 MHz configuration speed limit to itemized features.
		• Section "Description," page 1 and following: Added state conditions for $\overline{\text{CF}}$ and BUSY to the descriptive text.
		• Table 2, page 3: Updated Virtex®-II configuration bitstream sizes.
		• Section "Design Revisioning," page 8: Rewritten.
		• Section "Initiating FPGA Configuration," page 10 and following, five instances: Added instruction to tie $\overline{\text{CF}}$ High if it is not tied to the FPGA's PROG_B ($\overline{\text{PROGRAM}}$) input.
		• Figure 6, page 16, through Figure 13, page 23: Added footnote indicating the directionality of the $\overline{\text{CF}}$ pin in each configuration.
		• Section "I/O Input Voltage Tolerance and Power Sequencing," page 11: Rewritten.
		• Table 12, page 25: Added $\overline{\text{CF}}$ column to truth table, and added an additional row to document the Low state of $\overline{\text{CF}}$.
		• Section "Absolute Maximum Ratings," page 13: Revised V_{IN} and V_{TS} for 'P' devices.
		• Section "Supply Voltage Requirements for Power-On Reset and Power-Down," page 13:
		  • Revised footnote callout number on T_{OER} from Footnote (4) to Footnote (3).
		  • Added Footnote (2) callout to T_{VCC}.
		• Section "Recommended Operating Conditions," page 14:
		  • Added Typical (Typ) parameter columns and parameters for V_{CCINT} and V_{CCO}/V_{CCJ}.
		  • Added 1.5V operation parameter row to V_{IL} and V_{IH}, 'P' devices.
		  • Revised V_{IH} Min, 2.5V operation, from 2.0V to 1.7V.
		  • Added parameter row T_{IN} and Max parameters
		• (Continued on next page)
		• Section "DC Characteristics Over Operating Conditions," page 15:
		  • Added parameter row and parameters for parallel configuration mode, 'P' devices, to I_{CCO}.
		  • Added Footnote (1) and Footnote (2) with callouts in the Test Conditions column for I_{CCJ}, I_{CCINTS}, I_{CCOS}, and I_{CCJS}, to define active and standby mode requirements.
		• Section "AC Characteristics Over Operating Conditions," page 16:
		  • Corrected description for second T_{CAC} parameter line to show parameters for 1.8V V_{CCO}.
		  • Revised Footnote (7) to indicate V_{CCO} = 3.3V.
		  • Applied Footnote (7) to second T_{CYC} parameter line.
		• Section "AC Characteristics Over Operating Conditions When Cascading," page 23: Revised Footnote (5)T_{CYC} Min and T_{CAC} Min formulas.
		• Table 14, page 39:
		  • Added additional state conditions to CLK description.
		  • Added function of resetting the internal address counter to $\overline{\text{CF}}$ description.

Date	Version	Revision
07/20/04	2.4	• Added Pb-free package options VOG20, FSG48, and VOG48. • Figure 6, page 16, and Figure 7, page 17: Corrected connection name for FPGA DOUT (OPTIONAL Daisy-chained Slave FPGAs with different configurations) from DOUT to DIN. • Section "Absolute Maximum Ratings," page 13: Removed parameter T_{SOL} from table. (T_{SOL} information can be found in *Package User Guide*.) • Table 2, page 3: Removed reference to XC2VP125 FPGA.

10/18/04	2.5	• Table 1, page 1: Broke out V_{CCO} / V_{CCJ} into two separate columns.
		• Table 9, page 9: Added clarification of ID code die revision bits.
		• Table 10, page 10: Deleted T_{CKMIN2} (bypass mode) and renamed T_{CKMIN1} to T_{CKMIN}.
		• Table "Recommended Operating Conditions," page 14: Separated V_{CCO} and V_{CCJ} parameters.
		• Table "DC Characteristics Over Operating Conditions," page 15:
		  • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
		  • Added Footnote (1) to I_{CCO} specifying no-load conditions.
		• Table "AC Characteristics Over Operating Conditions," page 16:
		  • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
		  • Expanded Footnote (1) to include XCF08P, XCF16P, XCF32P devices.
		  • Added Footnote (8) through (11) relating to CLKOUT conditions for various parameters.
		  • Added rows to T_{CYC} specifying parameters for parallel mode.
		  • Added rows specifying parameters with decompression for T_{CLKO}, T_{COH}, T_{FF}, T_{SF}.
		  • Added T_{DDC} (setup time with decompression).
		• Table "AC Characteristics Over Operating Conditions When Cascading," page 23:
		  • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
		  • Separated Footnote (5) into Footnotes (5) and (6) to specify different derivations of T_{CYC}, depending on whether dual-purpose configuration pins persist as configuration pins, or become general I/O pins after configuration.

03/14/05	2.6	• Added Virtex-4 LX/FX/SX configuration data to Table 2.
		• Corrected Virtex-II configuration data in Table 2.
		• Corrected Virtex-II Pro configuration data in Table 2.
		• Added Spartan®-3L configuration data to Table 2.
		• Added Spartan-3E configuration data to Table 2.
		• Paragraph added to *FPGA Master SelectMAP (Parallel) Mode (1)*.
		• Changes to DC Characteristics
		  • T_{OER} changed, Page 15.
		  • I_{OL} changed for V_{OL}, Page 15.
		  • V_{CCO} added to test conditions for I_{IL}, I_{ILP}, I_{IHP} and II_H, Page 15. Values modified for I_{ILP} and I_{IHP}.
		• Changes to AC Characteristics
		  • T_{LC} and T_{HC} modified for 1.8V, Page 19.
		  • New rows added for T_{CEC} and T_{OEC}, Page 18.
		• Minor changes to grammar and punctuation.
		• Added explanation of "Preliminary" to DC and AC Electrical Characteristics.

07/11/05	2.7	• Move from "Preliminary" to "Product Specification" • Corrections to Virtex-4 configuration bitstream values • Minor changes to Figure 7, page 17, Figure 12, page 22, Figure 13, page 23, and Figure 16, page 31 • Change to "Internal Oscillator," page 8 description • Change to "CLKOUT," page 8 description
12/29/05	2.8	• Update to the first paragraph of "IEEE 1149.1 Boundary-Scan (JTAG)," page 5. • Added JTAG cautionary note to Page 5. • Corrected logic values for Erase/Program (ER/PROG) Status field, IR[4], listed under "XCFxxP Instruction Register (16 bits wide)," page 5. • Sections "XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source," page 16, "XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source," page 18 and "XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source," page 21 added to "AC Characteristics Over Operating Conditions," page 16.

Date	Version	Revision
12/29/05 (Cont'd)	2.8	• Notes for Figure 6, page 16, Figure 7, page 17, Figure 8, page 18, Figure 9, page 19, Figure 10, page 20, Figure 11, page 21, Figure 12, page 22, and Figure 13, page 23 updated to specify the need for a pull-up resistor if $\overline{CF}$ is not connected to PROGB. • Enhanced description under section "CLKOUT," page 8. • Enhanced description on design revision sampling under section "Design Revisioning," page 8. • Figure 4 and Figure 5 renamed to Table 7, page 8 and Table 8, page 8 respectively. All tables, figures, and table and figure references renumber this point forward. • Value for "ICCINT," page 15 updated from 5mA to 1mA for XCFxxP. • Block diagram in Figure 2, page 2 updated to show clock source muxing and route clocking to all functional blocks.
05/09/06	2.9	• Added Virtex-5 LX support to Table 2. • "VIL" maximum for 2.5V operation in "Recommended Operating Conditions," page 14 updated to match LVCMOS25 standard.
12/08/06	2.10	• Added Virtex-5 LXT support to Table 2. • Defined reprogramming operation requirements in "Programming," page 3. • Corrected statements regarding the FPGA BUSY pin and corrected various references.
02/01/07	2.11	• Removed Spartan-3L support and added Spartan-3A and Virtex-5 SXT support to Table 2. • Corrected Spartan-3E bitstream sizes in Table 2. • Correct supported voltages for "VCCJ" in Table 12, page 24, "VCCO" and "VCCJ" in Table 13, page 26.
03/30/07	2.11.1	Added Spartan-3A DSP support to Table 2.
01/28/08	2.12	• Added support for XC5VLX155, XC5VLX20T, and XC5VLX155T. • Updated JTAG TAP timing specifications in Table 9, page 7 to reflect improved performance. • Tied FPGA CS_B and FPGA RDWR_B to GND in the FPGA SelectMAP schematics to ensure valid logic Low. • Hardwired external oscillator to FPGA CCLK in the FPGA slave mode schematics. • Added marking templates (Figure 14, page 31, Figure 15 and Figure 16), and corrected marks for 48-pin TFBGA packages in "Marking Information," page 30. • Other edits and updates made. • Updated document template. • Updated URLs.
03/31/08	2.13	• Added Virtex-5 FX FPGA support to Table 2. • Corrected markings for all packaging (Figure 14, page 31, Figure 15, and Figure 16). • Added note regarding variances in packaging and marking to Page 31.
04/03/08	2.13.1	• Corrected typo. • Updated trademark notations.
05/14/08	2.14	Added support for XC5VSX240T and Platform Flash XL to Table 2.
07/07/08	2.15	Updated "Write Protection," page 4.
11/14/08	2.16	Added Virtex-5 TXT FPGA to Table 2.

10/26/09	2.17	• Globally changed PROG_B and $\overline{PROGRAM}$ to PROGRAM_B.
		• Removed the following information from this data sheet to UG161, *Platform Flash PROM User Guide:*
		  • Table 2 entitled "Xilinx FPGAs and Compatible Platform Flash PROMs"
		  • Section entitled "PROM to FPGA Configuration Mode and Connections Summary"
		  • Section entitled "Configuration PROM-to-FPGA Device Interface Connection Diagrams"
		• Moved "up to 33 MHz" from FPGA Configuration Interface bullets in "Features," page 1 to "Description," page 1, and added reference to related considerations.
		• Table 1, page 1: Changed lower bound on V_{CCO} for XCF08P, XCF16P, and XCF32P devices from 1.5V to 1.8V. Added table note 1 about design revisioning for the XCF08P.
		• Added statement about ignoring non-JTAG input pins to second paragraph of "In-System Programming," page 3.
		• Added reference to *Platform Flash PROM User Guide* in "External Programming," page 3 and "Internal Oscillator," page 8.

Date	Version	Revision
10/26/09	2.17 *(Cont'd)*	• Updated text in second and third bulleted items in "Initiating FPGA Configuration," page 10. • Removed all references to 1.5V operation from "Features," page 1, "Recommended Operating Conditions," page 14, "DC Characteristics Over Operating Conditions," page 15, and Table 13, page 26.
05/19/10	2.18	Removed ordering codes for discontinued VO48 package from "Valid Ordering Combinations" (see XCN09030). Added note to Figure 15 and Figure 16 describing traceability code in top mark (see XCN08005).

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