Low Power, Wide Supply Range, Low Cost Difference Amplifiers, G = ½, 2

AD8278/AD8279

FEATURES

Wide input range beyond supplies
Rugged input overvoltage protection
Low supply current: 200 µA maximum (per amplifier)
Low power dissipation: 0.5 mW at V_S = 2.5 V
Bandwidth: 1 MHz (G = ½)
CMRR: 80 dB minimum, dc to 20 kHz (G = ½, B Grade)
Low offset voltage drift: ±1 µV/°C maximum (B Grade)
Low gain drift: 1 ppm/°C maximum (B Grade)
Enhanced slew rate: 1.4 V/µs
Wide power supply range
  Single supply: 2 V to 36 V
  Dual supplies: ±2 V to ±18 V
8-lead SOIC, 14-lead SOIC, and 8-lead MSOP packages

APPLICATIONS

Voltage measurement and monitoring
Current measurement and monitoring
Instrumentation amplifier building block
Portable, battery-powered equipment
Test and measurement

GENERAL DESCRIPTION

The AD8278 and AD8279 are general-purpose difference amplifiers intended for precision signal conditioning in power critical applications that require both high performance and low power. The AD8278 and AD8279 provide exceptional common-mode rejection ratio (80 dB) and high bandwidth while amplifying input signals that are well beyond the supply rails. The on-chip resistors are laser trimmed for excellent gain accuracy and high CMRR. They also have extremely low gain drift vs. temperature.

The common-mode range of the amplifier extends to almost triple the supply voltage (for G = ½), making the amplifer ideal for single-supply applications that require a high common-mode voltage range. The internal resistors and ESD circuitry at the inputs also provide overvoltage protection to the op amp.

The AD8278 and AD8279 can be used as difference amplifiers with G = ½ or G = 2. They can also be connected in a high precision, single-ended configuration for non inverting and inverting gains of −½, −2, +3, +2, +1½, +1, or +½. The AD8278 and AD8279 provide an integrated precision solution that has a smaller size, lower cost, and better performance than a discrete alternative.

The AD8278 and AD8279 operate on single supplies (2.0 V to 36 V) or dual supplies (±2 V to ±18 V). The maximum quiescent supply current is 200 µA, which is ideal for battery-operated and portable systems. For unity-gain difference amplifiers with similar performance, refer to the AD8276 and AD8277 data sheets.

FUNCTIONAL BLOCK DIAGRAMS

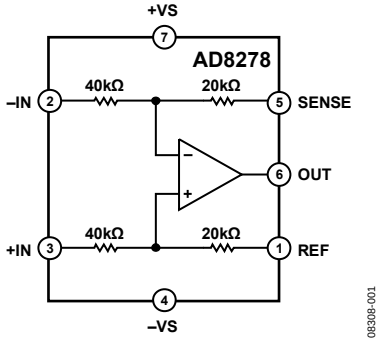


Figure 1. AD8278

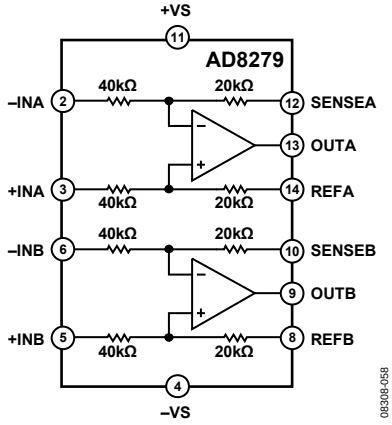


Figure 2. AD8279

Table 1. Difference Amplifiers by Category

Low Distortion	High Voltage	Current Sensing[1]	Low Power
AD8270	AD628	AD8202 (U)	AD8276
AD8271	AD629	AD8203 (U)	AD8277
AD8273		AD8205 (B)	
AD8274		AD8206 (B)	
AMP03		AD8216 (B)	

[1]U = unidirectional, B = bidirectional.

The AD8278 is available in the space-saving 8-lead MSOP and SOIC packages, and the AD8279 is offered in a 14-lead SOIC package. Both are specified for performance over the industrial temperature range of −40°C to +85°C and are fully RoHS compliant.

Rev. C
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2009–2011 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

1/11—Rev. B to Rev. C

Change to Impedance/Differential Parameter, Table 3 ... 4
Change to Impedance/Differential Parameter, Table 5 ... 6

4/10—Rev. A to Rev. B

Changed Supply Current Parameters to AD8278 Supply Current Parameter and AD8279 Supply Current Parameter, Table 5 ... 6
Updated Outline Dimensions ... 20

10/09—Rev. 0 to Rev. A

Added AD8279 and 14-Lead SOIC Model ... Universal
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7/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V to ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = ½ difference amplifier configuration, unless otherwise noted.

Table 2.

		G = ½						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			50	100		50	250	µV
Over Temperature	T_A = −40°C to +85°C			100			250	µV
vs. Power Supply	V_S = ±5 V to ±18 V			2.5			5	µV/V
Average Temperature Coefficient	T_A = −40°C to +85°C		0.3	1		2	5	µV/°C
Common-Mode Rejection Ratio (RTI)	V_S = ±15 V, V_{CM} = ±27 V, R_S = 0 Ω	80			74			dB
Input Voltage Range[2]		−3 (V_S + 0.1)		+3 (V_S − 1.5)	−3 (V_S + 0.1)		+3 (V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			1			1		MHz
Slew Rate		1.1	1.4		1.1	1.4		V/µs
Channel Separation	f = 1 kHz		130			130		dB
Settling Time to 0.01%	10 V step on output, C_L = 100 pF			9			9	µs
Settling Time to 0.001%				10			10	µs
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
Gain Nonlinearity	V_{OUT} = 20 V p-p			7			12	ppm
OUTPUT CHARACTERISTICS								
Output Voltage Swing[4]	V_S = ±15 V, R_L = 10 kΩ T_A = −40°C to +85°C	−V_S + 0.2		+V_S − 0.2	−V_S + 0.2		+V_S − 0.2	V
Short-Circuit Current Limit			±15			±15		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		1.4			1.4		µV p-p
	f = 1 kHz		47	50		47	50	nV/√Hz
POWER SUPPLY[6]								
AD8278 Supply Current				200			200	µA
Over Temperature	T_A = −40°C to +85°C			250			250	µA
AD8279 Supply Current			300	350		300	350	µA
Over Temperature	T_A = −40°C to +85°C			400			400	µA
Operating Voltage Range[7]		±2		±18	±2		±18	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 22 through Figure 25 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 26 and Figure 28 for details.
[7] Unbalanced dual supplies can be used, such as −V_S = −0.5 V and +V_S = +2 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

V_S = ±5 V to ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = 2 difference amplifier configuration, unless otherwise noted.

Table 3.

		G = 2						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			100	200		100	500	µV
Over Temperature	T_A = −40°C to +85°C			200			500	µV
vs. Power Supply	V_S = ±5 V to ±18 V			5			10	µV/V
Average Temperature Coefficient	T_A = −40°C to +85°C		0.6	2		2	5	µV/°C
Common-Mode Rejection Ratio (RTI)	V_S = ±15 V, V_{CM} = ±27 V, R_S = 0 Ω	86			80			dB
Input Voltage Range[2]		−1.5 (V_S + 0.1)		+1.5 (V_S − 1.5)	−1.5 (V_S + 0.1)		+1.5 (V_S − 1.5)	V
Impedance[3]								
Differential			30			30		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			550			550		kHz
Slew Rate		1.1	1.4		1.1	1.4		V/µs
Channel Separation	f = 1 kHz		130			130		dB
Settling Time to 0.01%	10 V step on output, C_L = 100 pF			10			10	µs
Settling Time to 0.001%				11			11	µs
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
Gain Nonlinearity	V_{OUT} = 20 V p-p			7			12	ppm
OUTPUT CHARACTERISTICS								
Output Voltage Swing[4]	V_S = ±15 V, R_L = 10 kΩ, T_A = −40°C to +85°C	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	V
Short-Circuit Current Limit			±15			±15		mA
Capacitive Load Drive			350			350		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		2.8			2.8		µV p-p
	f = 1 kHz		90	95		90	95	nV/√Hz
POWER SUPPLY[6]								
AD8278 Supply Current				200			200	µA
Over Temperature	T_A = −40°C to +85°C			250			250	µA
AD8279 Supply Current			300	350		300	350	µA
Over Temperature	T_A = −40°C to +85°C			400			400	µA
Operating Voltage Range[7]		±2		±18	±2		±18	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 22 through Figure 25 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 26 and Figure 28 for details.
[7] Unbalanced dual supplies can be used, such as $-V_S$ = −0.5 V and $+V_S$ = +2 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

V_S = +2.7 V to <±5 V, V_{REF} = midsupply, T_A = 25°C, R_L = 10 kΩ connected to midsupply, G = ½ difference amplifier configuration, unless otherwise noted.

Table 4.

		G = ½						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			75	150		75	250	µV
Over Temperature	T_A = −40°C to +85°C			150			250	µV
vs. Power Supply	V_S = ±5 V to ±18 V			2.5			5	µV/V
Average Temperature Coefficient	T_A = −40°C to +85°C		0.3	1		2	5	µV/°C
Common-Mode Rejection Ratio (RTI)	V_S = 2.7 V, V_{CM} = 0 V to 2.4 V, R_S = 0 Ω	80			74			dB
	V_S = ±5 V, V_{CM} = −10 V to +7 V, R_S = 0 Ω	80			74			dB
Input Voltage Range[2]		−3 (V_S + 0.1)		+3 (V_S − 1.5)	−3 (V_S + 0.1)		+3 (V_S − 1.5)	V
Impedance[3]								
Differential			120			120		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			870			870		kHz
Slew Rate			1.3			1.3		V/µs
Channel Separation	f = 1 kHz		130			130		dB
Settling Time to 0.01%	2 V step on output, C_L = 100 pF, V_S = 2.7 V		7			7		µs
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
OUTPUT CHARACTERISTICS								
Output Swing[4]	R_L = 10 kΩ, T_A = −40°C to +85°C	$-V_S$ + 0.1		$+V_S$ − 0.15	$-V_S$ + 0.1		$+V_S$ − 0.15	V
Short-Circuit Current Limit			±10			±10		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		1.4			1.4		µV p-p
	f = 1 kHz		47	50		47	50	nV/√Hz
POWER SUPPLY[6]								
AD8278 Supply Current	T_A = −40°C to +85°C			200			200	µA
AD8279 Supply Current	T_A = −40°C to +85°C			375			375	µA
Operating Voltage Range		2.0		36	2.0		36	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 22 through Figure 25 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 27 and Figure 28 for details.

V_S = +2.7 V to <±5 V, V_{REF} = midsupply, T_A = 25°C, R_L = 10 kΩ connected to midsupply, G = 2 difference amplifier configuration, unless otherwise noted.

Table 5.

		G = 2						
		Grade B			Grade A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
System Offset[1]			150	300		150	500	µV
Over Temperature	T_A = −40°C to +85°C			300			500	µV
vs. Power Supply	V_S = ±5 V to ±18 V			5			10	µV/V
Average Temperature Coefficient	T_A = −40°C to +85°C		0.6	2		3	5	µV/°C
Common-Mode Rejection Ratio (RTI)	V_S = 2.7 V, V_{CM} = 0 V to 2.4 V, R_S = 0 Ω	86			80			dB
	V_S = ±5 V, V_{CM} = −10 V to +7 V, R_S = 0 Ω	86			80			dB
Input Voltage Range[2]		−1.5 (V_S + 0.1)		+1.5 (V_S − 1.5)	−1.5 (V_S + 0.1)		+1.5 (V_S − 1.5)	V
Impedance[3]								
Differential			30			30		kΩ
Common Mode			30			30		kΩ
DYNAMIC PERFORMANCE								
Bandwidth			450			450		kHz
Slew Rate			1.3			1.3		V/µs
Channel Separation	f = 1 kHz		130			130		dB
Settling Time to 0.01%	2 V step on output, C_L = 100 pF, V_S = 2.7 V		9			9		µs
GAIN								
Gain Error			0.005	0.02		0.01	0.05	%
Gain Drift	T_A = −40°C to +85°C			1			5	ppm/°C
OUTPUT CHARACTERISTICS								
Output Swing[4]	R_L = 10 kΩ, T_A = −40°C to +85°C	$-V_S$ + 0.1		$+V_S$ − 0.15	$-V_S$ + 0.1		$+V_S$ − 0.15	V
Short-Circuit Current Limit			±10			±10		mA
Capacitive Load Drive			200			200		pF
NOISE[5]								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		2.8			2.8		µV p-p
	f = 1 kHz		94	100		94	100	nV/√Hz
POWER SUPPLY[6]								
AD8278 Supply Current	T_A = −40°C to +85°C			200			200	µA
AD8279 Supply Current	T_A = −40°C to +85°C			375			375	µA
Operating Voltage Range		2.0		36	2.0		36	V
TEMPERATURE RANGE								
Operating Range		−40		+125	−40		+125	°C

[1] Includes input bias and offset current errors, RTO (referred to output).
[2] The input voltage range may also be limited by absolute maximum input voltage or by the output swing. See the Input Voltage Range section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±20% absolute accuracy.
[4] Output voltage swing varies with supply voltage and temperature. See Figure 22 through Figure 25 for details.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature. See Figure 27 and Figure 28 for details.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	±18 V
Maximum Voltage at Any Input Pin	$-V_S + 40$ V
Minimum Voltage at Any Input Pin	$+V_S - 40$ V
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +85°C
Package Glass Transition Temperature (T_G)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The θ_{JA} values in Table 7 assume a 4-layer JEDEC standard board with zero airflow.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead MSOP	135	°C/W
8-Lead SOIC	121	°C/W
14-Lead SOIC	105	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8278 and AD8279 are limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period may result in a loss of functionality.

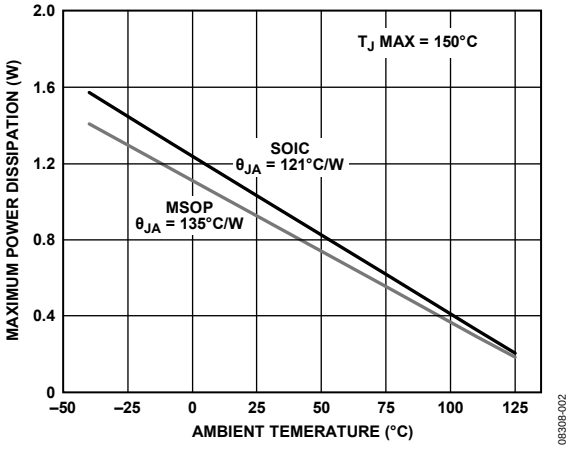


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

SHORT-CIRCUIT CURRENT

The AD8278 and AD8279 have built-in, short-circuit protection that limits the output current (see Figure 29 for more information). While the short-circuit condition itself does not damage the part, the heat generated by the condition can cause the part to exceed its maximum junction temperature, with corresponding negative effects on reliability. Figure 3 and Figure 29, combined with knowledge of the supply voltages and ambient temperature of the part, can be used to determine whether a short circuit will cause the part to exceed its maximum junction temperature.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

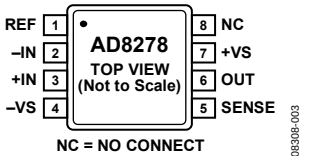


Figure 4. MSOP Pin Configuration

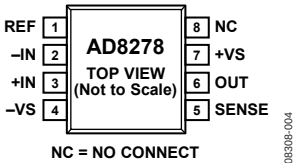


Figure 5. SOIC Pin Configuration

Table 8. AD8278 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF	Reference Voltage Input.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	−VS	Negative Supply.
5	SENSE	Sense Terminal.
6	OUT	Output.
7	+VS	Positive Supply.
8	NC	No Connect.

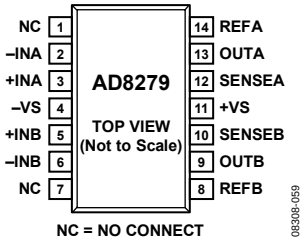


Figure 6. 14-Lead SOIC Pin Configuration

Table 9. AD8279 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	−INA	Channel A Inverting Input.
3	+INA	Channel A Noninverting Input.
4	−VS	Negative Supply.
5	+INB	Channel B Noninverting Input.
6	−INB	Channel B Inverting Input.
7	NC	No Connect.
8	REFB	Channel B Reference Voltage Input.
9	OUTB	Channel B Output.
10	SENSEB	Channel B Sense Terminal.
11	+VS	Positive Supply.
12	SENSEA	Channel A Sense Terminal.
13	OUTA	Channel A Output.
14	REFA	Channel A Reference Voltage Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to ground, G = ½ difference amplifier configuration, unless otherwise noted.

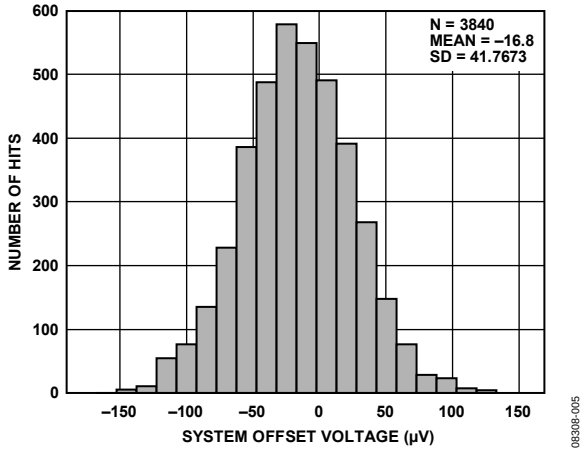


Figure 7. Distribution of Typical System Offset Voltage, G = 2

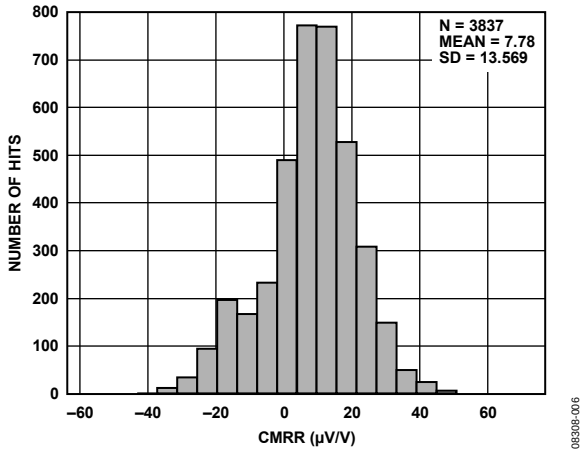


Figure 8. Distribution of Typical Common-Mode Rejection, G = 2

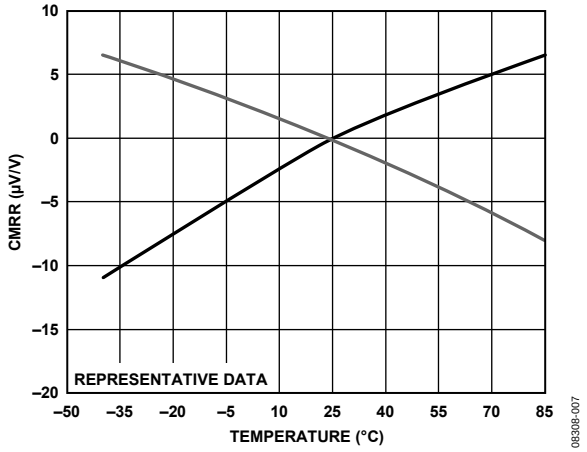


Figure 9. CMRR vs. Temperature, Normalized at 25°C, G = ½

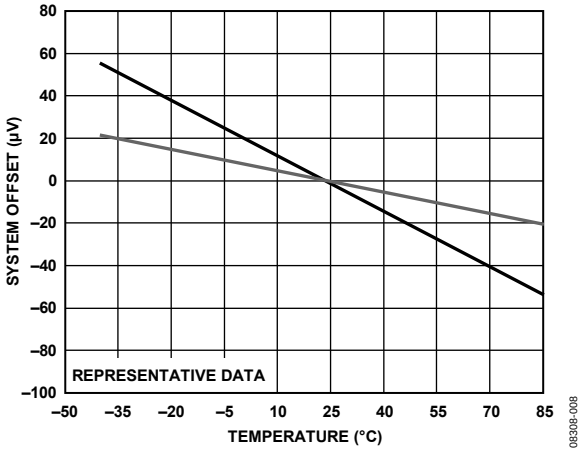


Figure 10. System Offset vs. Temperature, Normalized at 25°, G = ½

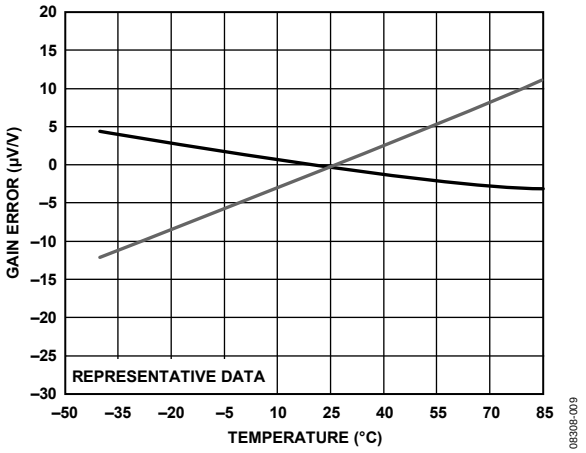


Figure 11. Gain Error vs. Temperature, Normalized at 25°C, G = ½

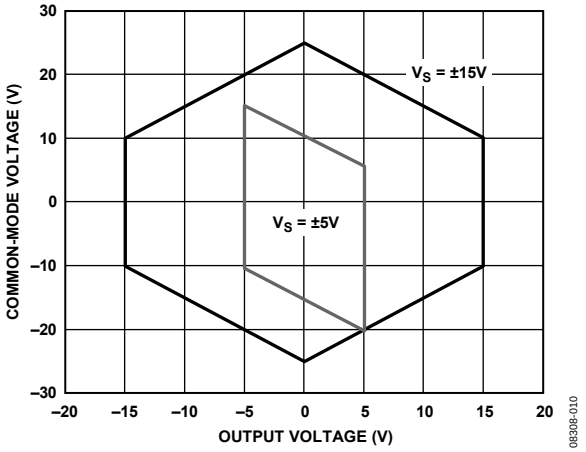


Figure 12. Input Common-Mode Voltage vs. Output Voltage, ±15 V and ±5 V Supplies, G = ½

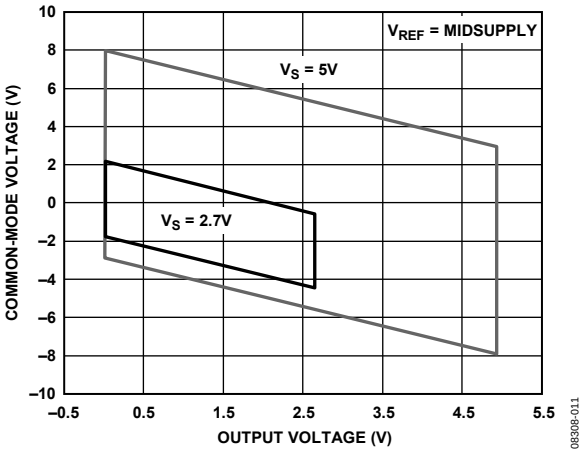


Figure 13. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = Midsupply, G = ½

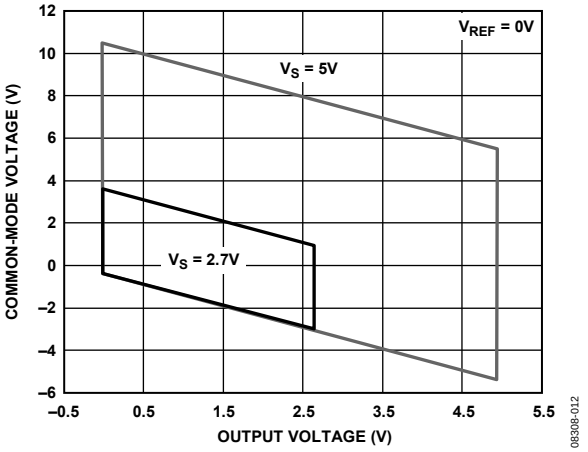


Figure 14. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = 0 V, G = ½

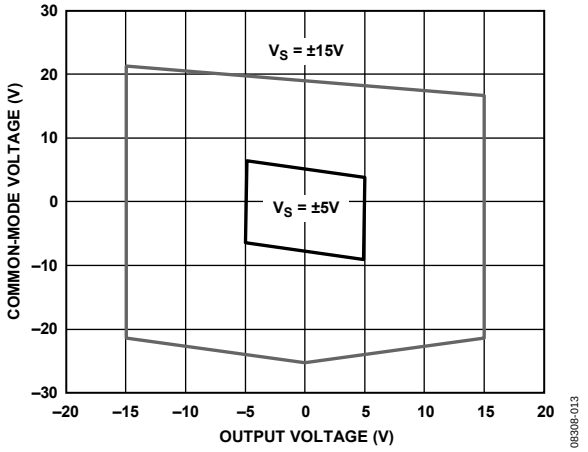


Figure 15. Input Common-Mode Voltage vs. Output Voltage, ±15 V and ±5 V Supplies, G = 2

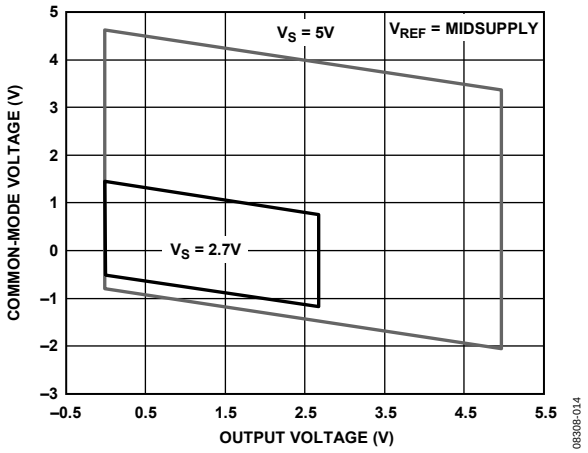


Figure 16. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = Midsupply, G = 2

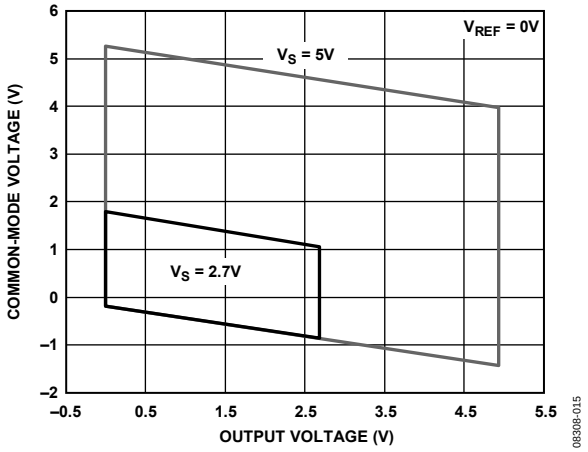


Figure 17. Input Common-Mode Voltage vs. Output Voltage, 5 V and 2.7 V Supplies, V_{REF} = 0 V, G = 2

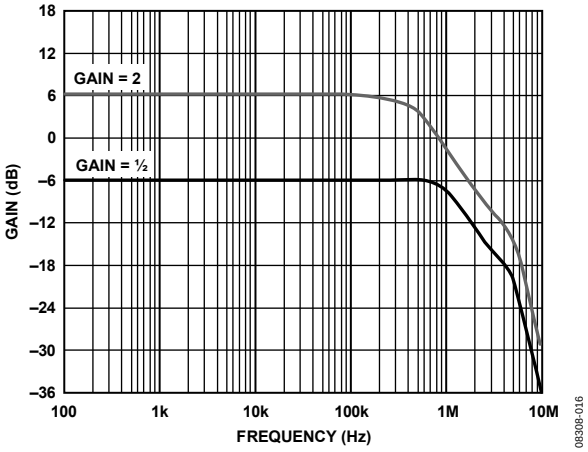


Figure 18. Gain vs. Frequency, ±15 V Supplies

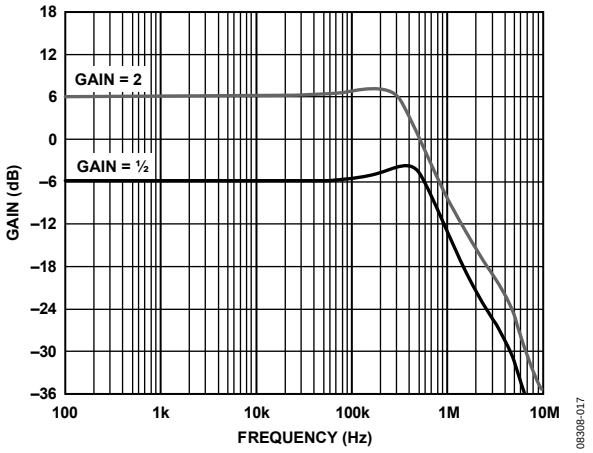


Figure 19. Gain vs. Frequency, +2.7 V Single Supply

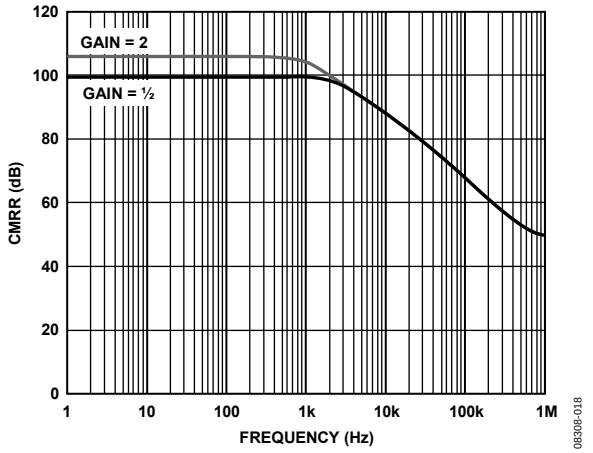


Figure 20. CMRR vs. Frequency

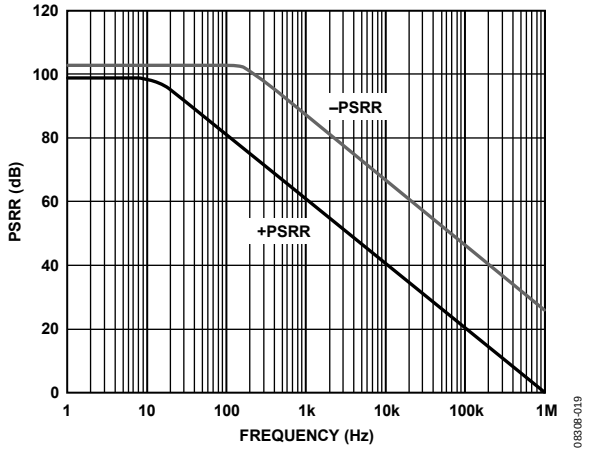


Figure 21. PSRR vs. Frequency

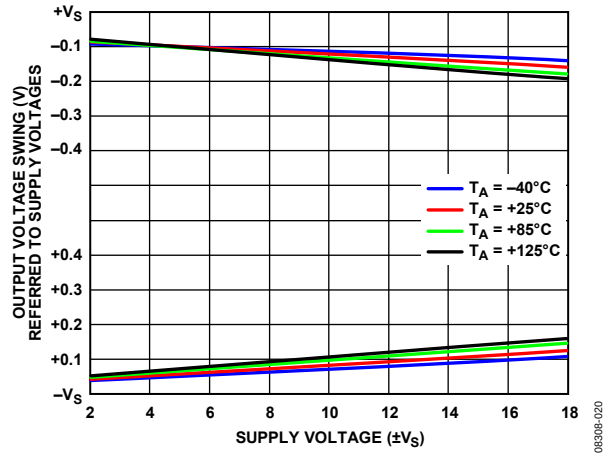


Figure 22. Output Voltage Swing vs. Supply Voltage and Temperature, R_L = 10 kΩ

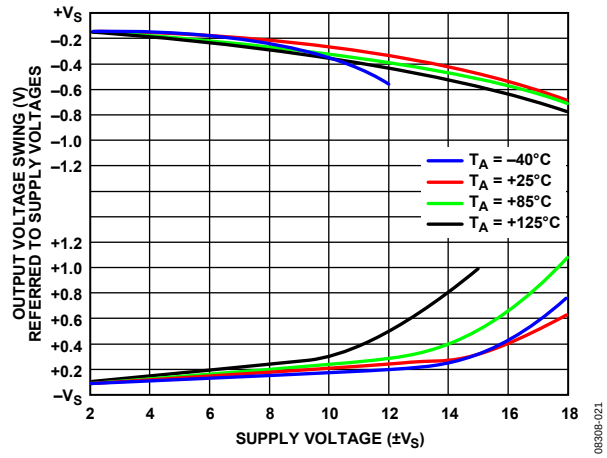


Figure 23. Output Voltage Swing vs. Supply Voltage and Temperature, R_L = 2 kΩ

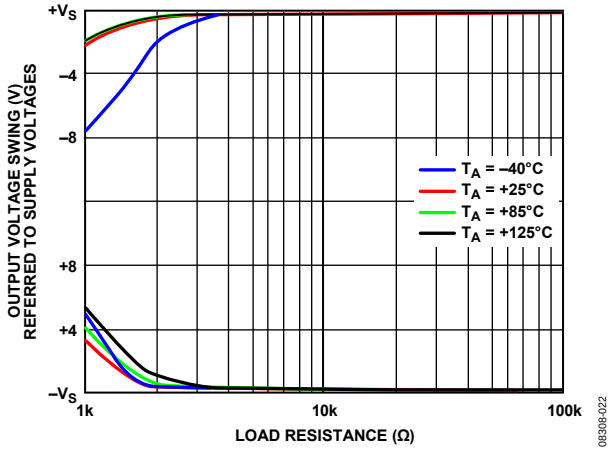


Figure 24. Output Voltage Swing vs. R_L and Temperature, V_S = ±15 V

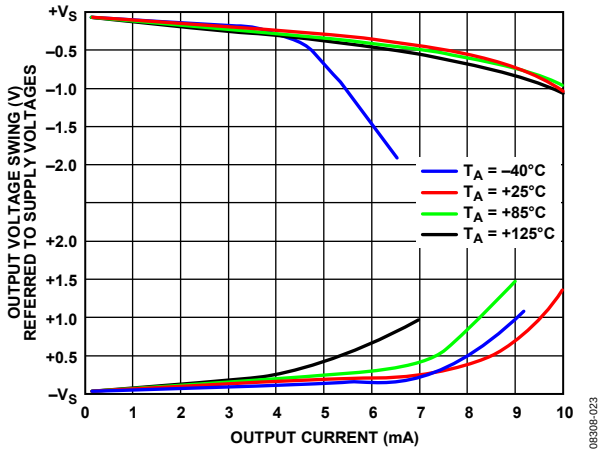


Figure 25. Output Voltage Swing vs. I_{OUT} and Temperature, V_S = ±15 V

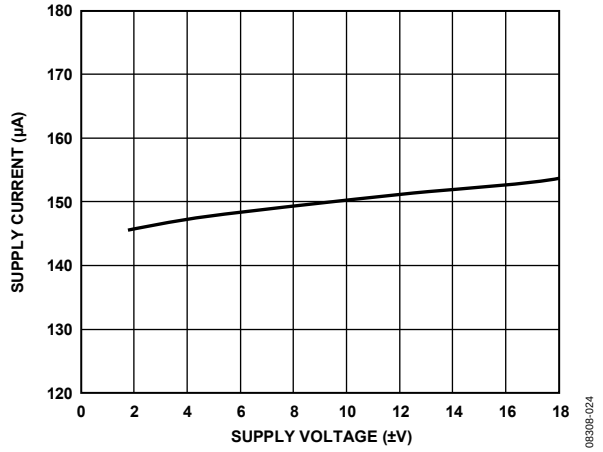


Figure 26. Supply Current per Channel vs. Dual-Supply Voltage, V_{IN} = 0 V

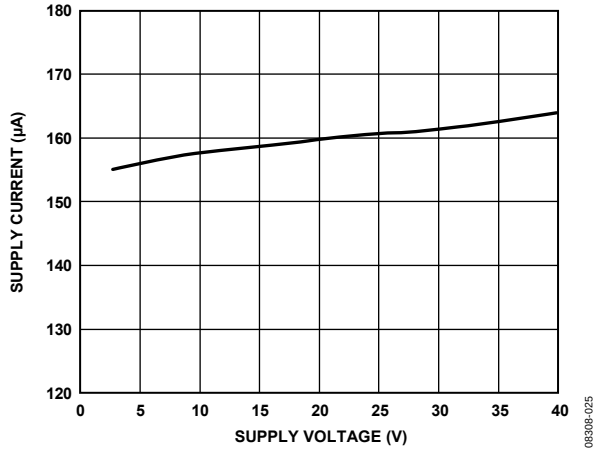


Figure 27. Supply Current per Channel vs. Single-Supply Voltage, V_{IN} = 0 V, V_{REF} = 0 V

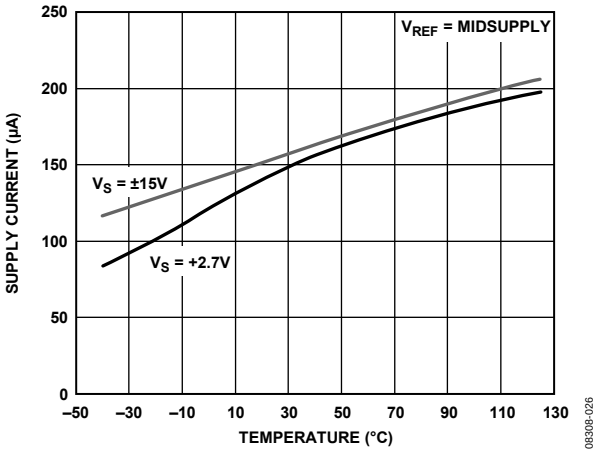


Figure 28. Supply Current per Channel vs. Temperature

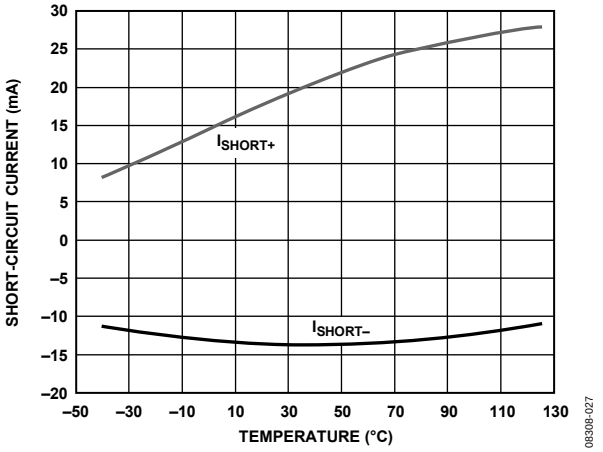


Figure 29. Short-Circuit Current per Channel vs. Temperature

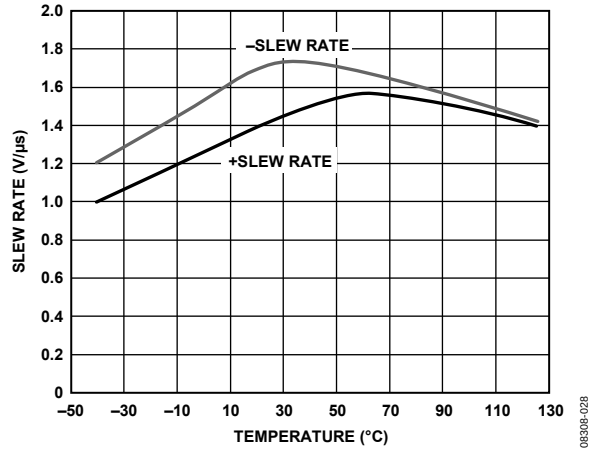


Figure 30. Slew Rate vs. Temperature, V_{IN} = 20 V p-p, 1 kHz

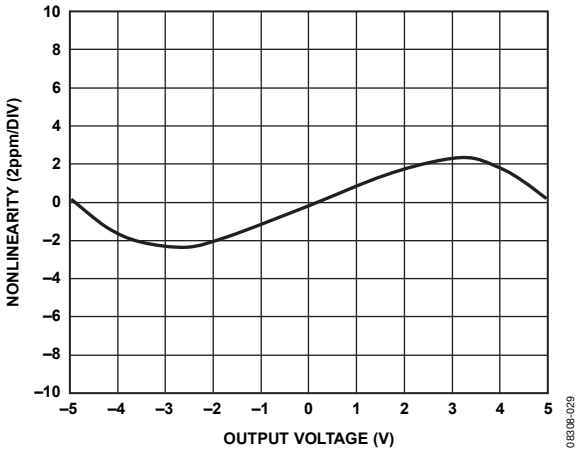


Figure 31. Gain Nonlinearity, $V_S = \pm 15$ V, $R_L \geq 2$ kΩ, $G = ½$

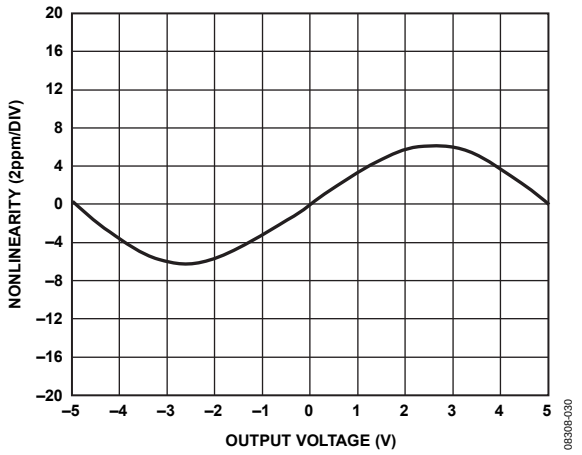


Figure 32. Gain Nonlinearity, $V_S = \pm 15$ V, $R_L \geq 2$ kΩ, $G = 2$

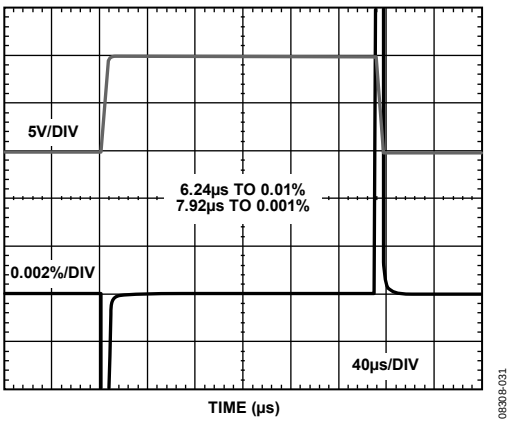


Figure 33. Large Signal Pulse Response and Settling Time, 10 V Step, $V_S = \pm 15$ V, $G = ½$

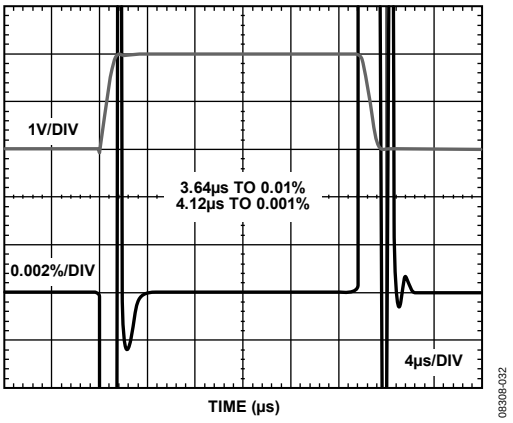


Figure 34. Large Signal Pulse Response and Settling Time, 2 V Step, $V_S = 2.7$ V, $G = ½$

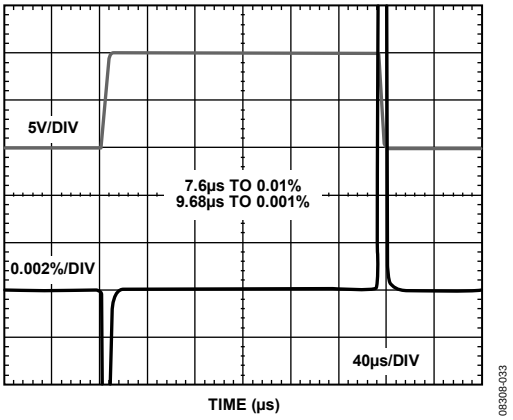


Figure 35. Large Signal Pulse Response and Settling Time, 10 V Step, $V_S = \pm 15$ V, $G = 2$

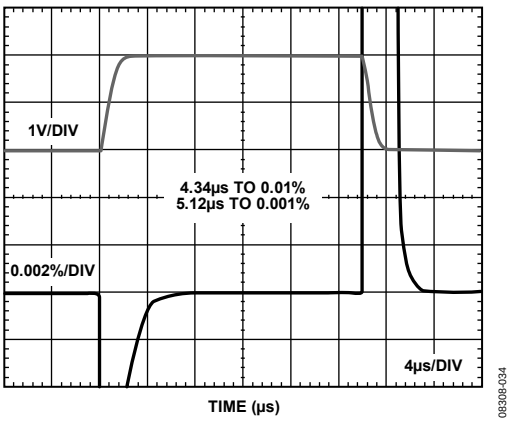


Figure 36. Large Signal Pulse Response and Settling Time, 2 V Step, $V_S = 2.7$ V

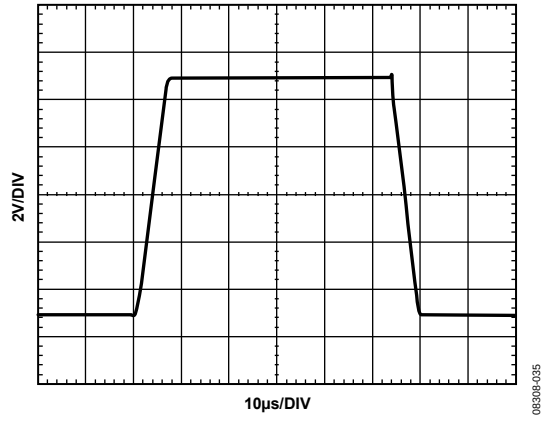


Figure 37. Large Signal Step Response, G = ½

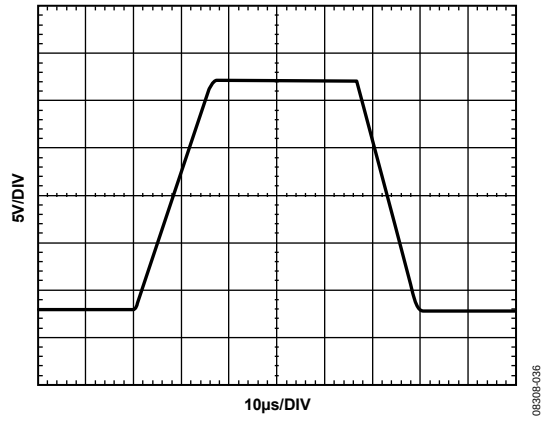


Figure 38. Large Signal Step Response, G = 2

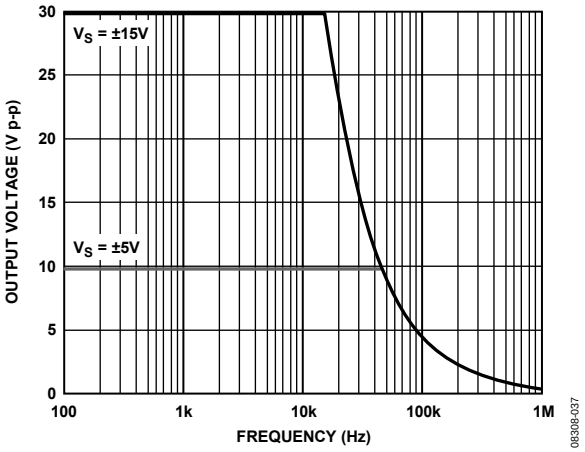


Figure 39. Maximum Output Voltage vs. Frequency, V_S = ±15 V, ±5 V

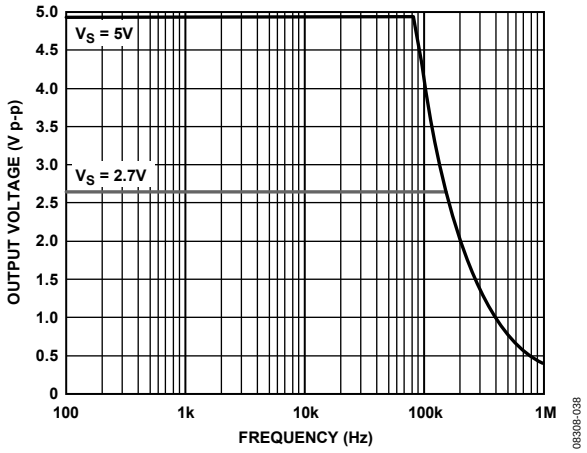


Figure 40. Maximum Output Voltage vs. Frequency, V_S = 5 V, 2.7 V

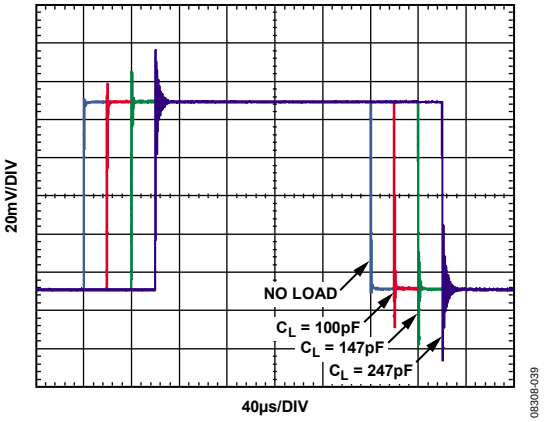


Figure 41. Small Signal Step Response for Various Capacitive Loads, G = ½

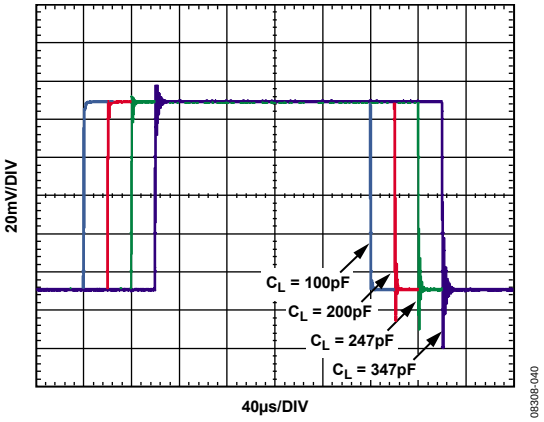


Figure 42. Small Signal Step Response for Various Capacitive Loads, G = 2

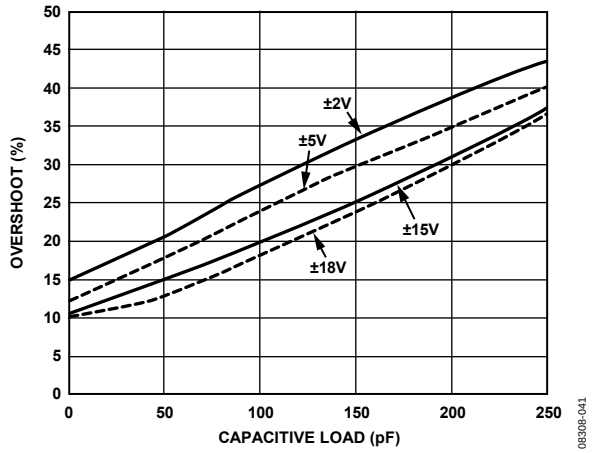


Figure 43. Small Signal Overshoot vs. Capacitive Load, $R_L \geq 2$ kΩ, G = ½

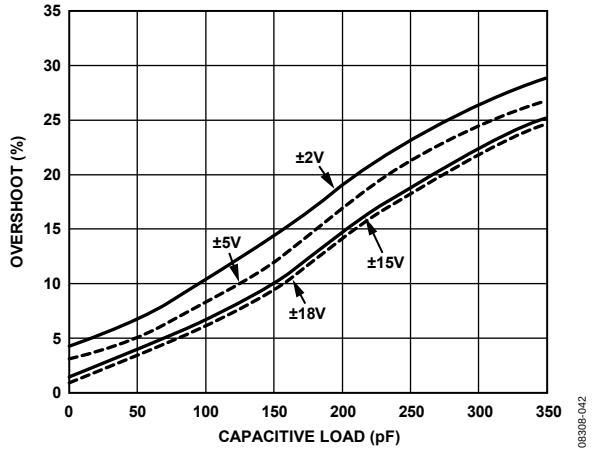


Figure 44. Small Signal Overshoot vs. Capacitive Load, $R_L \geq 2$ kΩ, G = 2

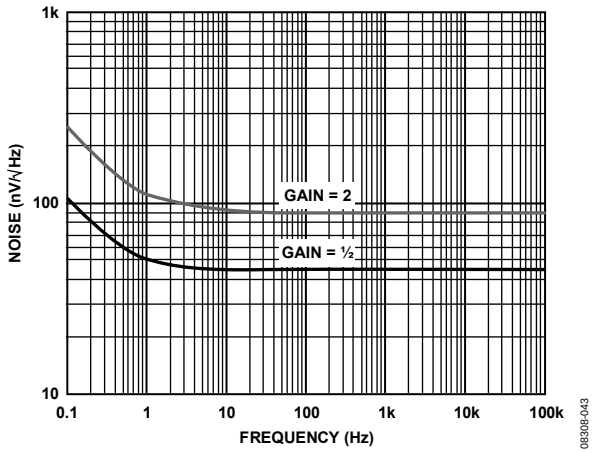


Figure 45. Voltage Noise Density vs. Frequency

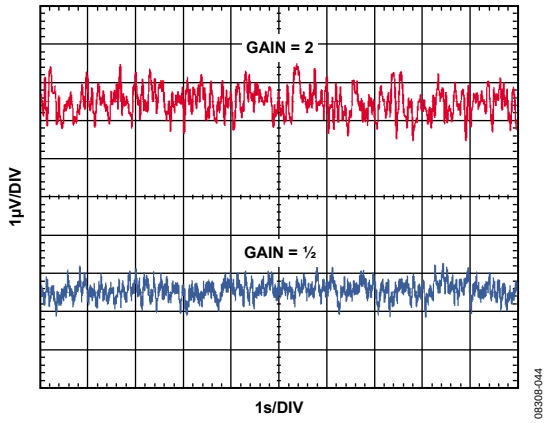


Figure 46. 0.1 Hz to 10 Hz Voltage Noise

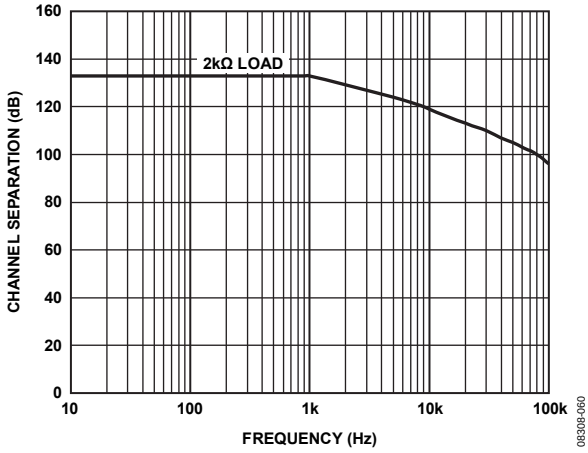


Figure 47. Channel Separation

THEORY OF OPERATION

CIRCUIT INFORMATION

Each channel of the AD8278 and AD8279 consists of a low power, low noise op amp and four laser-trimmed on-chip resistors. These resistors can be externally connected to make a variety of amplifier configurations, including difference, noninverting, and inverting configurations. Taking advantage of the integrated resistors of the AD8278 and AD8279 provides the designer with several benefits over a discrete design, including smaller size, lower cost, and better ac and dc performance.

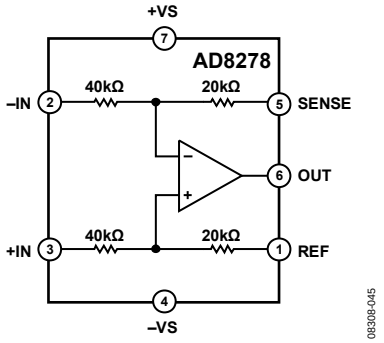


Figure 48. Functional Block Diagram

DC Performance

Much of the dc performance of op amp circuits depends on the accuracy of the surrounding resistors. Using superposition to analyze a typical difference amplifier circuit, as is shown in Figure 49, the output voltage is found to be

$$V_{OUT} = V_{IN+}\left(\frac{R2}{R1+R2}\right)\left(1+\frac{R4}{R3}\right) - V_{IN-}\left(\frac{R4}{R3}\right)$$

This equation demonstrates that the gain accuracy and common-mode rejection ratio of the AD8278 and AD8279 is determined primarily by the matching of resistor ratios. Even a 0.1% mismatch in one resistor degrades the CMRR to 69 dB for a G = 2 difference amplifier.

The difference amplifier output voltage equation can be reduced to

$$V_{OUT} = \frac{R4}{R3}\left(V_{IN+} - V_{IN-}\right)$$

as long as the following ratio of the resistors is tightly matched:

$$\frac{R2}{R1} = \frac{R4}{R3}$$

The resistors on the AD8278 and AD8279 are laser trimmed to match accurately. As a result, the AD8278 and AD8279 provide superior performance over a discrete solution, enabling better CMRR, gain accuracy, and gain drift, even over a wide temperature range.

AC Performance

Component sizes and trace lengths are much smaller in an IC than on a PCB; therefore, the corresponding parasitic elements are also smaller. This results in better ac performance of the AD8278 and AD8279. For example, the positive and negative input terminals of the AD8278 and AD8279 op amps are intentionally not pinned out. By not connecting these nodes to the traces on the PCB, their capacitance remains low and balanced, resulting in improved loop stability and excellent common-mode rejection over frequency.

DRIVING THE AD8278 AND AD8279

Care should be taken to drive the AD8278 and AD8279 with a low impedance source, for example, another amplifier. Source resistance of even a few kilohms (kΩ) can unbalance the resistor ratios and, therefore, significantly degrade the gain accuracy and common-mode rejection of the AD8278 and AD8279. Because all configurations present several kilohms (kΩ) of input resistance, the AD8278 and AD8279 do not require a high current drive from the source and are easy to drive.

INPUT VOLTAGE RANGE

The AD8278 and AD8279 are able to measure input voltages beyond the supply rails. The internal resistors divide down the voltage before it reaches the internal op amp and provide protection to the op amp inputs. Figure 49 shows an example of how the voltage division works in a difference amplifier configuration. For the AD8278 and AD8279 to measure correctly, the input voltages at the input nodes of the internal op amp must stay below 1.5 V of the positive supply rail and can exceed the negative supply rail by 0.1 V. Refer to the Power Supplies section for more details.

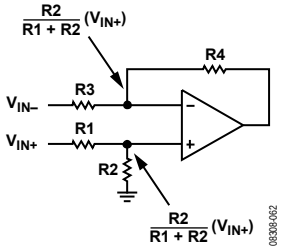


Figure 49. Voltage Division in the Difference Amplifier Configuration

The AD8278 and AD8279 have integrated ESD diodes at the inputs that provide overvoltage protection. This feature simplifies system design by eliminating the need for additional external protection circuitry and enables a more robust system.

The voltages at any of the inputs of the parts can safely range from $+V_S - 40$ V up to $-V_S + 40$ V. For example, on ±10 V supplies, input voltages can go as high as ±30 V. Care should be taken to not exceed the $+V_S - 40$ V to $-V_S + 40$ V input limits to avoid damaging the parts.

POWER SUPPLIES

The AD8278 and AD8279 operate extremely well over a very wide range of supply voltages. They can operate on a single supply as low as 2 V and as high as 36 V, under appropriate setup conditions.

For best performance, the user should ensure that the internal op amp is biased correctly. The internal input terminals of the op amp must have sufficient voltage headroom to operate properly. Proper operation of the part requires at least 1.5 V between the positive supply rail and the op amp input terminals. This relationship is expressed in the following equation:

$$\frac{R1}{R1+R2}V_{REF} < +V_S - 1.5\,\text{V}$$

For example, when operating on a $+V_S$= 2 V single supply and V_{REF} = 0 V, it can be seen from Figure 50 that the op amp input terminals are biased at 0 V, allowing more than the required 1.5 V headroom. However, if V_{REF} = 1 V under the same conditions, the input terminals of the op amp are biased at 0.66 V (G = ½). Now the op amp does not have the required 1.5 V headroom and cannot function. Therefore, the user must increase the supply voltage or decrease V_{REF} to restore proper operation.

The AD8278 and AD8279 are typically specified at single and dual supplies, but they can be used with unbalanced supplies as well; for example, $-V_S$ = −5 V, $+V_S$ = +20 V. The difference between the two supplies must be kept below 36 V. The positive supply rail must be at least 2 V above the negative supply.

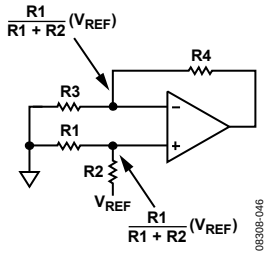


Figure 50. Ensure Sufficient Voltage Headroom on the Internal Op Amp Inputs

Use a stable dc voltage to power the AD8278 and AD8279. Noise on the supply pins can adversely affect performance. Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close as possible to each supply pin. Use a tantalum capacitor of 10 µF between each supply and ground. It can be farther away from the supply pins and, typically, it can be shared by other precision integrated circuits.

APPLICATIONS INFORMATION

CONFIGURATIONS

The AD8278 and AD8279 can be configured in several ways (see Figure 51 to Figure 57). These configurations have excellent gain accuracy and gain drift because they rely on the internal matched resistors. Note that Figure 53 shows the AD8278 and AD8279 as difference amplifiers with a midsupply reference voltage at the noninverting input. This allows the AD8278 and AD8279 to be used as a level shifter, which is appropriate in single-supply applications that are referenced to midsupply. Table 10 lists several single-ended amplifier configurations that are not illustrated.

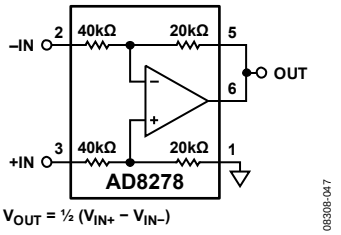


Figure 51. Difference Amplifier, Gain = ½

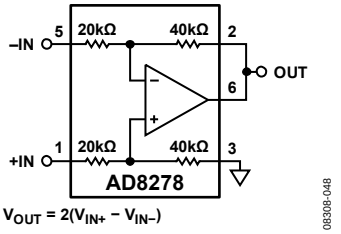


Figure 52. Difference Amplifier, Gain = 2

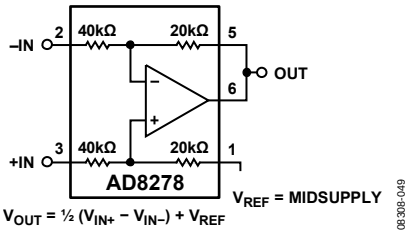


Figure 53. Difference Amplifier, Gain = ½, Referenced to Midsupply

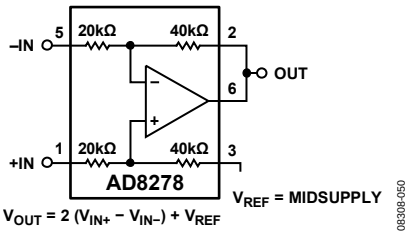


Figure 54. Difference Amplifier, Gain = 2, Referenced to Midsupply

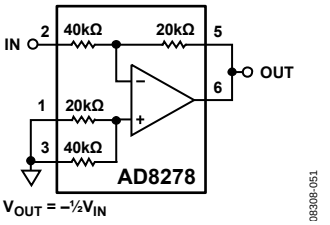


Figure 55. Inverting Amplifier, Gain = –½

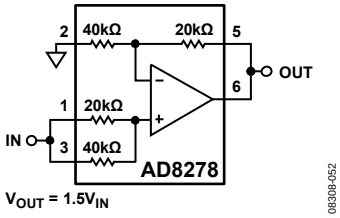


Figure 56. Noninverting Amplifier, Gain = 1.5

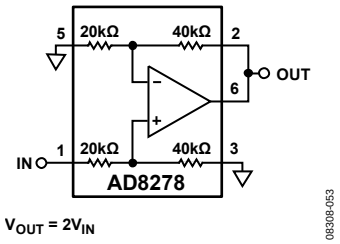


Figure 57. Noninverting Amplifier, Gain = 2

Table 10. AD8278 Difference and Single-Ended Amplifier Configurations

Amplifier Configuration	Signal Gain	Pin 1 (REF)	Pin 2 (VIN–)	Pin 3 (VIN+)	Pin 5 (SENSE)
Difference Amplifier	+½	GND	IN–	IN+	OUT
Difference Amplifier	+2	IN+	OUT	GND	IN–
Single-Ended Inverting Amplifier	–½	GND	IN	GND	OUT
Single-Ended Inverting Amplifier	–2	GND	OUT	GND	IN
Single-Ended Noninverting Amplifier	+3/2	IN	GND	IN	OUT
Single-Ended Noninverting Amplifier	+3	IN	OUT	IN	GND
Single-Ended Noninverting Amplifier	+½	GND	GND	IN	OUT
Single-Ended Noninverting Amplifier	+1	IN	GND	GND	OUT
Single-Ended Noninverting Amplifier	+1	GND	OUT	IN	GND
Single-Ended Noninverting Amplifier	+2	IN	OUT	GND	GND

The reference must be driven with a low impedance source to maintain the internal resistor ratio. An example using the low power, low noise OP1177 as a reference is shown in Figure 58.

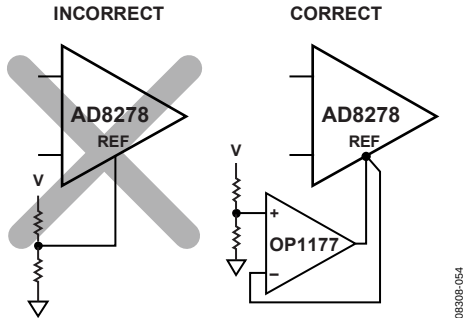


Figure 58. Driving the Reference Pin

DIFFERENTIAL OUTPUT

The two difference amplifiers of the AD8279 can be configured to provide a differential output, as shown in Figure 59. This differential output configuration is suitable for various applications, such as strain gage excitation and single-ended-to-differential conversion. The differential output voltage has a gain twice that of a single AD8279 channel, as shown in the following equation:

$$V_{DIFF_OUT} = V_{+OUT} - V_{-OUT} = 2 \times G_{AD8279} \times (V_{IN+} - V_{IN-})$$

If the AD8279 amplifiers are each configured for G = ½, the differential gain is 1×; if the AD8279 amplifiers are each configured for G = 2, the differential gain is 4×.

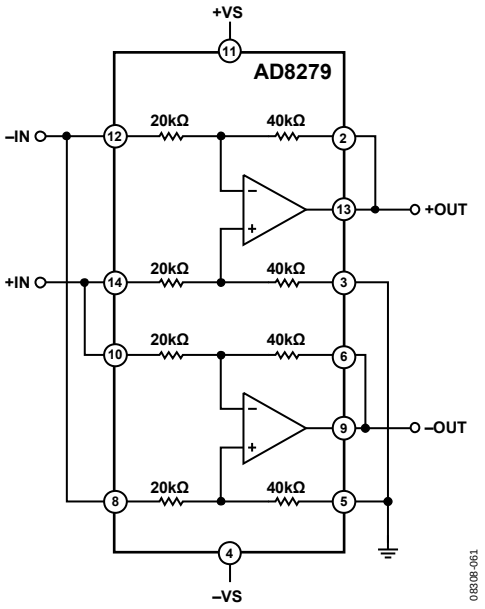


Figure 59. AD8279 Differential Output G = 4 Configuration

INSTRUMENTATION AMPLIFIER

The AD8278 and AD8279 can be used as building blocks for a low power, low cost instrumentation amplifier. An instrumentation amplifier provides high impedance inputs and delivers high common-mode rejection. Combining the AD8278 with an Analog Devices, Inc., low power amplifier (see Table 11) creates a precise, power efficient voltage measurement solution suitable for power critical systems.

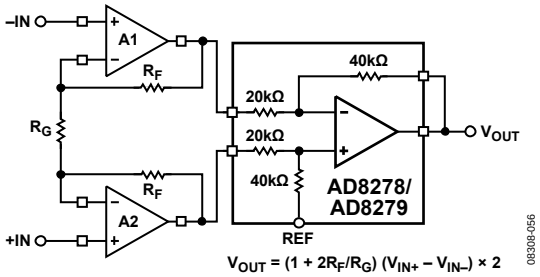


Figure 60. Low Power Precision Instrumentation Amplifier

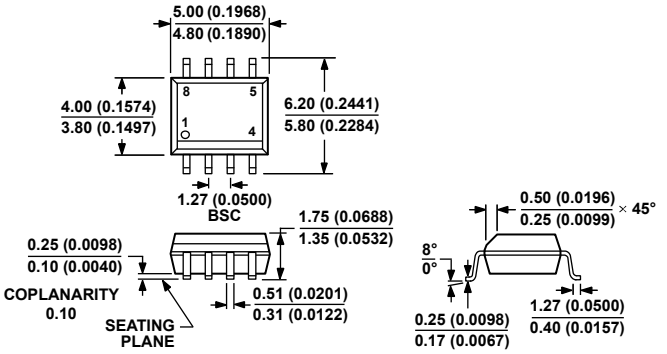
Table 11. Low Power Op Amps

Op Amp (A1, A2)	Features
AD8506	Dual micropower op amp
AD8607	Precision dual micropower op amp
AD8617	Low cost CMOS micropower op amp
AD8667	Dual precision CMOS micropower op amp

It is preferable to use dual op amps for the high impedance inputs because they have better matched performance and track each other over temperature. The AD8278 and AD8279 difference amplifiers cancel out common-mode errors from the input op amps, if they track each other. The differential gain accuracy of the in-amp is proportional to how well the input feedback resistors (R_F) match each other. The CMRR of the in-amp increases as the differential gain is increased ($1 + 2R_F/R_G$), but a higher gain also reduces the common-mode voltage range.

Refer to *A Designer's Guide to Instrumentation Amplifiers* for more design ideas and considerations at www.analog.com, under Technical Documentation.

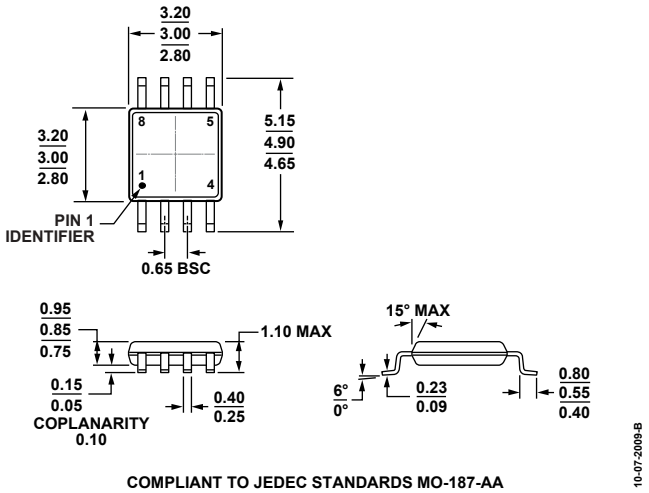
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 61. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 62. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

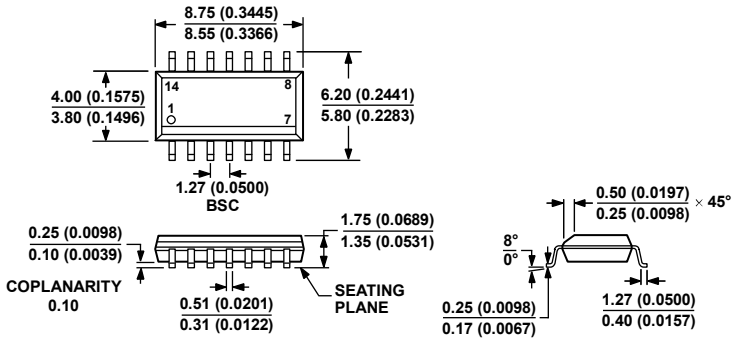


Figure 63. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8278ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8278ARZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8278ARZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8278BRZ	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8278BRZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8278BRZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8278ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	Y21
AD8278ARMZ-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y21
AD8278ARMZ-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y21
AD8278BRMZ	−40°C to +85°C	8-Lead MSOP	RM-8	Y22
AD8278BRMZ-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y22
AD8278BRMZ-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y22
AD8279ARZ	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8279ARZ-R7	−40°C to +85°C	14-Lead SOIC_N, 7" Tape and Reel	R-14	
AD8279ARZ-RL	−40°C to +85°C	14-Lead SOIC_N, 13" Tape and Reel	R-14	
AD8279BRZ	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8279BRZ-R7	−40°C to +85°C	14-Lead SOIC_N, 7" Tape and Reel	R-14	
AD8279BRZ-RL	−40°C to +85°C	14-Lead SOIC_N, 13" Tape and Reel	R-14	

[1] Z = RoHS Compliant Part.

NOTES

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ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
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