DS87C520/DS83C520
EPROM/ROM High-Speed Microcontrollers

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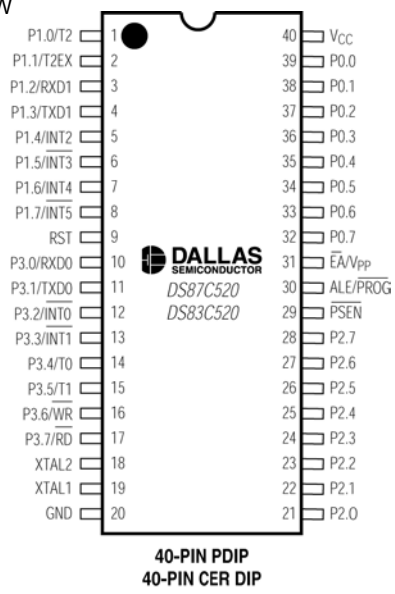
FEATURES

- **80C52 Compatible**
  8051 Pin- and Instruction-Set Compatible
  Four 8-Bit I/O Ports
  Three 16-Bit Timer/Counters
  256 Bytes Scratchpad RAM
- **Large On-Chip Memory**
  16kB Program Memory
  1kB Extra On-Chip SRAM for MOVX
- **ROMSIZE Feature**
  Selects Internal ROM Size from 0 to 16kB
  Allows Access to Entire External Memory Map
  Dynamically Adjustable by Software
  Useful as Boot Block for External Flash
- **High-Speed Architecture**
  4 Clocks/Machine Cycle (8051 = 12)
  Runs DC to 33MHz Clock Rates
  Single-Cycle Instruction in 121ns
  Dual Data Pointer
  Optional Variable Length MOVX to Access Fast/Slow RAM/Peripherals
- **Power Management Mode**
  Programmable Clock Source to Save Power
  CPU Runs from (crystal/64) or (crystal/1024)
  Provides Automatic Hardware and Software Exit
- **EMI Reduction Mode Disables ALE**
- **Two Full-Duplex Hardware Serial Ports**
- **High Integration Controller Includes**:
  Power-Fail Reset
  Early-Warning Power-Fail Interrupt
  Programmable Watchdog Timer
- **13 Interrupt Sources with Six External**
- **Available in 40-pin PDIP, 44-Pin PLCC, 44-Pin TQFP, and 40-Pin Windowed CERDIP**
- **Factory Mask DS83C520 or EPROM (OTP) DS87C520**

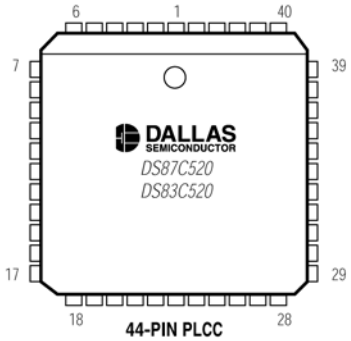
*The **High-Speed Microcontroller User's Guide** must be used in conjunction with this data sheet. Download it at: www.maxim-ic.com/microcontrollers.*

PIN CONFIGURATIONS

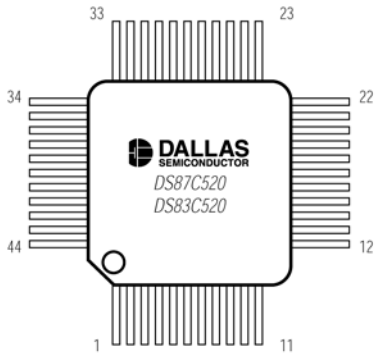
TOP VIEW



40-PIN PDIP
40-PIN CER DIP



44-PIN PLCC



44-PIN TQFP

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

REV: 091605

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS87C520-MCL	0˚C to +70˚C	33	40 Plastic DIP
DS87C520-MCL+	0˚C to +70˚C	33	40 Plastic DIP
DS87C520-QCL	0˚C to +70˚C	33	44 PLCC
DS87C520-QCL+	0˚C to +70˚C	33	44 PLCC
DS87C520-ECL	0˚C to +70˚C	33	44 TQFP
DS87C520-ECL+	0˚C to +70˚C	33	44 TQFP
DS87C520-MNL	-40˚C to +85˚C	33	40 Plastic DIP
DS87C520-MNL+	-40˚C to +85˚C	33	40 Plastic DIP
DS87C520-QNL	-40˚C to +85˚C	33	44 PLCC
DS87C520-QNL+	-40˚C to +85˚C	33	44 PLCC
DS87C520-ENL	-40˚C to +85˚C	33	44 TQFP
DS87C520-ENL+	-40˚C to +85˚C	33	44 TQFP
DS87C520-WCL*	0˚C to +70˚C	33	40 Windowed CERDIP
DS83C520-MCL	0˚C to +70˚C	33	40 Plastic DIP
DS83C520-MCL+	0˚C to +70˚C	33	40 Plastic DIP
DS83C520-QCL	0˚C to +70˚C	33	44 PLCC
DS83C520-QCL+	0˚C to +70˚C	33	44 PLCC
DS83C520-ECL	0˚C to +70˚C	33	44 TQFP
DS83C520-ECL+	0˚C to +70˚C	33	44 TQFP
DS83C520-MNL	-40˚C to +85˚C	33	40 Plastic DIP
DS83C520-MNL+	-40˚C to +85˚C	33	40 Plastic DIP
DS83C520-QNL	-40˚C to +85˚C	33	44 PLCC
DS83C520-QNL+	-40˚C to +85˚C	33	44 TQFP
DS83C520-ENL	-40˚C to +85˚C	33	44 TQFP
DS83C520-ENL+	-40˚C to +85˚C	33	44 TQFP

+ Denotes a Pb-free/RoHS-compliant device.

** The windowed ceramic DIP package is intrinsically Pb free.*

DESCRIPTION

The DS87C520/DS83C520 EPROM/ROM high-speed microcontrollers are fast 8051-compatible microcontrollers. They feature a redesigned processor core without wasted clock and memory cycles. As a result, the devices execute every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520/DS83C520 offer a maximum crystal speed of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS87C520/DS83C520 are pin compatible with all three packages of the standard 8051, and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. They feature 16kB of EPROM or mask ROM with an extra 1kB of data RAM. Both OTP and windowed packages are available.

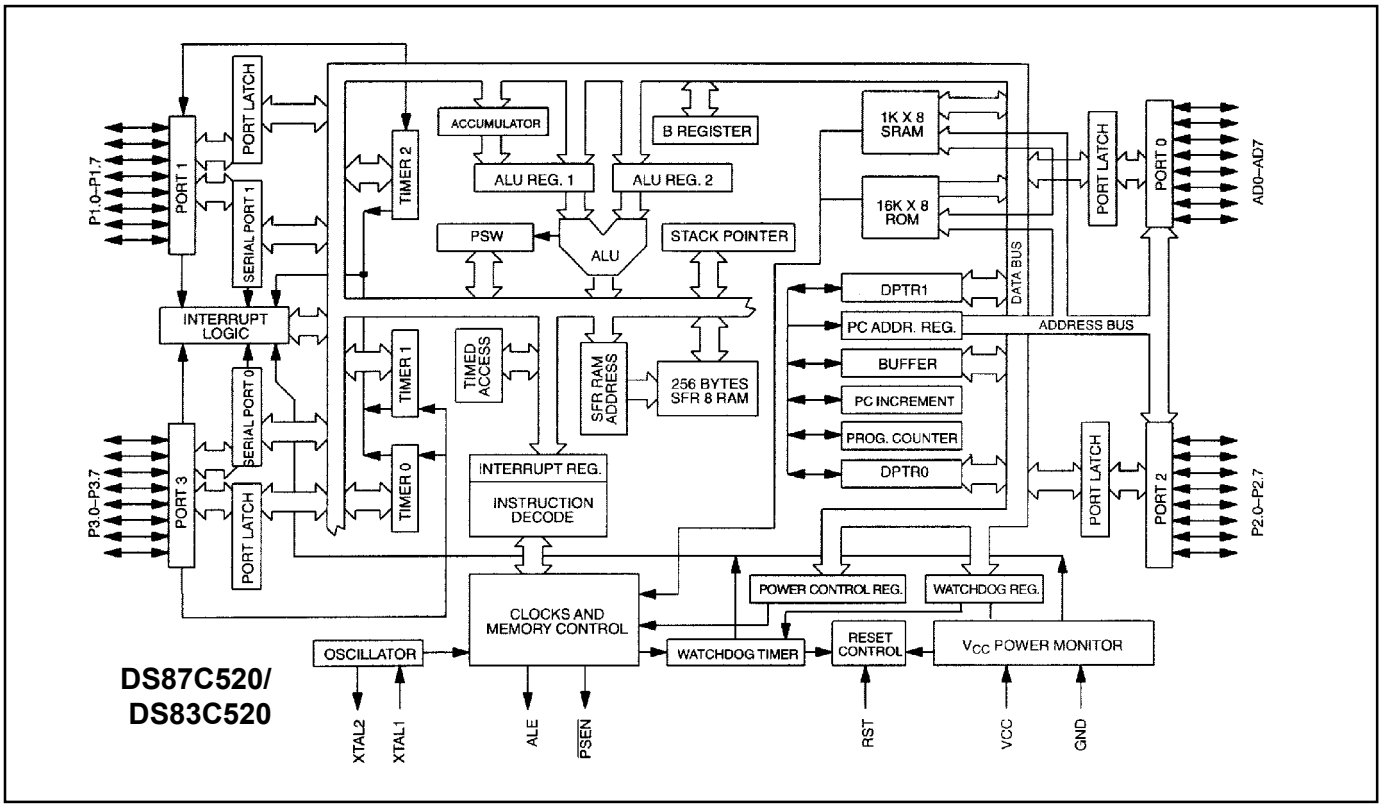
Besides greater speed, the microcontroller includes a second full hardware serial port, seven additional interrupts, programmable Watchdog Timer, Brownout Monitor, and Power-Fail Reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access from two to nine machine cycles for flexibility in selecting external memory and peripherals.

A new Power Management Mode (PMM) is useful for portable applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. For example, at 12MHz, standard operation has a machine cycle rate of 3MHz. In Power Management Mode, software can select either 187.5kHz or 11.7kHz machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C520 is a factory mask ROM version of the DS87C520 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C520, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C520 will apply to the DS83C520, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**Positive Supply Voltage.** +5V
20	1, 22, 23	16, 17, 39	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is not required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output.** This active-low signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external ROM is not being accessed.

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
30	33	27	ALE	**Address Latch Enable Output**. The ALE functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C520/DS83C520 are in a reset condition. ALE can also be disabled and forced high by writing ALEOFF = 1 (PMR.2). ALE operates independently of ALEOFF during external memory accesses.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–7), I/O**. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pullup resistors are required when using Port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	
1	2	40	P1.0	**Port 1, I/O**. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state; a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are out-lines as follows. **Port** **Alternate** **Function** P1.0 T2 External I/O for Timer/Counter 2 P1.1 T2EX EX Timer/Counter 2 Capture/Reload Trigger P1.2 RXD1 Serial Port 1 Input P1.3 TXD1 Serial Port 1 Output P1.4 INT2 External Interrupt 2 (Positive Edge Detect) P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect) P1.6 INT4 External Interrupt 4 (Positive Edge Detect) P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)
2	3	41	P1.1	
3	4	42	P1.2	
4	5	43	P1.3	
5	6	44	P1.4	
6	7	1	P1.5	
7	8	2	P1.6	
8	9	3	P1.7	

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
21	24	18	P2.0 (A8)	**Port 2 (A8–15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
22	25	19	P2.1 (A9)	
23	26	20	P2.2 (A10)	
24	27	21	P2.3 (A11)	
25	28	22	P2.4 (A12)	
26	29	23	P2.5 (A13)	
27	30	24	P2.6 (A14)	
28	31	25	P2.7 (A15)	
10	11	5	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port — Alternate — Mode** P3.0 — RXD0 — Serial Port 0 Input P3.1 — TXD0 — Serial Port 0 Output P3.2 — $\overline{INT0}$ — External Interrupt 0 P3.3 — $\overline{INT1}$ — External Interrupt 1 P3.4 — T0 — Timer 0 External Input P3.5 — T1 — Timer 1 External Input P3.6 — $\overline{WR}$ — External Data Memory Write Strobe P3.7 — $\overline{RD}$ — External Data Memory Read Strobe
11	13	7	P3.1	
12	14	8	P3.2	
13	15	9	P3.3	
14	16	10	P3.4	
15	17	11	P3.5	
16	18	12	P3.6	
17	19	13	P3.7	
31	35	29	$\overline{EA}$	**External Access Input, Active Low.** Connect to ground to force the DS87C520/DS83C520 to use an external ROM. The internal RAM is still accessible as determined by register settings. Connect $\overline{EA}$ to V_{CC} to use internal ROM.
—	12, 34	6, 28	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in this family.

COMPATIBILITY

The DS87C520/DS83C520 are fully static CMOS 8051-compatible microcontrollers designed for high performance. In most cases, the DS87C520/DS83C520 can drop into an existing socket for the 8xc51 family to improve the operation significantly. While remaining familiar to 8051 family users, the devices have many new features. In general, software written for existing 8051-based systems works without modification on the DS87C520/DS83C520. The exception is critical timing since the high-speed microcontrollers performs instructions much faster than the original for any given crystal selection. The DS87C520/DS83C520 run the standard 8051 family instruction set and are pin compatible with DIP, PLCC, or TQFP packages.

The DS87C520/DS83C520 provide three 16-bit timer/counters, full-duplex serial port (2), 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12-clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new four clocks per cycle if desired. The PCA is not supported.

The DS87C520/DS83C520 provide several new hardware features implemented by new special function registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C520/DS83C520 feature a high-speed 8051-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C520/DS83C520, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C520/DS83C520 will see the full 3-to-1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements produce a peak instruction cycle in 121ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the *High-Speed Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520/DS83C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520/DS83C520 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520/DS83C520. This allows the DS87C520/DS83C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C520/DS83C520 duplicate the SFRs contained in the standard 80C52. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

MEMORY RESOURCES

Like the 8051, the DS87C520/DS83C520 use three memory areas. The total memory configuration of the DS87C520/DS83C520 is 16kB of ROM, 1kB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1kB of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1kB as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window of the windowed CERDIP should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the data sheet.

PROGRAM MEMORY ACCESS

On-chip ROM begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip ROM will cause the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS87C520/DS83C520 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as Flash, is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory, and then restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 2.

The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RMS2, RMS1, RMS0 have the following effect.

RMS2	RMS1	RMS0	MAXIMUM ON-CHIP ROM ADDRESS
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB (default)/3FFFh
1	1	0	Invalid—reserved
1	1	1	Invalid—reserved

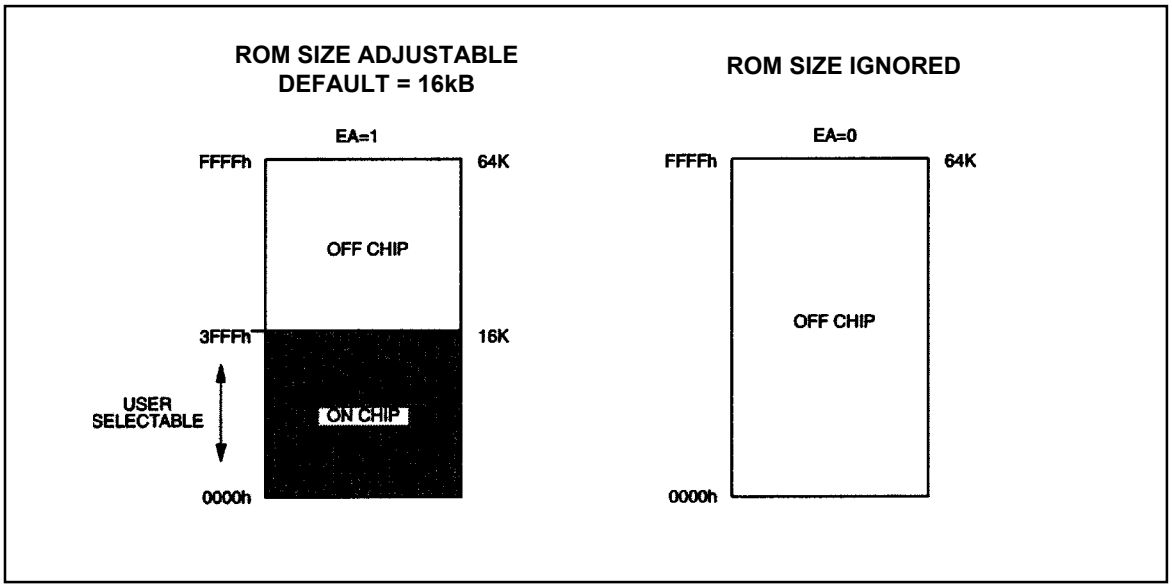
The reset default condition is a maximum on-chip ROM address of 16kB. Thus no action is required if this feature is not used. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2–RMS0. Altering these bits requires a Timed-Access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that the DS87C520/DS83C520 are executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code

from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520/DS83C520 contain on-chip data memory. They also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C520/DS83C520 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External data memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFFh	External data memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

Note: After internal MOVX SRAM has been initialized, changing the DME0/1 bits has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C520/DS83C520 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch

setting. When desiring maximum speed, software should select a Stretch value of 0. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. Also, setup and hold times are increased by 1 clock when using any Stretch greater than 0. This results in a wider read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the *Electrical Specifications* section. Table 3 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120ns RAMs without dramatically lengthening the memory access.

Table 3. Data Memory Cycle Stretch Values

CKCON.2-0			MEMORY CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME at 33MHz (ns)
M2	M1	M0			
0	0	0	2 (forced internal)	2	60
0	0	1	3 (default external)	4	121
0	1	0	4	8	242
0	1	1	5	12	364
1	0	0	6	16	485
1	0	1	7	20	606
1	1	0	8	24	727
1	1	1	9	28	848

DUAL DATA POINTER

The timing of block moves of data memory is faster using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS87C520/DS83C520, this data pointer is called DPTR0, located at SFR addresses 82h and 83h. These are the original locations. Using DPTR requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR0 and 1 once software loads them. The relevant register locations are as follows:

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

POWER MANAGEMENT

Along with the standard Idle and power down (Stop) modes of the standard 80C52, the DS87C520/DS83C520 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C520/DS83C520 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C520/DS83C520 use four clocks per machine cycle. Thus the instruction cycle rate is Clock/4. At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slow and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle mode, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle, and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520/DS83C520 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h).

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Switchback

To return to a 4-clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C520/DS83C520 provide several hardware alternatives for automatic Switchback. If Switchback is enabled, then the device will automatically return to a 4-clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled (REN = 1). Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A switchback will also occur when a byte is written to SBUF0 or SBUF1 for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{\text{INT0}}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{\text{INT0}}$ if the CPU is servicing a high priority interrupt.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C520/DS83C520 support three levels of interrupt priority. These levels are Power-fail, High, and Low. Bits STATUS.7-5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS. 7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port 0 Receive Activity (SPRA0;STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port 0 Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. These bits should be interrogated before entering PMM1 or PMM2 to ensure that no serial port operations are in progress. Changing the clock divisor rate during a serial transmission or reception will corrupt the operation.

Crystal/Ring Operation

The DS87C520/DS83C520 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C520/DS83C520 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP=1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

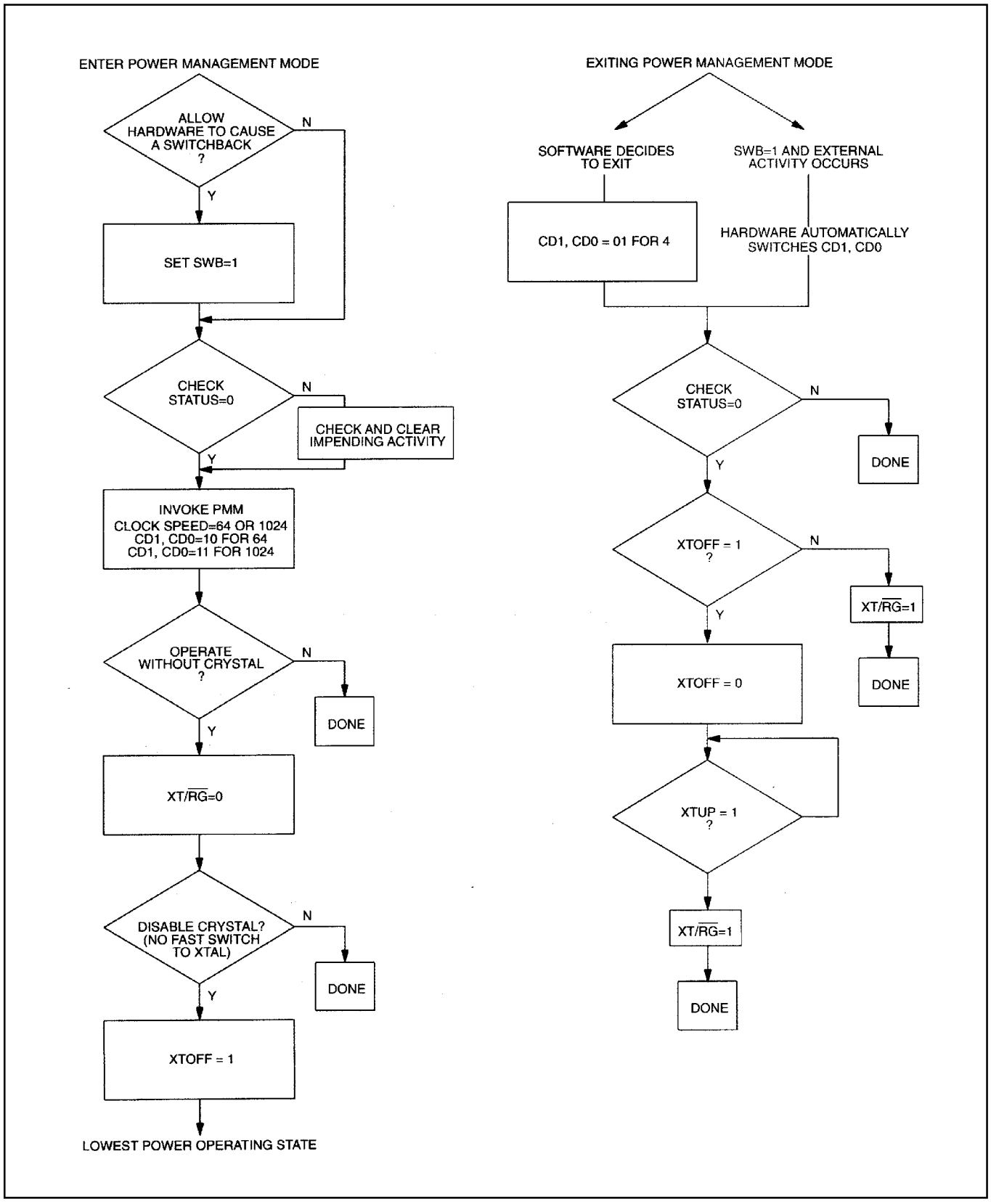
Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Figure 3 illustrates a typical decision set associated with PMM. Table 6 is a summary of the bits relating to PMM and its operation.

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$ = 1, runs from crystal or external clock; XT/$\overline{RG}$ = 0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF = 0
RGMD	EXIF.2	Status. RGMD = 1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

Figure 3. Invoking and Clearing PMM



IDLE MODE

Setting the lsb of the Power Control register (PCON;87h) invokes the Idle mode. Idle will leave internal clocks, serial ports and timers running. Power consumption drops because the CPU is not active. Since clocks are running, the Idle power consumption is a function of crystal frequency. It should be approximately one-half the operational power at a given frequency. The CPU can exit the Idle state with any interrupt or a reset. Idle is available for backward software compatibility. The system can now reduce power consumption to below Idle levels by using PMM1 or PMM2 and running NOPs.

STOP MODE ENHANCEMENTS

Setting Bit 1 of the Power Control register (PCON; 87h) invokes the Stop mode. Stop mode is the lowest power state since it turns off all internal clocking. The I_{CC} f a standard Stop mode is approximately 1µA (but is specified in the Electrical Specifications). The CPU will exit Stop mode from an eternal interrupt or a reset condition. Internally generated interrupts (timer, serial port, Watchdog) are not useful since they require clocking activity.

The DS87C520/DS83C520 provide two enhancements to the Stop mode. As documented below, the device provides a bandgap reference to determine Power-Fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off while in Stop mode. This allows the extremely low-power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. With the bandgap reference enabled, PFI and Power-fail Reset are functional and are a valid means for leaving Stop mode. This allows software to detect and compensate for a brownout or power supply sag, even when in Stop mode. In Stop mode with the bandgap enabled, I_{CC} will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain disabled. Only the most power-sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF; 91h). Setting BGS (EXIF.0) to a 1 will keep the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being off during Stop mode. Note that this bit has no control of the reference during full power, PMM, or Idle modes.

The second feature allows an additional power saving option while also making Stop easier to use. This is the ability to start instantly when exiting Stop mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

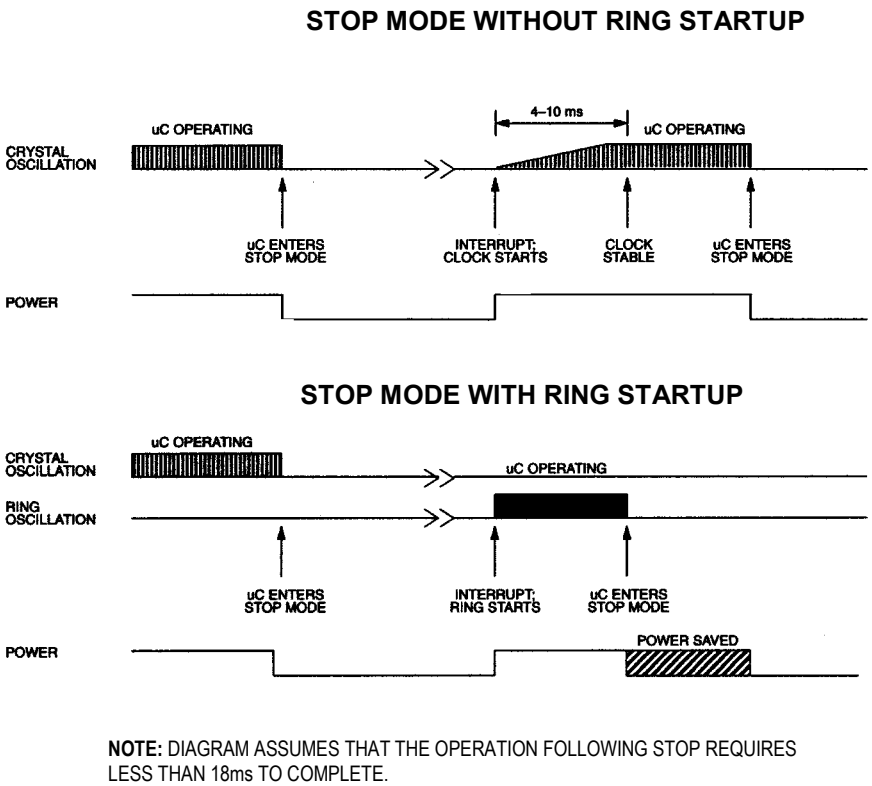
Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual startup time is crystal-dependent, but is normally at least 4ms. A common recommendation is 10 ms. In an application that will wake up, perform a short operation, then return to sleep, the crystal startup can be longer than the real transaction. However, the ring oscillator will start instantly. Running from the ring, the user can perform a simple operation and return to sleep before the crystal has even started. If a user selects the ring to provide the startup clock and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65,536 clocks) has expired. Hardware uses this value to assure proper crystal start even though power is not being cycled.

The ring oscillator runs at approximately 2MHz to 4MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. Figure 3 shows

how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL - Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD-Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 4. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The microcontroller allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static mode when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C520/DS83C520 provide several of the most commonly needed peripheral functions in micro-computer-based systems. These new functions include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C520/DS83C520 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C520/DS83C520 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C520/DS83C520 architecture normally uses four clocks per machine cycle. However, in the area of timers and serial ports, the DS87C520/DS83C520 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON;8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C520/DS83C520 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C520/DS83C520 use 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C520/DS83C520 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power-Fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

To prevent software from losing control, the DS87C520/DS83C520 include a programmable Watchdog Timer. The Watchdog is a free-running timer that sets a flag if allowed to reach a preselected timeout. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag, which generates reset. Software must restart the timer before it reaches its timeout or the processor is reset.

Software can select one of four timeout values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a "Timed Access" circuit. This prevents errant software from accidentally clearing the Watchdog. Timeout values are precise since they are a function of the crystal frequency as shown in Table 7. For reference, the time periods at 33MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time-base generator or can wake-up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON-8Eh), Watchdog Control (WDCON-D8h), and Extended Interrupt Enable (EIE-E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog timeout period as shown in Table 7.

Table 7. Watchdog Timeout Values

WD1	WD2	INTERRUPT TIMEOUT	TIME (33 MHz)	RESET TIMEOUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	2^{17} + 512 clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	2^{20} + 512 clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	2^{23} + 512 clocks	254.21 ms
1	1	2^{26} clocks	2033.60 ms	2^{26} + 512 clocks	2033.62 ms

As shown in Table 7, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; and 2^{26} = 67,108,864 clocks. The times shown in Table 7 are with a 33MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware

will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable.

There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source.

EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the timeout. Both of these bits are protected by Timed Access. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

INTERRUPTS

The DS87C520/DS83C520 provide 13 interrupt sources with three priority levels. The Power-Fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power-Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Timeout Interrupt	63h	13	DALLAS

TIMED-ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV     0C7h,   #0Aah
MOV     0C7h,   #55h
```

Writing an AAh then a 55h to the Timed Access register (location C7h) opens a 3-cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Bandgap Select
WDCON.6	POR	Power-On Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RMS2	ROM Size Select 2
ROMSIZE.1	RMS1	ROM Size Select 1
ROMSIZE.0	RMS0	ROM Size Select 0

EPROM PROGRAMMING

The DS87C520 follows standards for a 16kB EPROM version in the 8051 family. It is available in a UV-erasable, ceramic-windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options. ROM-specific features are described later in this data sheet.

Most commercially available device programmers will directly support Dallas Semiconductor microcontrollers. If your programmer does not, please contact the manufacturer for updated software.

PROGRAMMING PROCEDURE

The DS87C520 should run from a clock speed between 4MHz and 6MHz when being programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 9. The diagram in Table 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the *Electrical Specifications* section.

Program the DS87C520 as follows:

1) Apply the address value,
2) Apply the data value,
3) Select the programming option from Table 9 using the control signals,
4) Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5) Pulse the $\overline{PROG}$ signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6) Repeat as many times as necessary.

Table 9. EPROM Programming Modes

MODE		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	PL	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0-3Fh		H	L	PL	12.75V	L	H	H	L	H
Program Lock Bits	LB1	H	L	PL	12.75V	H	H	H	H	H
	LB2	H	L	PL	12.75V	H	H	H	L	L
	LB3	H	L	PL	12.75V	H	L	H	H	L
Program Option Register Address FCh		H	L	PL	12.75V	L	H	H	L	L
Read Signature or Option Registers 30, 31, 60 FCh		H	L	H	H	L	L	L	L	L

Table 10. DS87C520 EPROM Lock Bits

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted verify if encryption table was programmed.
2	P	U	U	Prevent MOVC instructions in external memory from reading program bytes in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevent MOVX instructions in external memory from reading SRAM (MOVX) in internal memory.
4	P	P	P	Level 3 plus no external execution.

SECURITY OPTIONS

The DS87C520 employs a standard three-level lock that restricts viewing of the EPROM contents. A 64-byte Encryption Array allows the authorized user to verify memory by presenting the data in encrypted form.

Lock Bits

The security lock consists of three lock bits. These bits select a total of four levels of security. Higher levels provide increasing security but also limit application flexibility. Table 10 shows the security settings. Note that the programmer cannot directly read the state of the security lock. User software has access to this information as described in the *Memory* section.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 9. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C520 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 9. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

Bits 7 to 4 Reserved, program to a 1.

Bit 3 Watchdog POR default. Set = 1; watchdog reset function is disabled on power-up. Set = 0; watchdog reset function is enabled automatically.

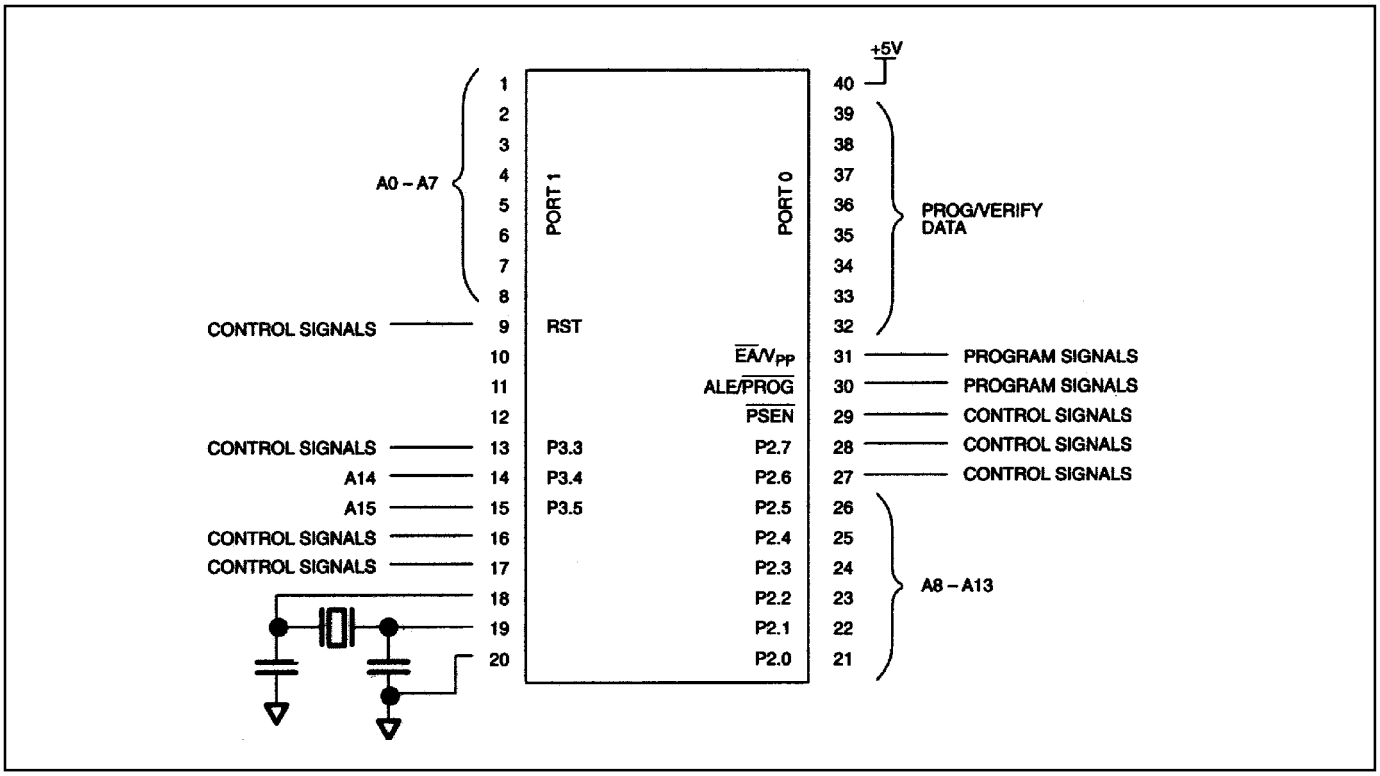
Bits 2 to 0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	20h	Model
60h	01h	Extension

Figure 5. EPROM Programming Configuration



ROM-SPECIFIC FEATURES

The DS83C520 supports a subset of the EPROM features found on the DS87C520.

SECURITY OPTIONS

Lock Bits

The DS83C520 employs a lock that restricts viewing of the ROM contents. When set, the lock will prevent MOVC instructions in external memory from reading program bytes in internal memory. When locked, the $\overline{EA}$ pin is sampled and latched on reset. The lock setting is enabled or disabled when the devices are manufactured according to customer specifications. The lock bit cannot be read in software, and its status can only be determined by observing the operation of the device.

Encryption Array

The DS83C520 Encryption Array allows an authorized user to verify ROM without allowing the true memory contents to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the ROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the Encryption Array is programmed (or optionally left unprogrammed) when the devices are manufactured according to customer specifications.

DS83C520 ROM VERIFICATION

The DS83C520 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 5, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C520 SIGNATURE

The Signature bytes identify the DS83C520 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	21h	Model
60h	01h	Extension

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground..……-0.3V to +6.0V
Operating Temperature Range……0°C to +70°C
Storage Temperature……-55°C to +125°C
Soldering Temperature..……..See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	2
Power-Fail Warning	DS87C520	V_{PFW}	4.25	4.38	4.5	V	2
	DS83C520		4.25	4.38	4.55		
Minimum Operating Voltage	DS87C520	V_{RST}	4.0	4.13	4.25	V	2
	DS83C520		4.0	4.13	4.275		
Supply Current Active Mode at 33MHz		I_{CC}		30	45	mA	3
Supply Current Idle Mode at 33MHz		I_{IDLE}		15	25	mA	4
Supply Current Stop Mode, Bandgap Disabled (0°C to +70°C)		I_{STOP}		1	100	µA	5
Supply Current Stop Mode, Bandgap Disabled (-40°C to +85°C)				1	150	µA	5
Supply Current Stop Mode, Bandgap Enabled (0°C to +70°C)		I_{SPBG}		50	170	µA	5
Supply Current Stop Mode, Bandgap Enabled (-40°C to +85°C)				50	195	µA	5
Input Low Level		V_{IL}	-0.3		+0.8	V	2
Input High Level (except XTAL1 and RST)		V_{IH}	2.0		V_{CC} + 0.3	V	2
Input High Level XTAL1 and RST		V_{IH2}	3.5		V_{CC} + 0.3	V	2
Output Low Voltage, Ports 1 and 3 at I_{OL} = 1.6mA		V_{OL1}		0.15	0.45	V	2
Output Low Voltage Ports 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA		V_{OL2}		0.15	0.45	V	2
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA		V_{OH1}	2.4			V	2, 7
Output High Voltage Ports 1, 2, 3 at I_{OH} = -1.5mA		V_{OH2}	2.4			V	2, 8
Output High Voltage Port 0, 2, ALE, $\overline{PSEN}$ in Bus Mode at I_{OH} = -8mA		V_{OH3}	2.4			V	2, 6
Input Low Current Ports 1, 2, 3 at 0.45V		I_{IL}			-70	µA	12

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Current from 1 to 0 Ports 1, 2, 3 at 2V	I_{TL}			-800	µA	9
Input Leakage Port 0, and $\overline{EA}$ pins, I/O Mode	I_L	-10		+10	µA	11
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	10
RST Pulldown Resistance	R_{RST}	50		200	kΩ	

Note 1: All parameters apply to both commercial and industrial temperature operation, unless otherwise noted.

Note 2: All voltages are referenced to ground.

Note 3: Active current measured with 33MHz clock source on XTAL1, V_{CC} = RST = 5.5V, other pins disconnected.

Note 4: Idle mode current measured with 33MHz clock source on XTAL1, V_{CC} = 5.5V, RST at ground, other pins disconnected.

Note 5: Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.

Note 6: When addressing external memory. This specification only applies to the first clock cycle following the transition.

Note 7: RST = V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

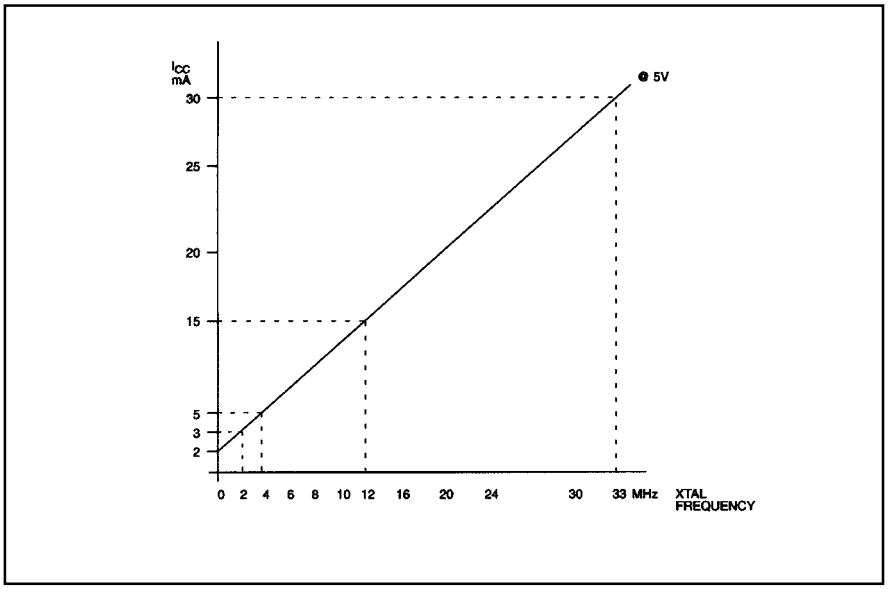
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

Note 10: 0.45 < V_{IN} < V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

Note 11: 0.45 < V_{IN} < V_{CC}. RST = V_{CC}. This condition mimics operation of pins in I/O mode.

Note 12: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

TYPICAL I_{CC} vs. FREQUENCY



AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low		t_{LLAX1}	(Note 2)		(Note 2)		ns
ALE Low to Valid Instruction In		t_{LLIV}		43		$2.5t_{CLCL}$-33	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}	4		$0.5t_{CLCL}$-11		ns
$\overline{PSEN}$ Pulse Width		t_{PLPH}	55		$2t_{CLCL}$-5		ns
$\overline{PSEN}$ Low to Valid Instruction In		t_{PLIV}		37		$2t_{CLCL}$-24	ns
Input Instruction Hold after $\overline{PSEN}$		t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{PSEN}$		t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		59		$3t_{CLCL}$-32	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		68		$3.5t_{CLCL}$-38	ns
$\overline{PSEN}$ Low to Address Float		t_{PLAZ}		(Note 2)		(Note 2)	ns

Note 1: All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics are not 100% tested, but are characterized and guaranteed by design. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$-5		ns	t_{MCS}=0
		$2t_{CLCL}$-5			t_{MCS}>0
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}$-5		ns	t_{MCS}=0
		t_{CLCL}-5			t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$-10		ns	t_{MCS}=0
		t_{CLCL}-7			t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-22	ns	t_{MCS}=0
			t_{MCS}-24		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	—
Data Float after Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-31	ns	t_{MCS}=0
			$t_{MCS}+t_{CLCL}$-26		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-29	ns	t_{MCS}=0
			$t_{MCS}+2t_{CLCL}$-29		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-37	ns	t_{MCS}=0
			$t_{MCS}+2.5t_{CLCL}$-37		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-10	$0.5t_{CLCL}$+5	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-9		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-17		ns	t_{MCS}=0
		$2.5t_{CLCL}$-16			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-6		ns	—
Data Hold after Write	t_{WHQX}	t_{CLCL}-5		ns	t_{MCS}=0
		$2t_{CLCL}$-6			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 1)	ns	—
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-4	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0

Note 1: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

MOVX CHARACTERISTICS (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, the DS87C520 and DS83C520 specify the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time	I	Instruction	W	$\overline{WR}$ signal
A	Address	P	$\overline{PSEN}$	X	No longer a valid logic level
C	Clock	Q	Output data		
D	Input data	R	$\overline{RD}$ signal	Z	Tri-State
H	Logic level high	V	Valid		
L	Logic level low				

POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

Note 1: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox.

Note 2: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

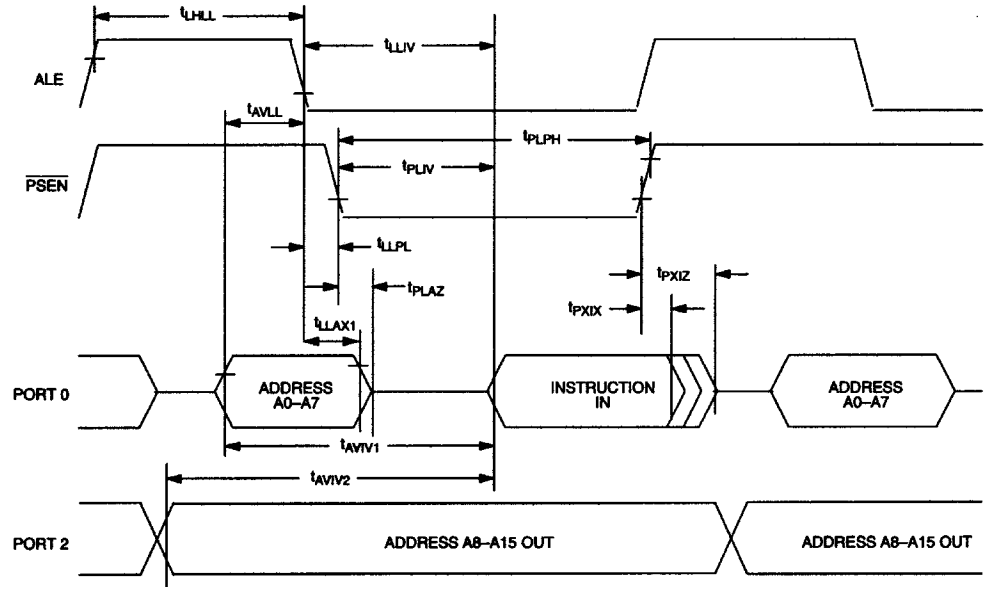
EPROM PROGRAMMING AND VERIFICATION

(V_{CC} = 4.5V to 5.5V, T_A = +21°C to +27°C.)

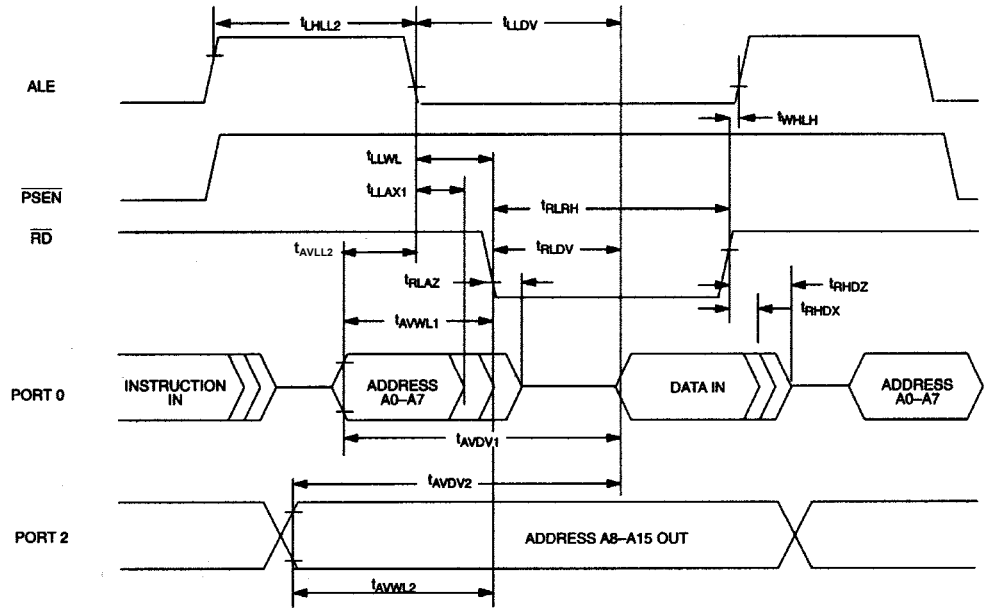
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	48 t_{CLCL}				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	48 t_{CLCL}				
Data Hold after $\overline{PROG}$	t_{GHDX}	48 t_{CLCL}				
Enable High to V_{PP}	t_{EHSH}	48 t_{CLCL}				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{SHGL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			48 t_{CLCL}		
Enable Low to Data Valid	t_{ELQV}			48 t_{CLCL}		
Data Float after Enable	t_{EHQZ}	0		48 t_{CLCL}		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

Note 1: All voltages are referenced to ground.

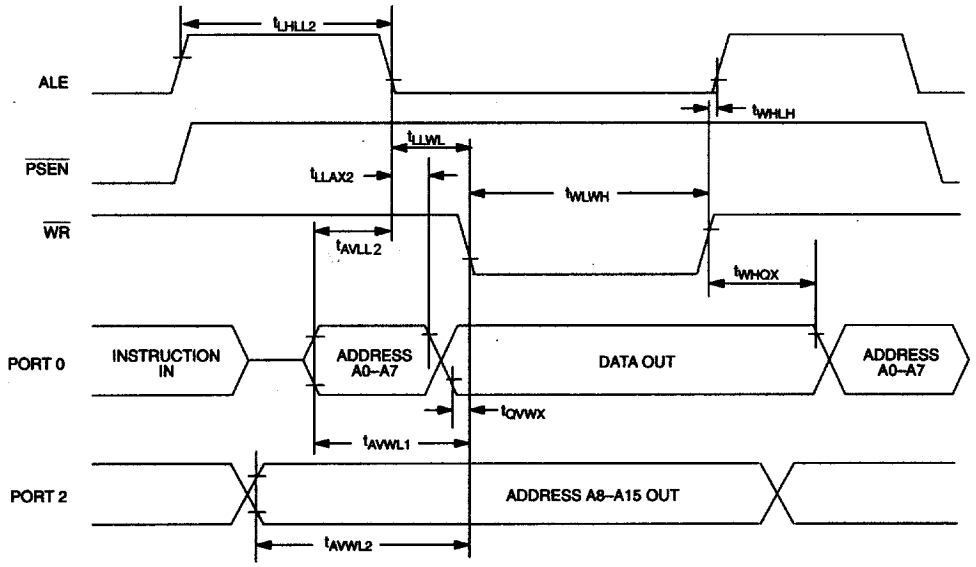
EXTERNAL PROGRAM MEMORY READ CYCLE



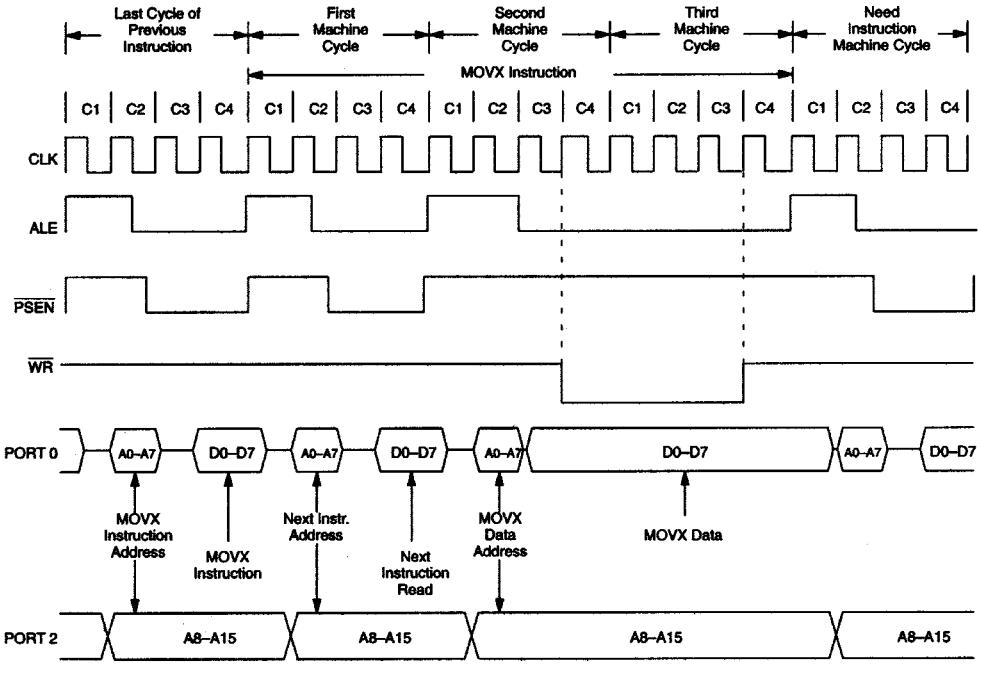
EXTERNAL DATA MEMORY READ CYCLE



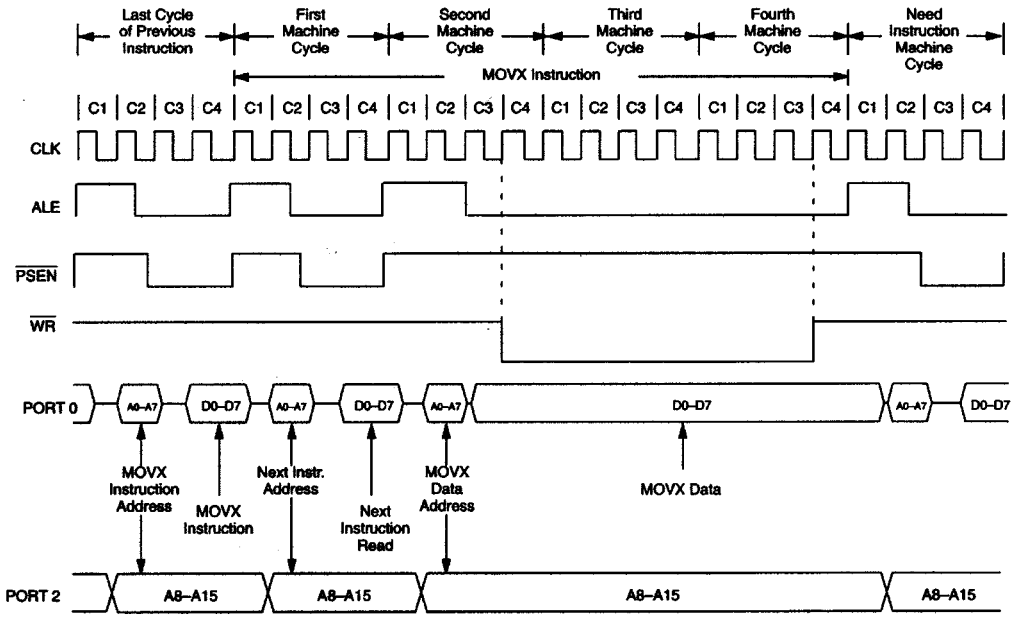
EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

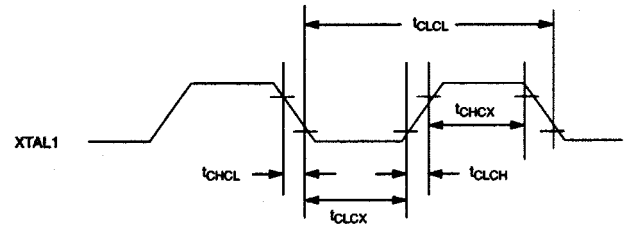


DATA MEMORY WRITE WITH STRETCH = 2

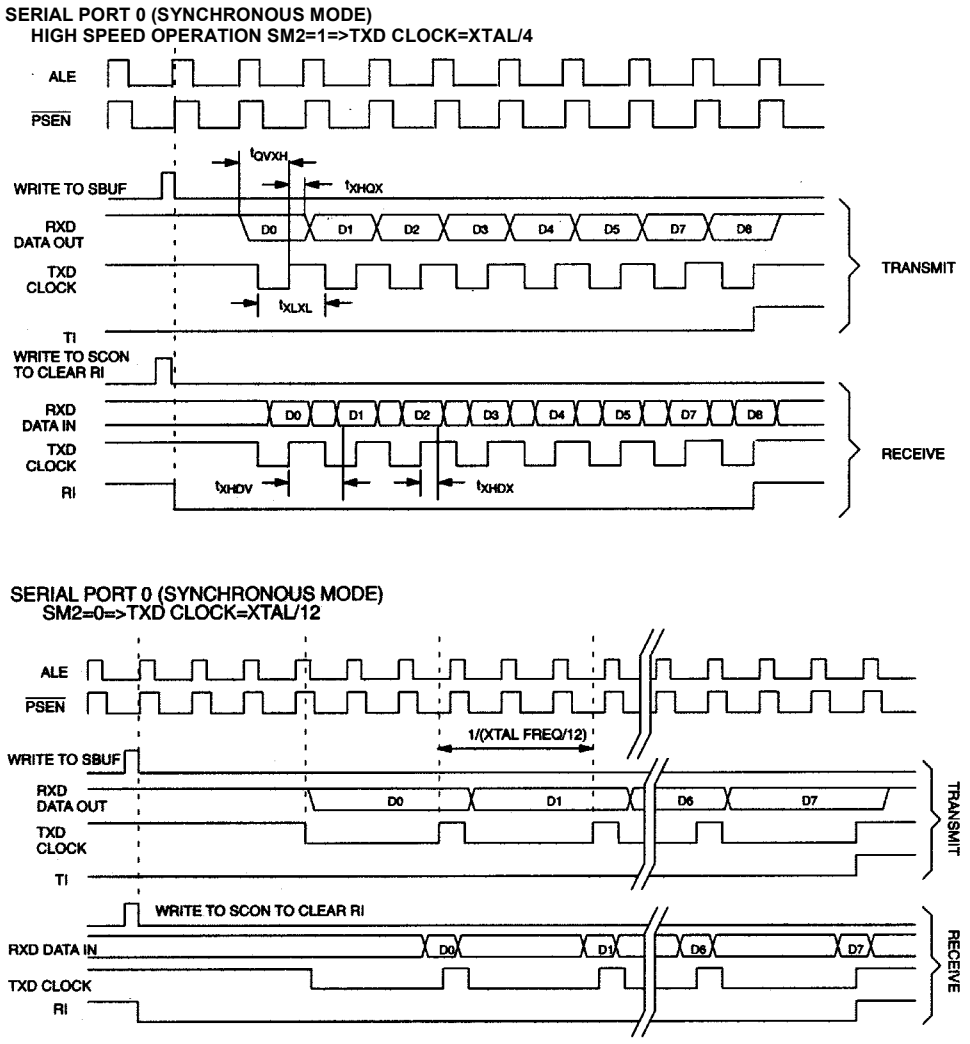


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

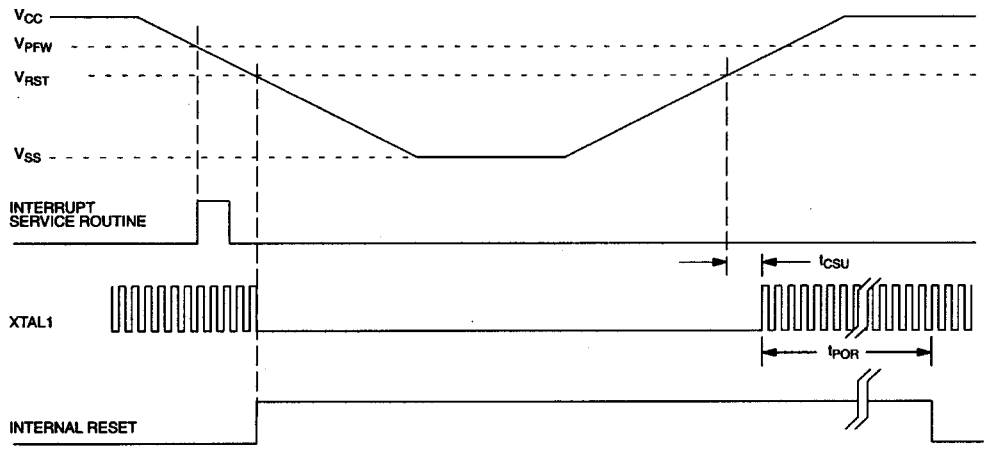
EXTERNAL CLOCK DRIVE



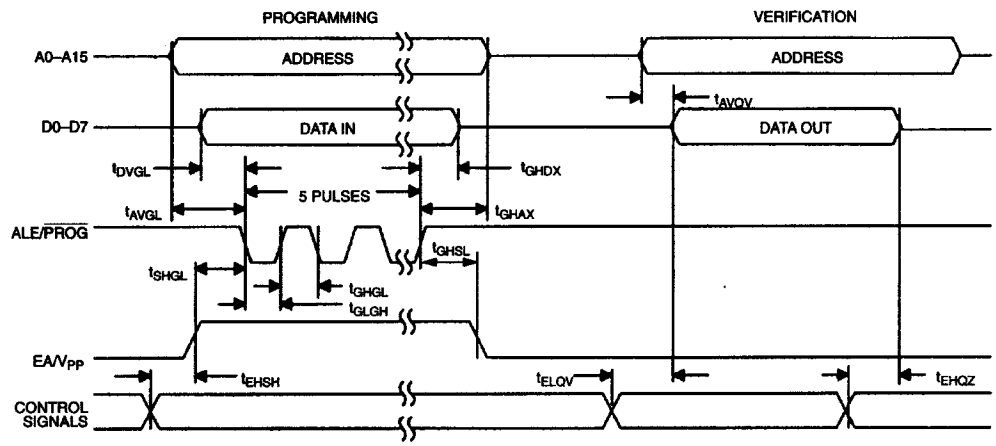
SERIAL PORT MODE 0 TIMING



POWER-CYCLE TIMING



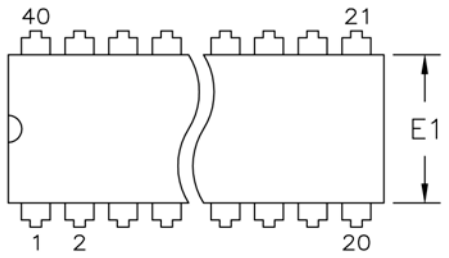
EPROM PROGRAMMING AND VERIFICATION WAVEFORMS

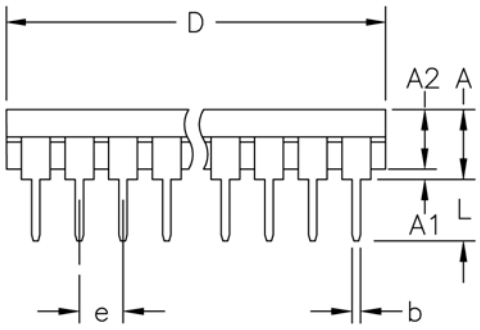


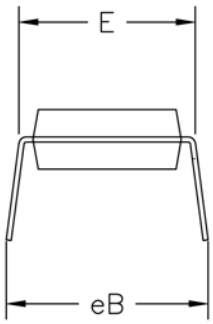
PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		







	40 PIN	
	MIN	MAX
A	–	0.200
A1	0.015	–
A2	0.140	0.160
b	0.014	0.022
c	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
e	0.090	0.110
L	0.115	0.145
eB	0.600	0.700

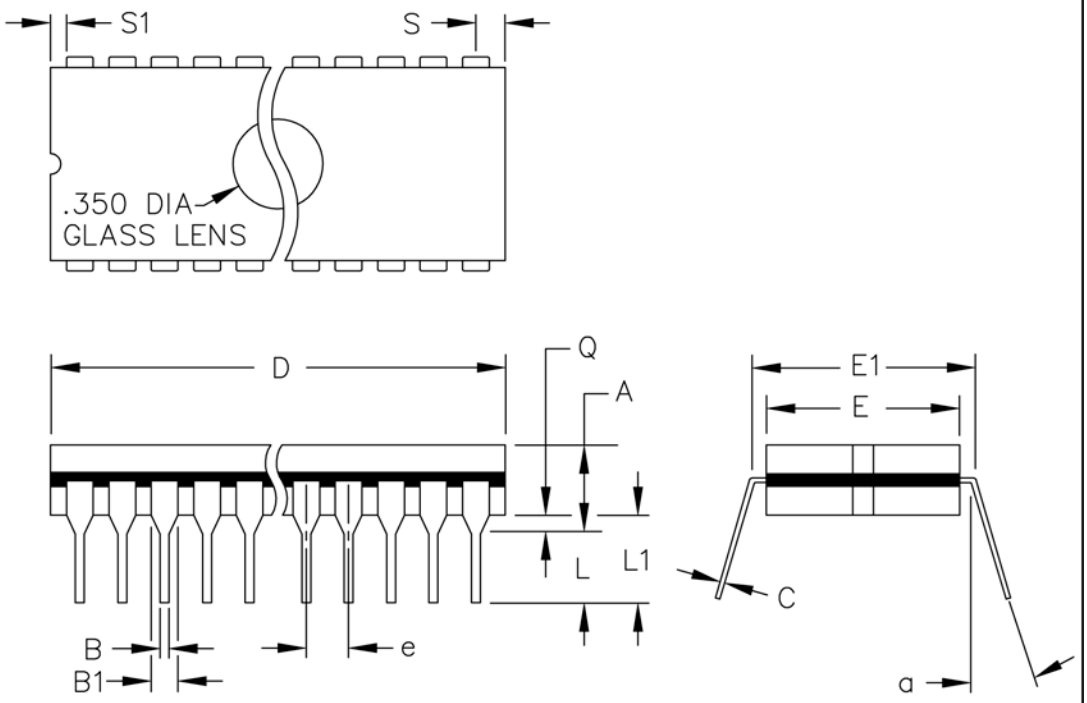
ALL DIMENSIONS ARE IN INCHES

SIGNATURE	DATE	DALLAS SEMICONDUCTOR MAXIM			
DOC. CONTROL:					
ENGR. MGR:		TITLE: MARKETING OUTLINE, 40 LEAD PLASTIC DUAL–IN–LINE PACKAGE (0.600")			
MFG. ENGR:					
CHECKED BY:					
DRAWN BY: R. RADKE	1/95	SIZE A	FSCM NO	PART NO. 56–G5000–000	REV A
DO NOT SCALE DWG.		SCALE N/A		SHEET 1 OF 1	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		



LTR	MIN	MAX
A	–	.225
B	.014	.023
B1	.038	.065
C	.006	.015
D	–	2.096
E	.510	.620
E1	.590	.630
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	–	.098
S1	.005	–
a	0°	15°

ALL DIMENSIONS SHOWN ARE IN INCHES.

SIGNATURE		DATE
DOC. CONTROL:		
ENGR. MGR:		
MFG. ENGR:		
CHECKED BY:		
DRAWN BY:	M.W.C.	5/94
DO NOT SCALE DWG.		

DALLAS SEMICONDUCTOR MAXIM

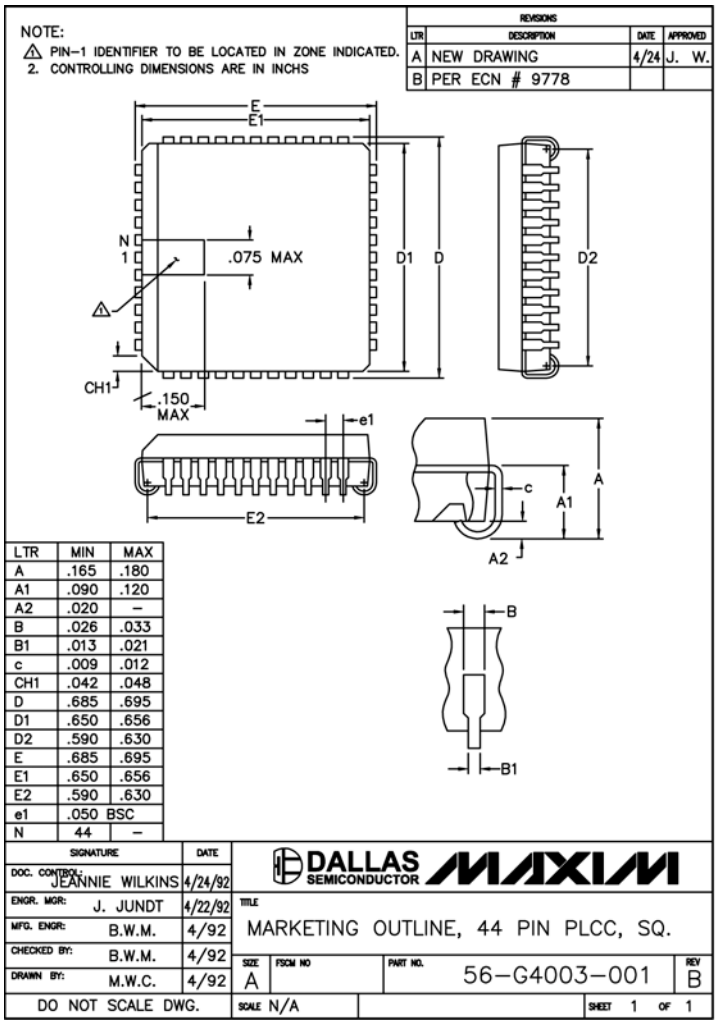
TITLE: MARKETING OUTLINE, 40–PIN CERAMIC DUAL–IN–LINE PACKAGE WITH GLASS LENS

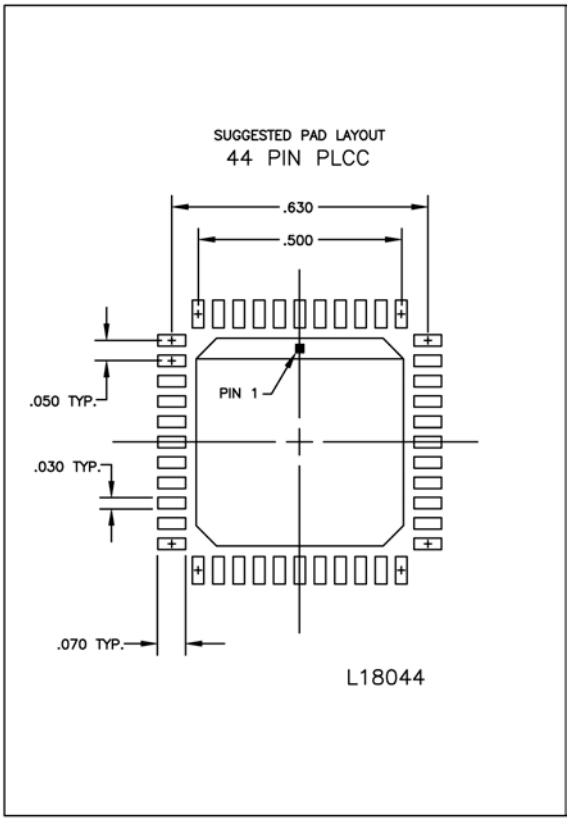
SIZE	FSCM NO	PART NO.	REV
A		56–G4008–001	A

SCALE N/A SHEET 1 OF 1

PACKAGE INFORMATION (continued)

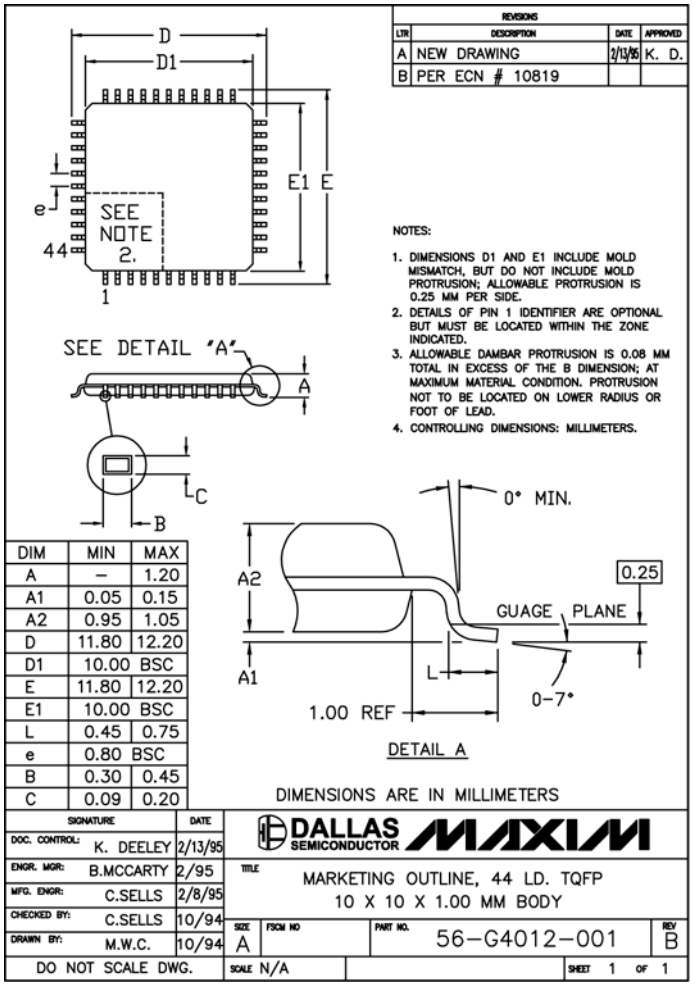
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

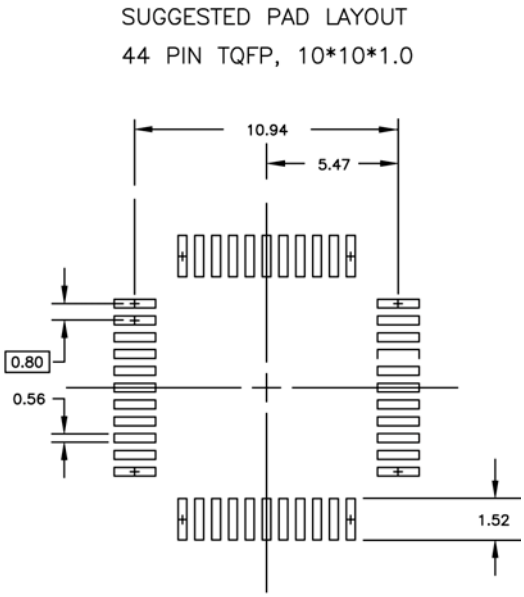




PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)





DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
091605	1) In DC Electrical Characteristics table, added separate specification for DS83C520 V_{PFW}. 2) Changed V_{RST} max to from 4.25V to 4.275V for DS83C520 value.
070505	3) Added Pb-free/RoHS-compliant part numbers to Ordering Information table. 4) Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.
040104	5) Removed "Preliminary" status. 6) Soldering temperature parameter now references JEDEC specification. 7) Added note to absolute maximums clarifying voltages referenced to ground. 8) Updated I_{CC}, I_{IDLE}, I_{STOP}, I_{SPBG}, I_{IL}, and I_{TL} to incorporate errata conditions. 9) Added note clarifying DC electrical test conditions. 10) Added note clarifying V_{OH3} specification applies to first clock cycle following the transition. 11) Updated AC and MOVX electrical characteristics with final characterization values. 12) Added t_{AVLL2} specification and corrected MOVX timing diagrams to show t_{AVLL2} instead of t_{AVLL}.
070300	1) Corrected P0 pinout description for TQFP package. 2) Clarified point at which reset delay begins.
070698	1) Update PMM operating current estimates 2) Added note to clarify I_{IL} specification. 3) Added note to prevent accidental corruption of Watchdog Timer count while changing counter length. 4) Changed minimum oscillator frequency to 1MHz when using external crystal. 5) Changed RST pulldown resistance from 170kΩ to 200kΩ maximum. 6) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.
022097	1) Update ALE pin description. 2) Add note pertaining to erasure window. 3) Add note pertaining to internal MOVX SRAM. 4) Change Note 10 from RST = 5.5V to RST = V_{CC}. 5) Change serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}.
110195	Preliminary release.

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