Dual 12-Bit, High Bandwidth, Multiplying DAC with 4-Quadrant Resistors and Parallel Interface

AD5405

FEATURES

10 MHz multiplying bandwidth
On-chip 4-quadrant resistors allow flexible output ranges
INL of ±1 LSB
40-lead LFCSP package
2.5 V to 5.5 V supply operation
±10 V reference input
21.3 MSPS update rate
Extended temperature range: –40°C to 125°C
4-quadrant multiplication
Power-on reset
0.5 µA typical current consumption
Guaranteed monotonic
Readback function

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation applications
Programmable amplifiers and attenuators
Digitally controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5405[1] is a CMOS, 12-bit, dual-channel, current output digital-to-analog converter (DAC). This device operates from a 2.5 V to 5.5 V power supply, making it suited to battery-powered and other applications.

As a result of manufacture with a CMOS submicron process, the device offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier. This device also contains the 4-quadrant resistors necessary for bipolar operation and other configuration modes.

This DAC uses data readback, allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with 0s, and the DAC outputs are at zero scale.

The AD5405 has a 6 mm × 6 mm, 40-lead LFCSP package.

[1] U.S. Patent Number 5,689,257.

FUNCTIONAL BLOCK DIAGRAM

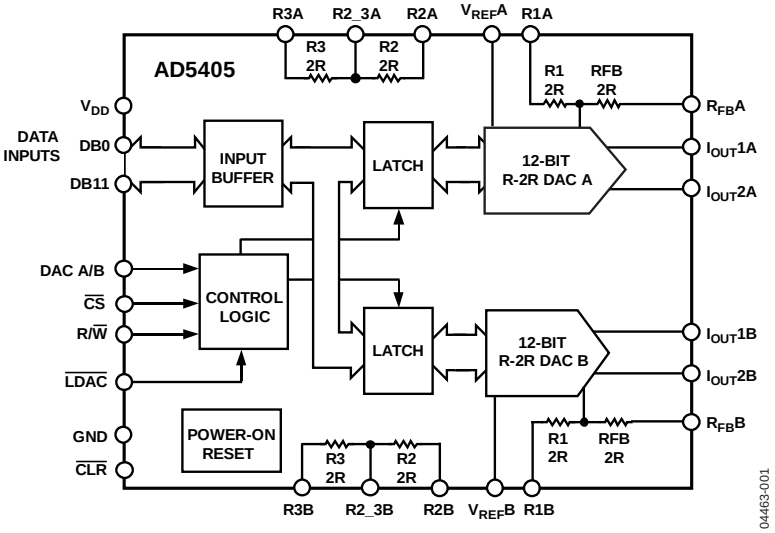


Figure 1.

Rev. B

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REVISION HISTORY

12/09—Rev. A to Rev. B

Changes to Figure 1 ... 1
Changes to Table 2 and Figure 2 ... 5
Changes to Table 4 and Figure 4 ... 7
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

7/05—Rev. 0 to Rev. A

Changed Pin DAC A/B to DAC $\overline{A}$/B ... Universal
Changes to Features List ... 1
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Changes to Timing Characteristics ... 5
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Added Figure 38 Through Figure 40 ... 18
Change to Power Supplies for the Evaluation Board Section ... 19
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

7/04—Revision 0: Initial Version

SPECIFICATIONS[1]

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. Temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance is measured with OP177, and ac performance is measured with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±25	mV	
Gain Error Temperature Coefficient		±5		ppm FSR/°C	
Bipolar Zero-Code Error			±25	mV	
Output Leakage Current			±1	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±15	nA	Data = 0x0000, T_A = −40°C to +125°C, $I_{OUT}1$
REFERENCE INPUT					
Reference Input Range		±10		V	
$V_{REF}A$, $V_{REF}B$ Input Resistance	8	10	13	kΩ	Input resistance TC = −50 ppm/°C
$V_{REF}A$-to-$V_{REF}B$ Input Resistance Mismatch		1.6	2.5	%	Typ = 25°C, max = 125°C
R1, R_{FB} Resistance	17	20	25	kΩ	Input resistance TC = −50 ppm/°C
R2, R3 Resistance	17	20	25	kΩ	Input resistance TC = −50 ppm/°C
R2-to-R3 Resistance Mismatch		0.06	0.18	%	Typ = 25°C, max = 125°C
Input Capacitance					
Code 0		3.5		pF	
Code 4095		3.5		pF	
DIGITAL INPUTS/OUTPUT					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 3.6 V to 5.5 V
	1.7			V	V_{DD} = 2.5 V to 3.6 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5.5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5.5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE					
Reference-Multiplying BW		10		MHz	V_{REF} = ±3.5 V p-p, DAC loaded all 1s
Output Voltage Settling Time					R_{LOAD} = 100 Ω, C_{LOAD} = 15 pF, V_{REF} = 10 V
					DAC latch alternately loaded with 0s and 1s
Measured to ±1 mV of FS		80	120	ns	
Measured to ±4 mV of FS		35	70	ns	
Measured to ±16 mV of FS		30	60	ns	
Digital Delay		20	40	ns	Interface time delay
10% to 90% Settling Time		15	30	ns	Rise and fall times
Digital-to-Analog Glitch Impulse		3		nV-sec	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error					DAC latch loaded with all 0s, V_{REF} = ±3.5 V
			70	dB	1 MHz
			48	dB	10 MHz
Output Capacitance		12	17	pF	DAC latches loaded with all 0s
		25	30	pF	DAC latches loaded with all 1s

Parameter	Min	Typ	Max	Unit	Conditions
Digital Feedthrough		1		nV-sec	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz
Analog THD		81		dB	V_{REF} = 3. 5 V p-p, all 1s loaded, f = 1 kHz
Digital THD					Clock = 10 MHz, V_{REF} = 3.5 V
100 kHz f_{OUT}		61		dB	
50 kHz f_{OUT}		66		dB	
SFDR Performance (Wideband)					V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50 kHz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					V_{REF} = 3.5 V
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	Clock = 10 MHz
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	Clock = 25 MHz
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.7	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.5	10	µA	T_A = −40°C to +125°C, logic inputs = 0 V or V_{DD}
Power Supply Sensitivity			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V, temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
Write Mode			
t_1	0	ns min	R/$\overline{W}$-to-$\overline{CS}$ setup time
t_2	0	ns min	R/$\overline{W}$-to-$\overline{CS}$ hold time
t_3	10	ns min	$\overline{CS}$ low time
t_4	10	ns min	Address setup time
t_5	0	ns min	Address hold time
t_6	6	ns min	Data setup time
t_7	0	ns min	Data hold time
t_8	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_9	7	ns min	$\overline{CS}$ min high time
t_{14}	10	ns typ	$\overline{CS}$ rising-to-$\overline{LDAC}$ falling time
t_{15}	12	ns typ	$\overline{LDAC}$ pulse width
t_{16}	10	ns typ	$\overline{CS}$ rising-to-$\overline{LDAC}$ rising time
t_{17}	10	ns typ	$\overline{LDAC}$ falling-to-$\overline{CS}$ rising time
Data Readback Mode			
t_{10}	0	ns typ	Address setup time
t_{11}	0	ns typ	Address hold time
t_{12}	5	ns typ	Data access time
	35	ns max	
t_{13}	5	ns typ	Bus relinquish time
	10	ns max	
Update Rate	21.3	MSPS	Consists of $\overline{CS}$ min high time, $\overline{CS}$ low time, and output voltage settling time

[1] Guaranteed by design and characterization, not subject to production test.

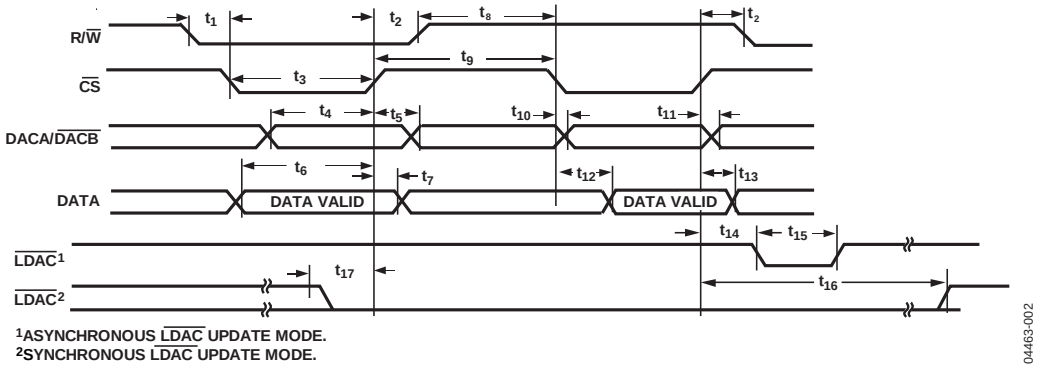


Figure 2. Timing Diagram

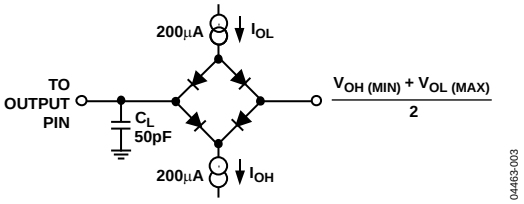


Figure 3. Load Circuit for Data Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.
T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
$V_{REF}A$, $V_{REF}B$, $R_{FB}A$, $R_{FB}B$ to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to +7 V
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
40-lead LFCSP, θ_{JA} Thermal Impedance	30°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at DBx, $\overline{LDAC}$, $\overline{CS}$, and R/$\overline{W}$ are clamped by internal diodes.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

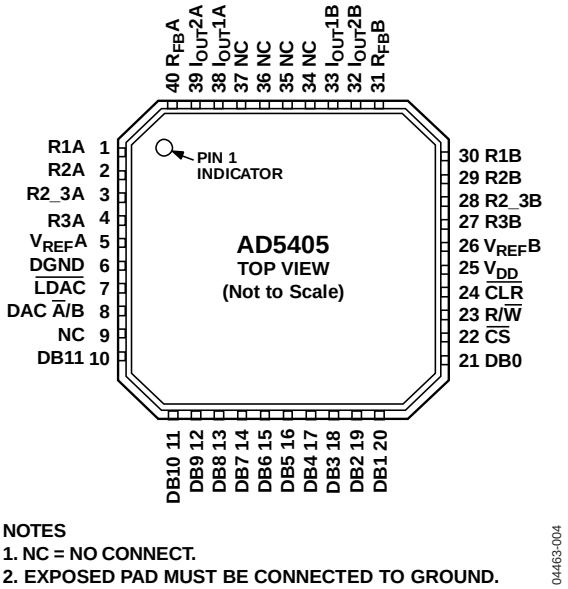


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	R1A, R2B, R2_3B, R3A	DAC A 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with minimum of external components.
5, 26	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
6	DGND	Digital Ground Pin.
7	$\overline{LDAC}$	Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the rising edge of $\overline{CS}$.
8	DAC $\overline{A}$/B	Selects DAC A or B. Low selects DAC A, and high selects DAC B.
9, 34 to 37	NC	Not internally connected.
10 to 21	DB11 to DB0	Parallel Data Bits 11 through 0.
22	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Edge sensitive; when pulled high, the DAC data is latched.
23	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of DAC register.
24	$\overline{CLR}$	Active Low Control Input. Clears DAC output and input and DAC registers.
25	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
27 to 30	R3B, R2_3B, R2B, R1B	DAC B 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with a minimum of external components.
31, 40	$R_{FB}B$, $R_{FB}A$	External Amplifier Output.
32	$I_{OUT}2B$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
33	$I_{OUT}1B$	DAC B Current Outputs.
38	$I_{OUT}1A$	DAC A Current Outputs.
39	$I_{OUT}2A$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
	EPAD	Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

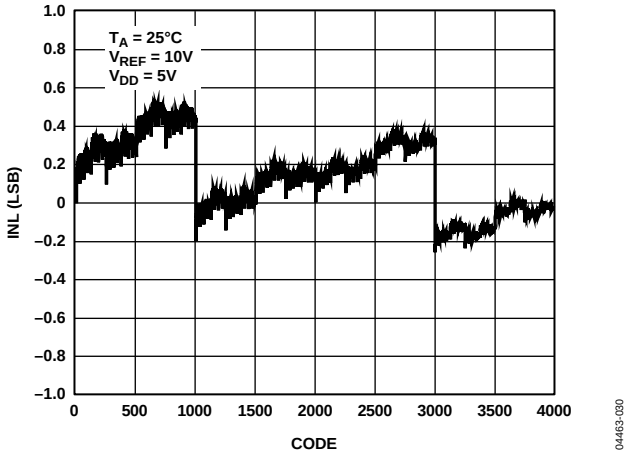


Figure 5. INL vs. Code (12-Bit DAC)

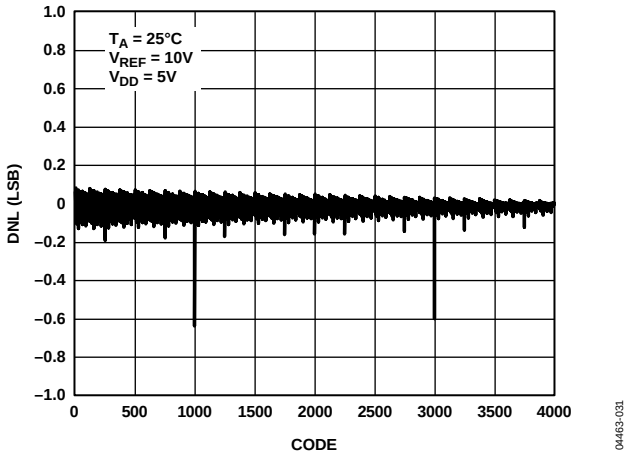


Figure 6. DNL vs. Code (12-Bit DAC)

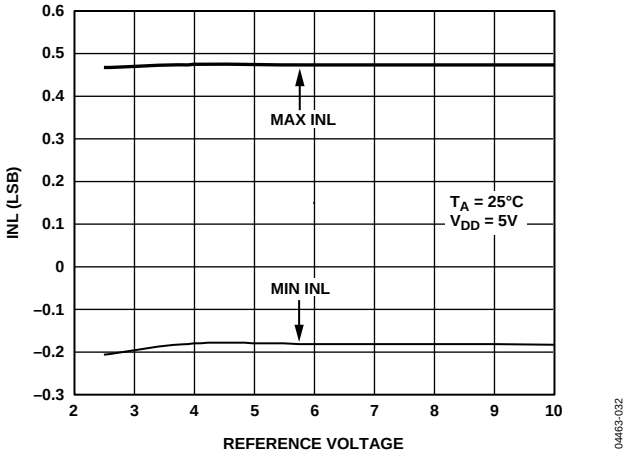


Figure 7. INL vs. Reference Voltage

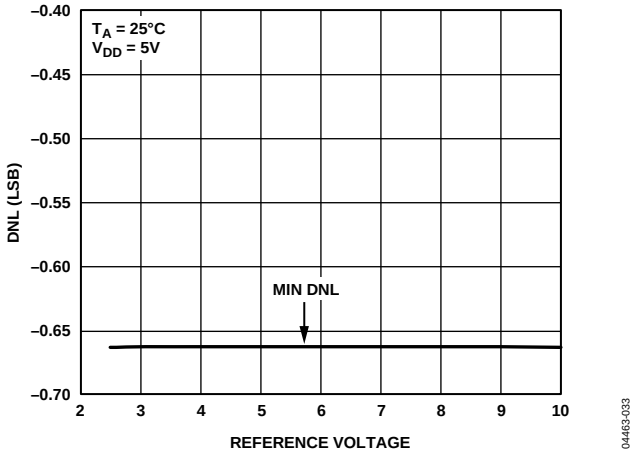


Figure 8. DNL vs. Reference Voltage

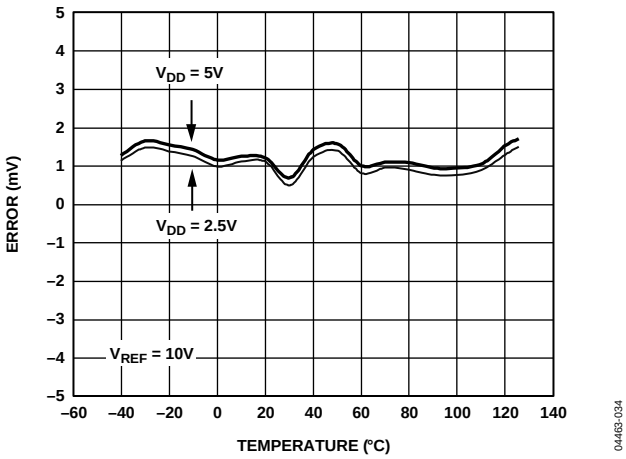


Figure 9. Gain Error vs. Temperature

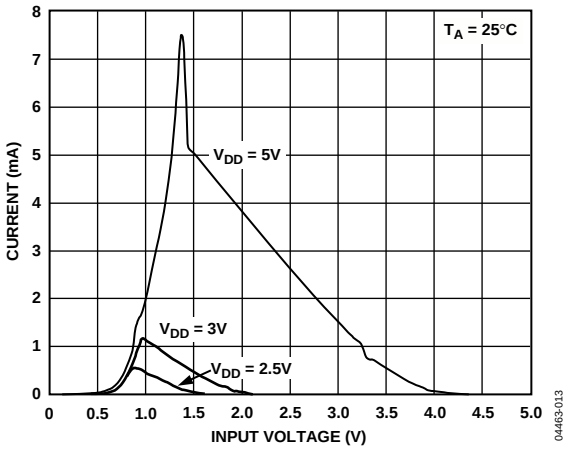


Figure 10. Supply Current vs. Logic Input Voltage

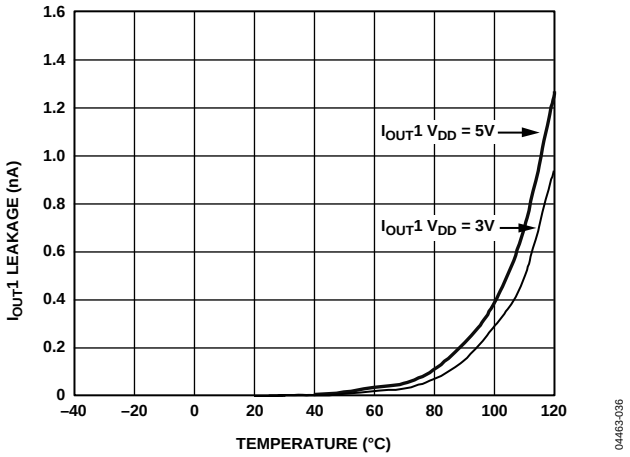


Figure 11. $I_{OUT}1$ Leakage Current vs. Temperature

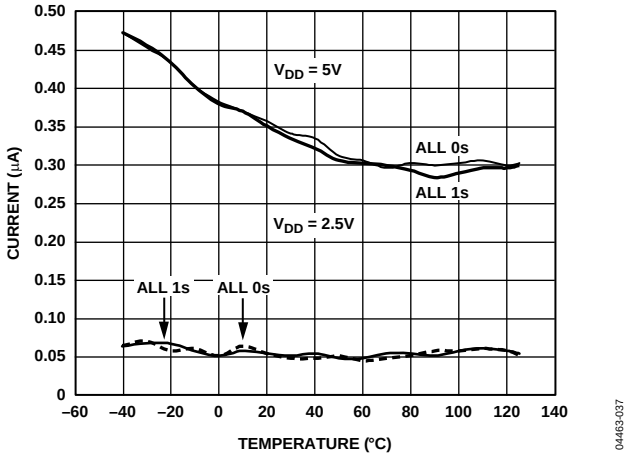


Figure 12. Supply Current vs. Temperature

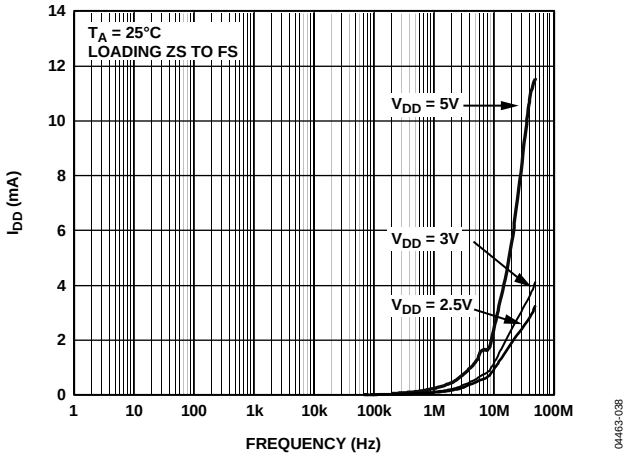


Figure 13. Supply Current vs. Update Rate

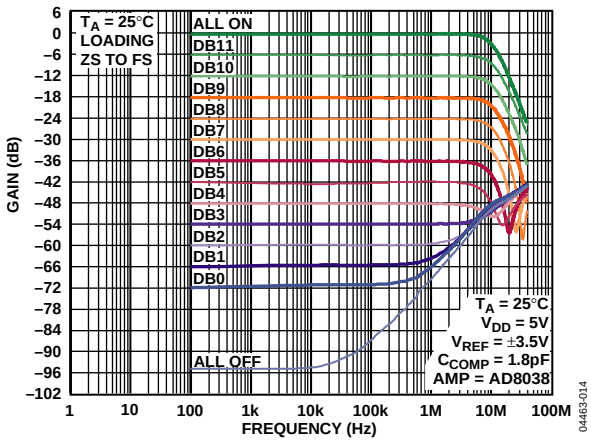


Figure 14. Reference Multiplying Bandwidth vs. Frequency and Code

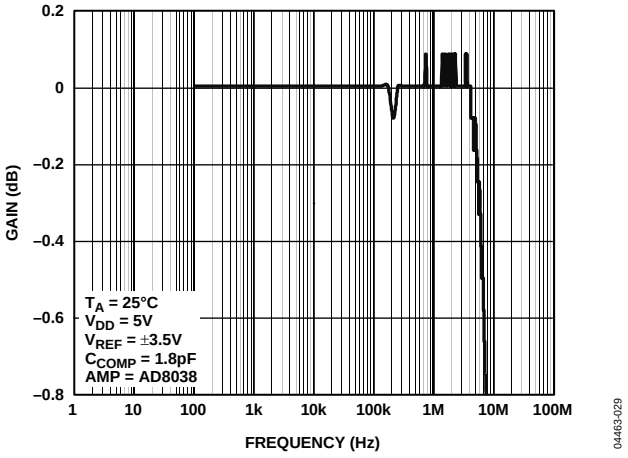


Figure 15. Reference Multiplying Bandwidth—All 1s Loaded

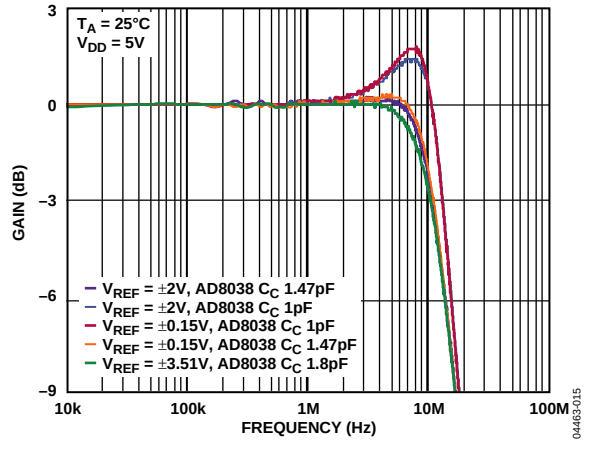


Figure 16. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

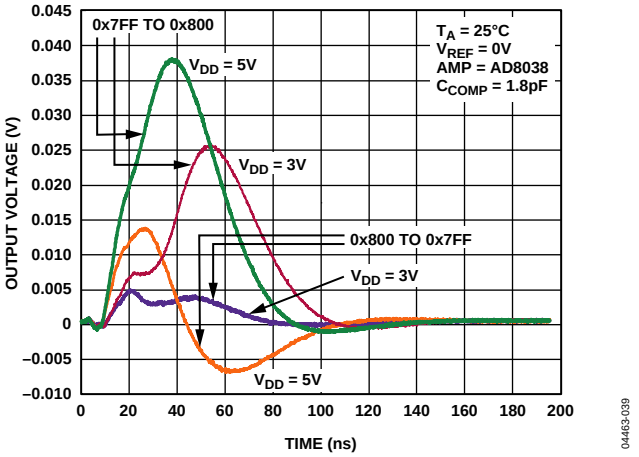


Figure 17. Midscale Transition, V_{REF} = 0 V

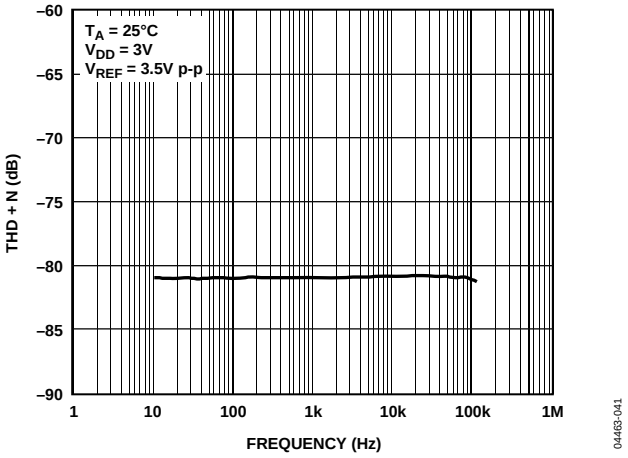


Figure 20. THD and Noise vs. Frequency

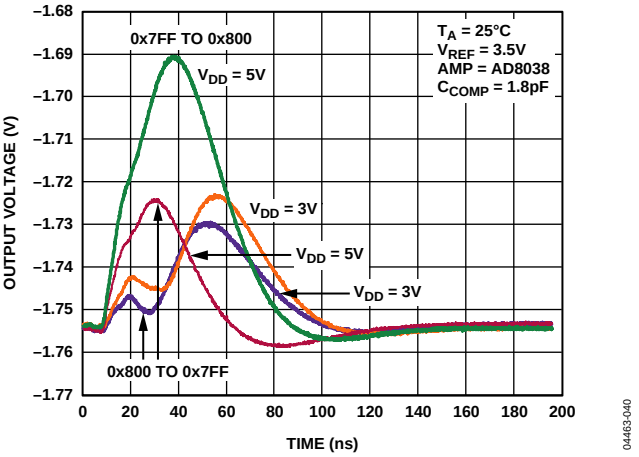


Figure 18. Midscale Transition, V_{REF} = 3.5 V

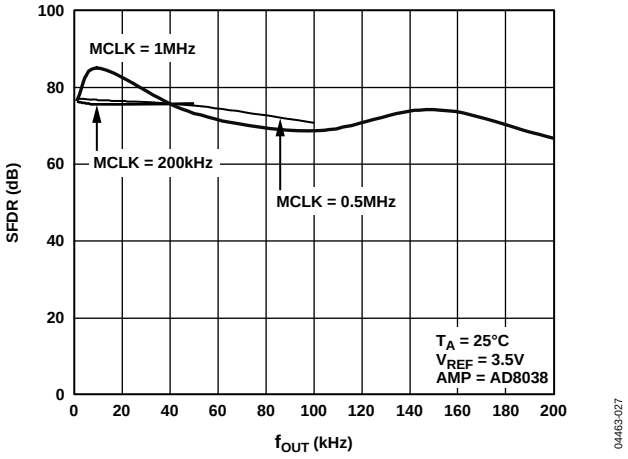


Figure 21. Wideband SFDR vs. f_{OUT} Frequency

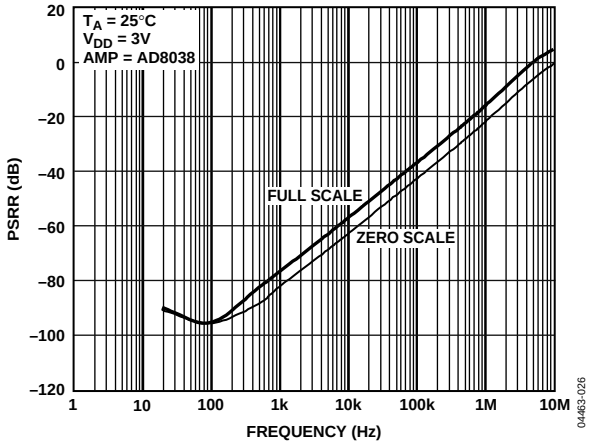


Figure 19. Power Supply Rejection Ratio vs. Frequency

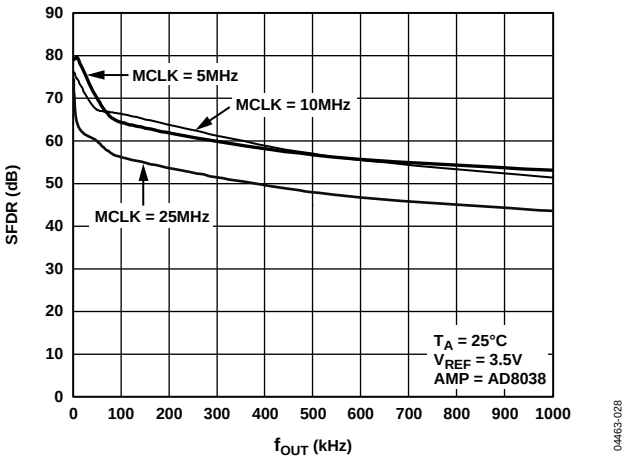


Figure 22. Wideband SFDR vs. f_{OUT} Frequency

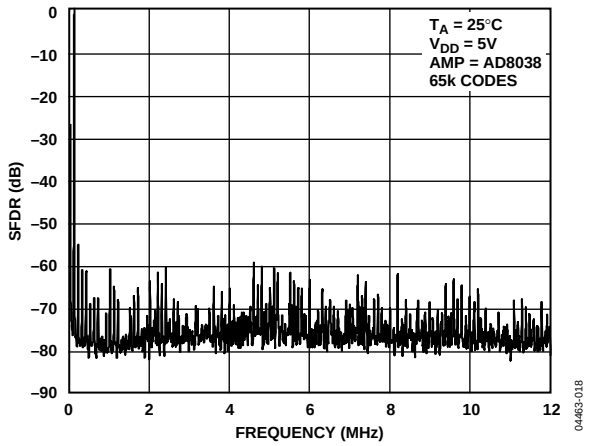


Figure 23. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

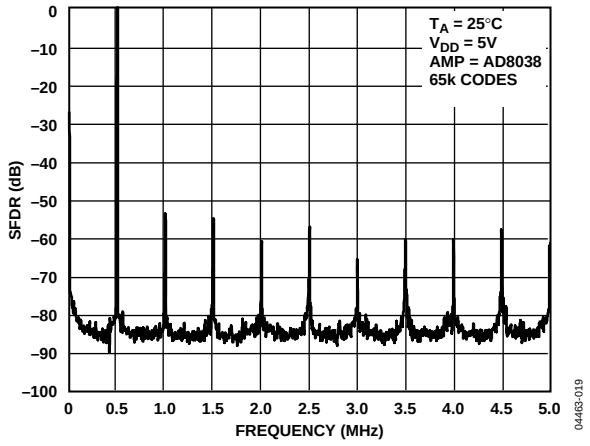


Figure 24. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz

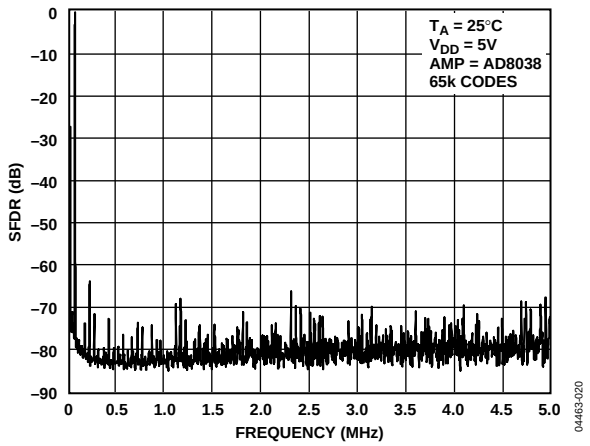


Figure 25. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz

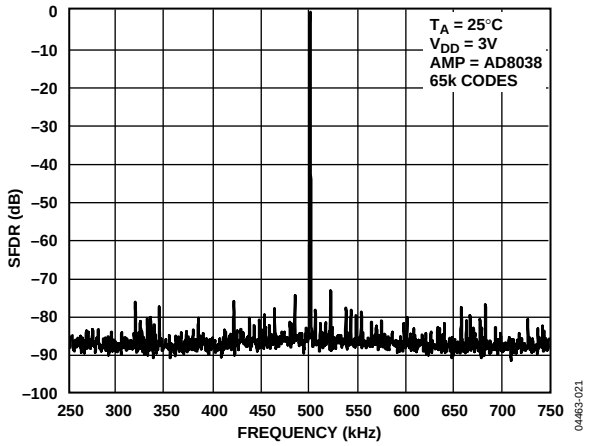


Figure 26. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz

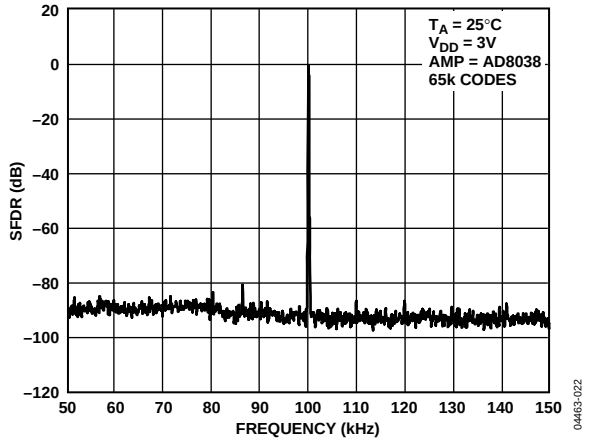


Figure 27. Narrow-Band SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

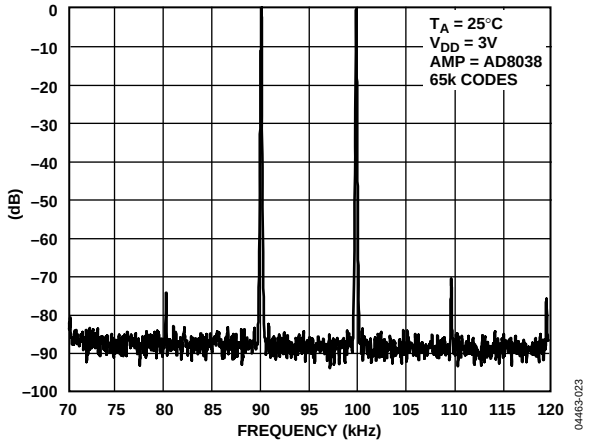


Figure 28. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz

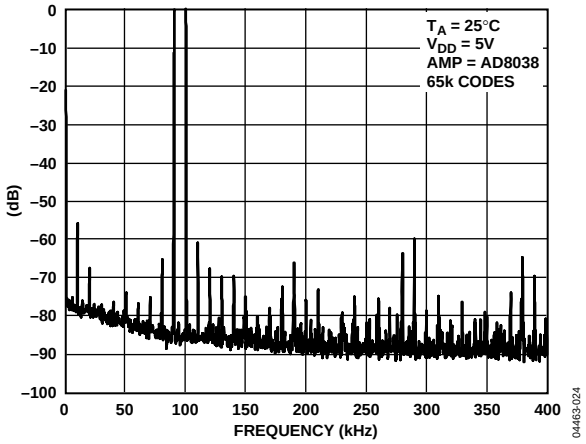


Figure 29. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz

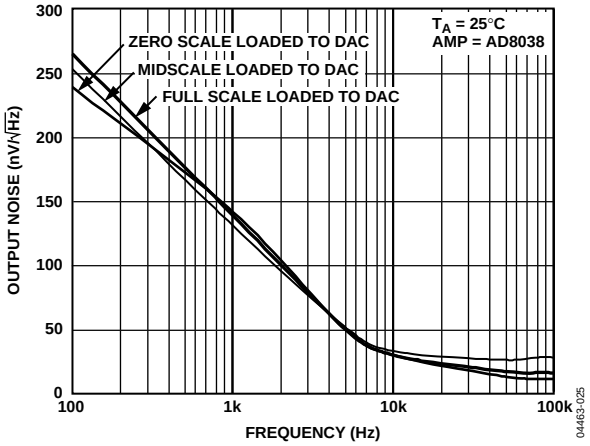


Figure 30. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy (Endpoint Nonlinearity)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of the full-scale reading.

Differential Nonlinearity
The difference in the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of −1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error (Full-Scale Error)
A measure of the output error between an ideal DAC and the actual device output. For this DAC, ideal maximum output is V_{REF} − 1 LSB. The gain error of the DAC is adjustable to zero with an external resistance.

Output Leakage Current
The current that flows into the DAC ladder switches when they are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows into the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
The amount of time for the output to settle to a specified level for a full-scale input change. For this device, it is specified with a 100 Ω resistor to ground.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is typically specified as the area of the glitch in either pA-sec or nV-sec, depending on whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs is capacitively coupled through the device and produces noise on the I_{OUT} pins and, subsequently, on the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
The error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal when all 0s are loaded to the DAC.

Digital Crosstalk
The glitch impulse transferred to the outputs of a DAC in response to a full-scale code change (all 0s to all 1s, or vice versa) in the input register of another DAC. It is expressed in nV-sec.

Analog Crosstalk
The glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s, or vice versa) while keeping LDAC high and then pulsing LDAC low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-sec.

Channel-to-Channel Isolation
The portion of input signal from a DAC's reference input that appears at the output of the other DAC. It is expressed in decibels.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as the second to the fifth harmonics.

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

Intermodulation Distortion (IMD)
The DAC is driven by two combined sine wave references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 ... Intermodulation terms are those for which m or n is not equal to 0. The second-order terms include (fa + fb) and (fa − fb), and the third-order terms are (2fa + fb), (2fa − fb), (f + 2fa + 2fb), and (fa − 2fb). IMD is defined as

$$IMD = 20 \log \frac{\left(rms\ sum\ of\ the\ sum\ and\ diff\ distortion\ products\right)}{rms\ amplitude\ of\ the\ fundamental}$$

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

GENERAL DESCRIPTION

DAC SECTION

The AD5405 is a 12-bit, dual-channel, current-output DAC consisting of a standard inverting R-2R ladder configuration. Figure 31 shows a simplified diagram for a single channel of the AD5405. The feedback resistor $R_{FB}A$ has a value of 2R. The value of R is typically 10 kΩ (with a minimum of 8 kΩ and a maximum of 13 kΩ). If $I_{OUT}1A$ and $I_{OUT}2A$ are kept at the same potential, a constant current flows into each ladder leg, regardless of digital input code. Therefore, the input resistance presented at $V_{REF}A$ is always constant.

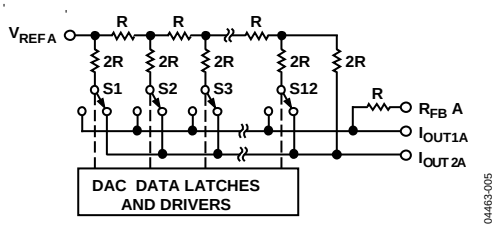


Figure 31. Simplified Ladder Configuration

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of the DAC, making the device extremely versatile and allowing it to be configured for several operating modes, such as unipolar output, bipolar output, or single-supply mode.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, this DAC can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 32.

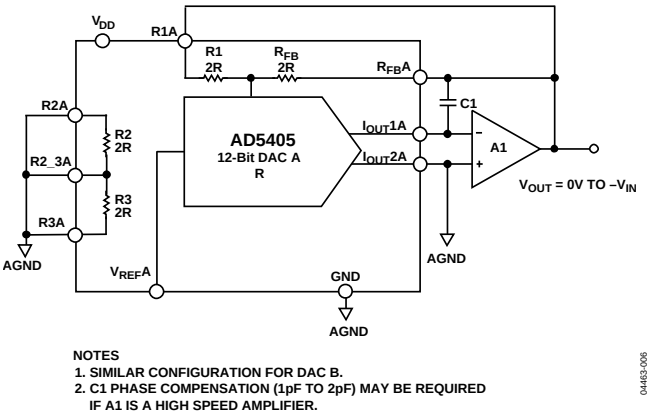


Figure 32. Unipolar Operation

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times D/2^n$$

where:
D is the fractional representation, in the range of 0 to 4,095, of the digital word loaded to the DAC.
n is the resolution of the DAC.

With a fixed 10 V reference, the circuit shown in Figure 32 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between digital code and the expected output voltage for unipolar operation.

Table 5. Unipolar Code

Digital Input	Analog Output (V)
1111 1111 1111	$-V_{REF}$ (4,095/4,096)
1000 0000 0000	$-V_{REF}$ (2,048/4,096) = $-V_{REF}/2$
0000 0000 0001	$-V_{REF}$ (1/4,096)
0000 0000 0000	$-V_{REF}$ (0/4,096) = 0

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier, as shown in Figure 33.

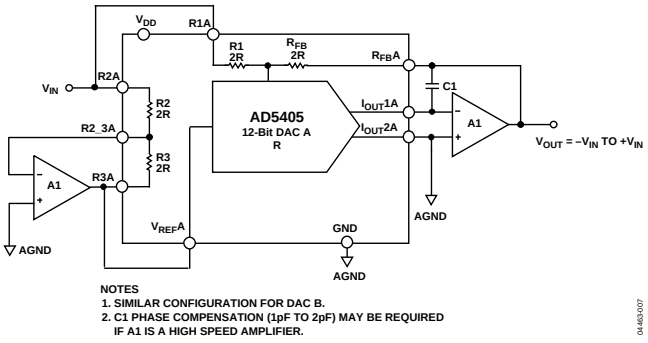


Figure 33. Bipolar Operation (4-Quadrant Multiplication)

When in bipolar mode, the output voltage is given by

$$V_{OUT} = (V_{REF} \times D/2^{n-1}) - V_{REF}$$

where:
D is the fractional representation, in the range of 0 to 4,095, of the digital word loaded to the DAC.
n is the number of bits.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 6 shows the relationship between the digital code and the expected output voltage for bipolar operation.

Table 6. Bipolar Code

Digital Input	Analog Output (V)
1111 1111 1111	$+V_{REF}$ (4,095/4,096)
1000 0000 0000	0
0000 0000 0001	$-V_{REF}$ (4,095/4,096)
0000 0000 0000	$-V_{REF}$ (4,096/4,096)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be used. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in the closed-loop applications circuit.

An optional compensation capacitor, C1, can be added in parallel with $R_{FB}A$ for stability, as shown in Figure 32 and Figure 33. Too small a value of C1 can produce ringing at the output, whereas too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.

SINGLE-SUPPLY APPLICATIONS

Voltage-Switching Mode of Operation

Figure 34 shows the DAC operating in the voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1A$ pin, $I_{OUT}2A$ is connected to AGND, and the output voltage is available at the $V_{REF}A$ terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Therefore, an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. Therefore, the voltage input should be driven from a low impedance source.

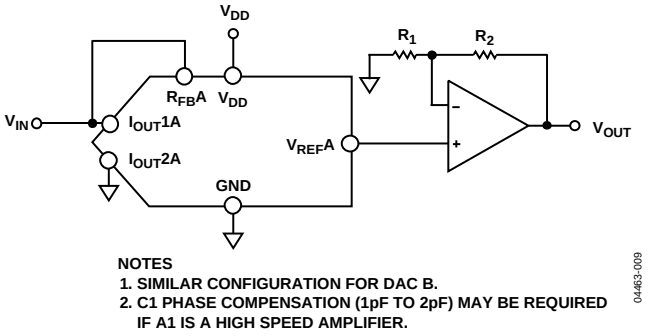


Figure 34. Single-Supply Voltage-Switching Mode

Note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V, or an internal diode turns on, causing the device to exceed the maximum ratings. In this type of application, the full range of multiplying capability of the DAC is lost.

Positive Output Voltage

The output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. To achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor's tolerance errors. To generate a negative reference, the reference can be level-shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and −2.5 V, respectively, as shown in Figure 35.

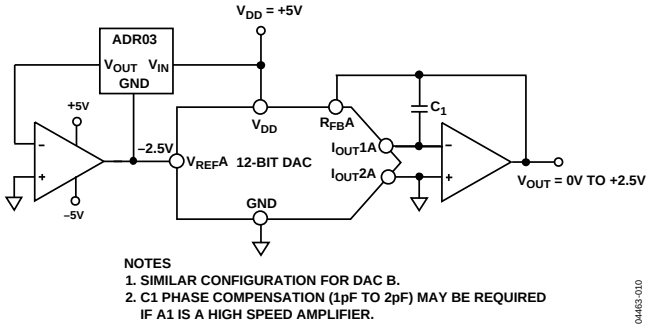


Figure 35. Positive Voltage Output with Minimum Components

ADDING GAIN

In applications where the output voltage must be greater than V_{IN}, gain can be added with an additional external amplifier, or it can be achieved in a single stage. Consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 36 shows the recommended method for increasing the gain of the circuit. R1, R2, and R3 should have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of greater than 1 are required.

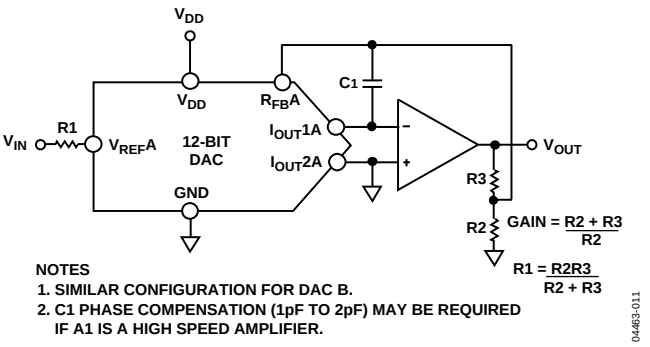


Figure 36. Increasing Gain of Current Output DAC

DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many applications. If this type of DAC is connected as the feedback element of an op amp and $R_{FB}A$ is used as the input resistor, as shown in Figure 37, the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$, the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/\left(1 - 2^{-n}\right)$$

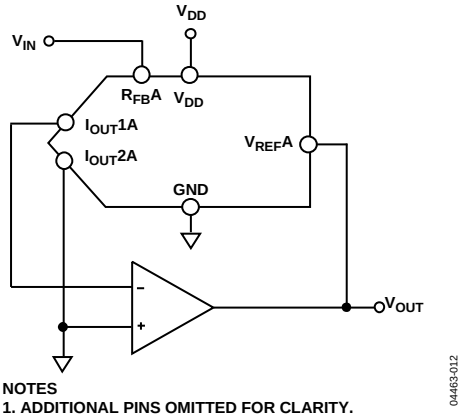


Figure 37. Current-Steering DAC Used as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0x10 (0001 0000)—that is, 16 decimal—in the circuit of Figure 37 should cause the output voltage to be 16 times V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB, D can have a weight in the range of 15.5/256 to 16.5/256 so that the possible output voltage is in the range of 15.5 V_{IN} to 16.5 V_{IN}—an error of 3%, even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction, D, of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage changes as follows:

Output Error Voltage Due to DAC Leakage = (*Leakage* × *R*)/*D*

where *R* is the DAC resistance at the V_{REF} terminal.

For a DAC leakage current of 10 nA, R = 10 kΩ, and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD54xx series of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but also can affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. Choosing a precision reference with low output temperature coefficient minimizes this error source.

Table 7 lists some references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code-dependent output resistance of the DAC, the input offset voltage of an op amp is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB}. Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 12-bit resolution.

Provided that the DAC switches are driven from true wideband, low impedance sources (V_{IN} and AGND), they settle quickly.

Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turn requires an amplifier that can handle rail-to-rail signals. Analog Devices offers a wide range of single-supply amplifiers, as listed in Table 8 and Table 9.

Table 7. Suitable ADI Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 8. Suitable ADI Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 9. Suitable ADI High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/µs)	VOS (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1,500	6,000	SOIC-8, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1,000	10,500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3,000	750	SOIC-8, SC70-5
AD9631	±3 to ±6	320	1,300	10,000	7,000	SOIC-8

PARALLEL INTERFACE

Data is loaded into the AD5405 in a 12-bit parallel word format. Control lines $\overline{CS}$ and R/$\overline{W}$ allow data to be written to or read from the DAC register. A write event takes place when $\overline{CS}$ and R/$\overline{W}$ are brought low, data available on the data lines fills the shift register, and the rising edge of $\overline{CS}$ latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on $\overline{CS}$ to ensure that data is loaded into the DAC register and that its analog equivalent is reflected on the DAC output. A read event takes place when R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Data is loaded from the DAC register, goes back into the input register, and is output onto the data line, where it can be read back to the controller for verification or diagnostic purposes. The input and DAC registers of these devices are not transparent; therefore, a falling and rising edge of $\overline{CS}$ is required to load each data-word.

MICROPROCESSOR INTERFACING

ADSP-21xx-to-AD5405 Interface

Figure 38 shows the AD5405 interfaced to the ADSP-21xx series of DSPs as a memory-mapped device. A single wait state may be necessary to interface the AD5405 to the ADSP-21xx, depending on the clock speed of the DSP. The wait state can be programmed via the data memory wait state control register of the ADSP-21xx (see the ADSP-21xx family's user manual for details).

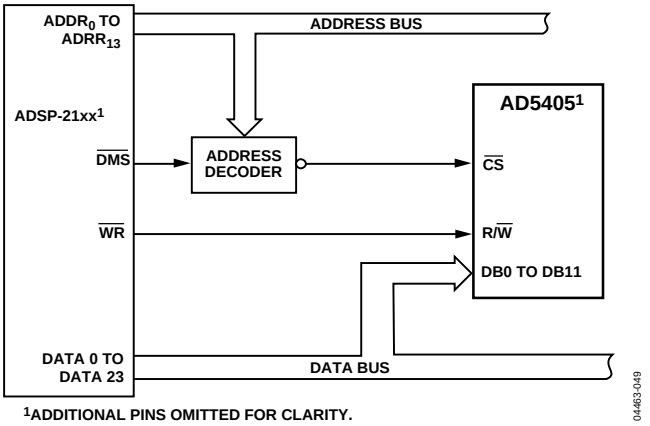


Figure 38. ADSP21xx-to-AD5405 Interface

8xC51-to-AD5405 Interface

Figure 39 shows the interface between the AD5405 and the 8xC51 family of DSPs. To facilitate external data memory access, the address latch enable (ALE) mode is enabled. The low byte of the address is latched with this output pulse during access to the external memory. AD0 to AD7 are the multiplexed low order addresses and data bus; they require strong internal pull-ups when emitting 1s. During access to external memory, A8 to A15 are the high order address bytes. Because these ports are open drained, they also require strong internal pull-ups when emitting 1s.

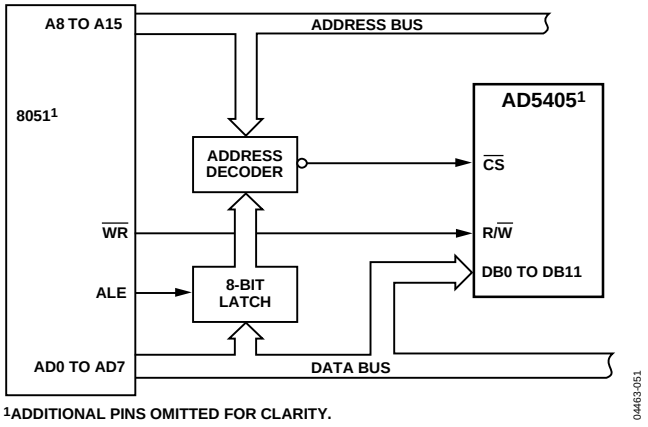


Figure 39. 8xC51-to-AD5405 Interface

ADSP-BF5xx-to-AD5405 Interface

Figure 40 shows a typical interface between the AD5405 and the ADSP-BF5xx family of DSPs. The asynchronous memory write cycle of the processor drives the digital inputs of the DAC. The $\overline{AMS}$x line is actually four memory select lines. Internal ADDR lines are decoded into $\overline{AMS}_{3-0}$; these lines are then inserted as chip selects. The rest of the interface is a standard handshaking operation.

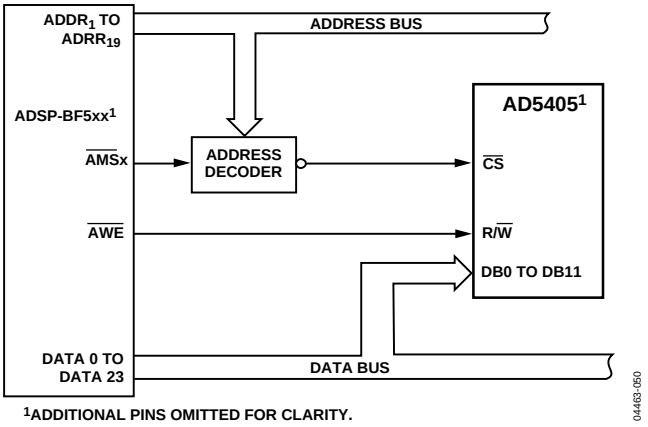


Figure 40. ADSP-BF5xx-to-AD5405 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5405 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close as possible to the package, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), like the common ceramic types of capacitors that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Components, such as clocks, that produce fast-switching signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but its use is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the soldered side.

It is good practice to use compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close as possible to the device.

EVALUATION BOARD FOR THE DACS

The evaluation board consists of a DAC and a current-to-voltage amplifier, the AD8065. Included on the evaluation board is a 10 V reference, the ADR01. An external reference may also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self-installing PC software to control the DAC. The software simply allows the user to write a code to the device.

POWER SUPPLIES FOR THE EVALUATION BOARD

The board requires ±12 V and +5 V supplies. The +12 V V_{DD} and −12 V V_{SS} are used to power the output amplifier; the +5 V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10 μF tantalum and 0.1 μF ceramic capacitors.

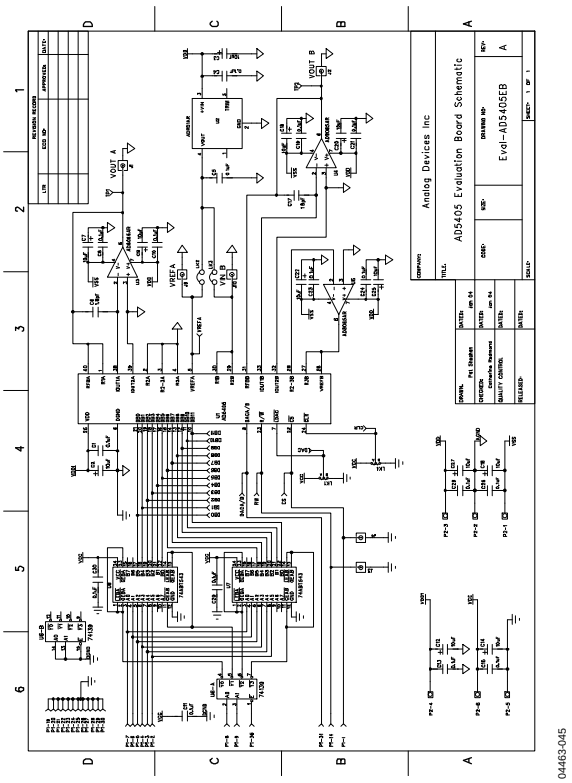


Figure 41. Schematic of AD5405 Evaluation Board

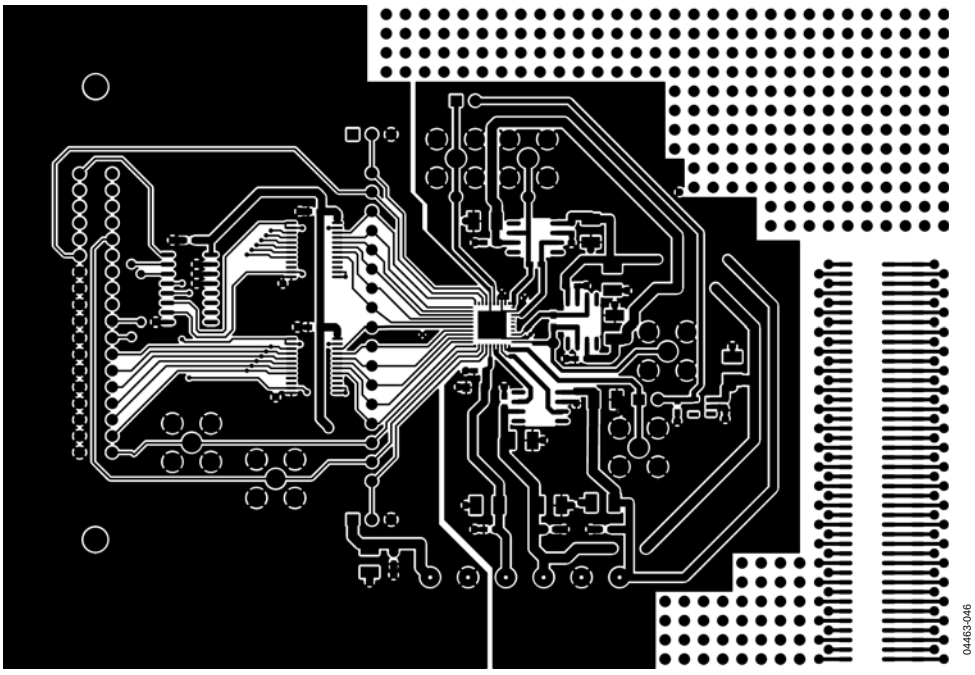


Figure 42. Component-Side Artwork

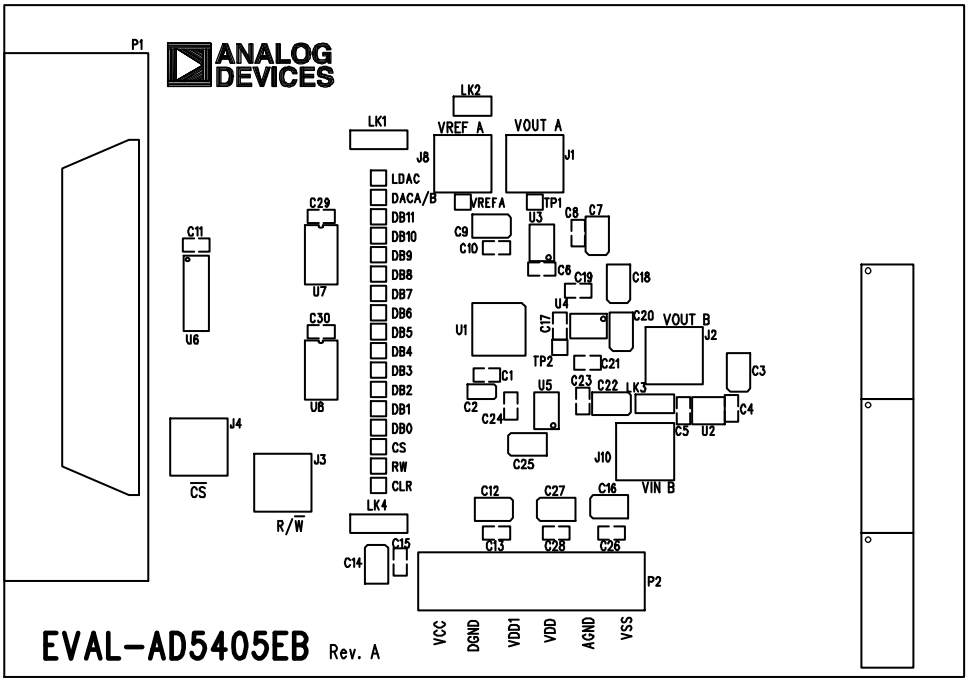


Figure 43. Silkscreen—Component-Side View (Top Layer)

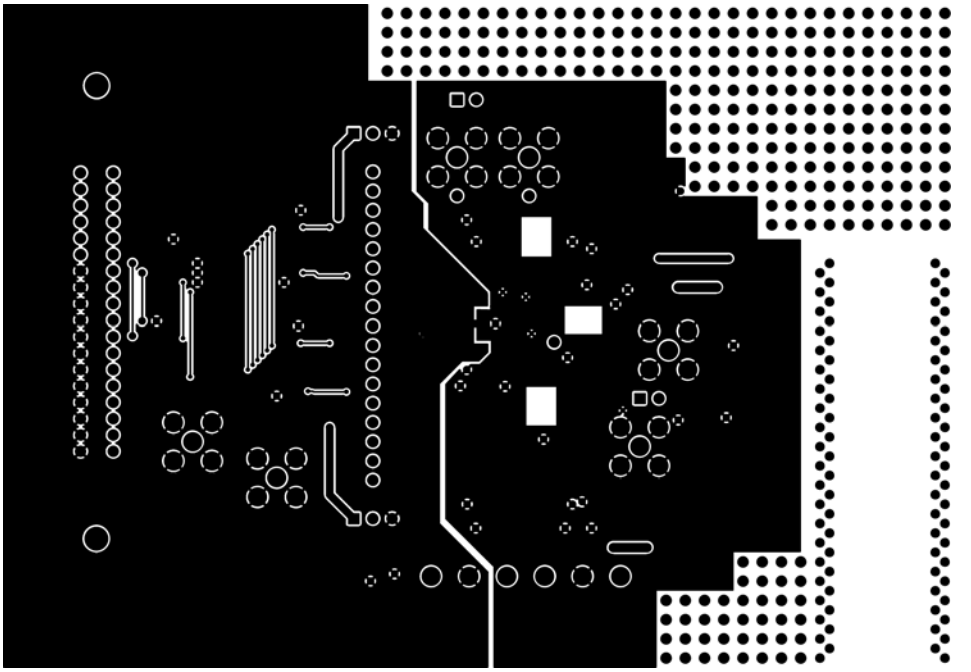


Figure 44. Solder-Side Artwork

OVERVIEW OF AD54xx DEVICES

Table 10.

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package[1]	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	UJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40-1	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

[1] RU = TSSOP, CP = LFCSP, RM = MSOP, UJ = TSOT.

OUTLINE DIMENSIONS

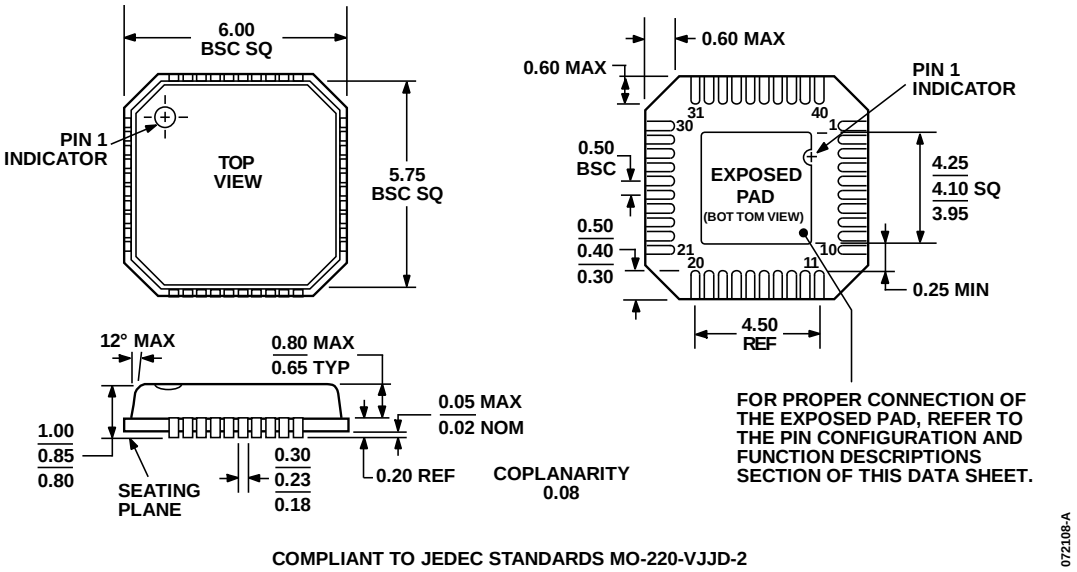


Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	INL (LSB)	Temperature Range	Package Description	Package Option
AD5405YCP	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
AD5405YCP–REEL	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
AD5405YCP–REEL7	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
AD5405YCPZ	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
AD5405YCPZ–REEL	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
AD5405YCPZ–REEL7	12	±1	−40°C to +125°C	40-Lead LFCSP_VQ	CP-40-1
EVAL-AD5405EB				Evaluation Kit	

[1] Z = RoHS Compliant Part.

NOTES

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