SBOS316D − JULY 2005 − REVISED OCTOBER 2008

Dual, Low-Noise Variable-Gain Amplifier with Preamp

FEATURES

- VERY LOW NOISE: 0.7nV/√Hz
- LOW-NOISE PREAMP (LNP)
  - Active Termination
  - Programmable Gains: 3, 12, 18, 22dB
  - Programmable Input Impedance (R_F)
  - Buffered, Differential Outputs for CW Processing
  - Excellent Input Signal Handling Capabilities
- LOW-NOISE VARIABLE-GAIN AMPLIFIER
  - High/Low-Mode (0/+6dB)
  - 52dB Gain Control Range
  - Linear Control Response: 22dB/V
  - Switchable Differential Inputs
  - Adjustable Output Clipping-Level
- BANDWIDTH: 42MHz
- HARMONIC DISTORTION: −55dB
- 5V SINGLE SUPPLY
- LOW-POWER: 154mW/Channel
- POWER-DOWN MODES

APPLICATIONS

- MEDICAL AND INDUSTRIAL ULTRASOUND SYSTEMS
  - Suitable for 10-Bit and 12-Bit Systems
- TEST EQUIPMENT

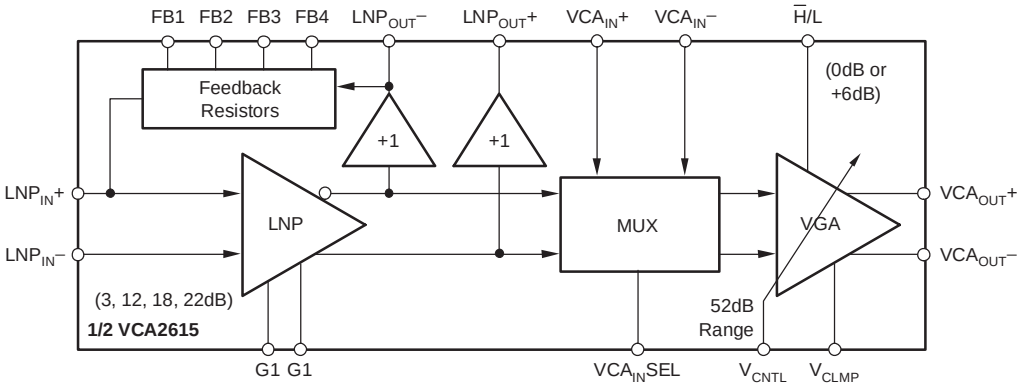
DESCRIPTION

The VCA2615 is a dual-channel, variable gain amplifier consisting of a Low-Noise Preamplifier (LNP) and a Variable-Gain Amplifier (VGA). This combination along with the device features makes it well-suited for a variety of ultrasound systems.

The LNP offers a high level of flexibility to adapt to a wide range of systems and probes. The LNP gain can be programmed to one of four settings (3dB, 12dB, 18dB, 22dB), while maintaining excellent noise and signal handling characteristics. The input impedance of the LNP can be controlled by selecting one of the built-in feedback resistors. This active termination allows the user to closely match the LNP to a given source impedance, resulting in optimized overall system noise performance. The differential LNP outputs are provided either as buffered outputs for further CW processing, or fed directly into the variable-gain amplifier (VGA). Alternatively, an external signal can be applied to the differential VGA inputs through a programmable switch.

Following a linear-in-dB response, the gain of the VGA can be varied over a 52dB range with a 0.2V to 2.5V control voltage common to both channels of the VCA2615. In addition, the overall gain can be switched between a 0dB and +6dB postgain, allowing the user to optimize the output swing of VCA2615 for a variety of high-speed Analog-to-Digital Converters (ADCs). As a means to improve system overload recovery time, the VCA2615 provides an internal clipping function where an externally applied voltage sets the desired clipping level.

The VCA2615 operates on a single +5V supply and is available in a small QFN-48 (7x7mm) or TQFP package.



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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply (V_{DD})	+6V
Analog Inputs	−0.3V to (+V_S + 0.3V)
Logic Inputs	−0.3V to (+V_S + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	−40°C to +150°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may affect device reliability.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

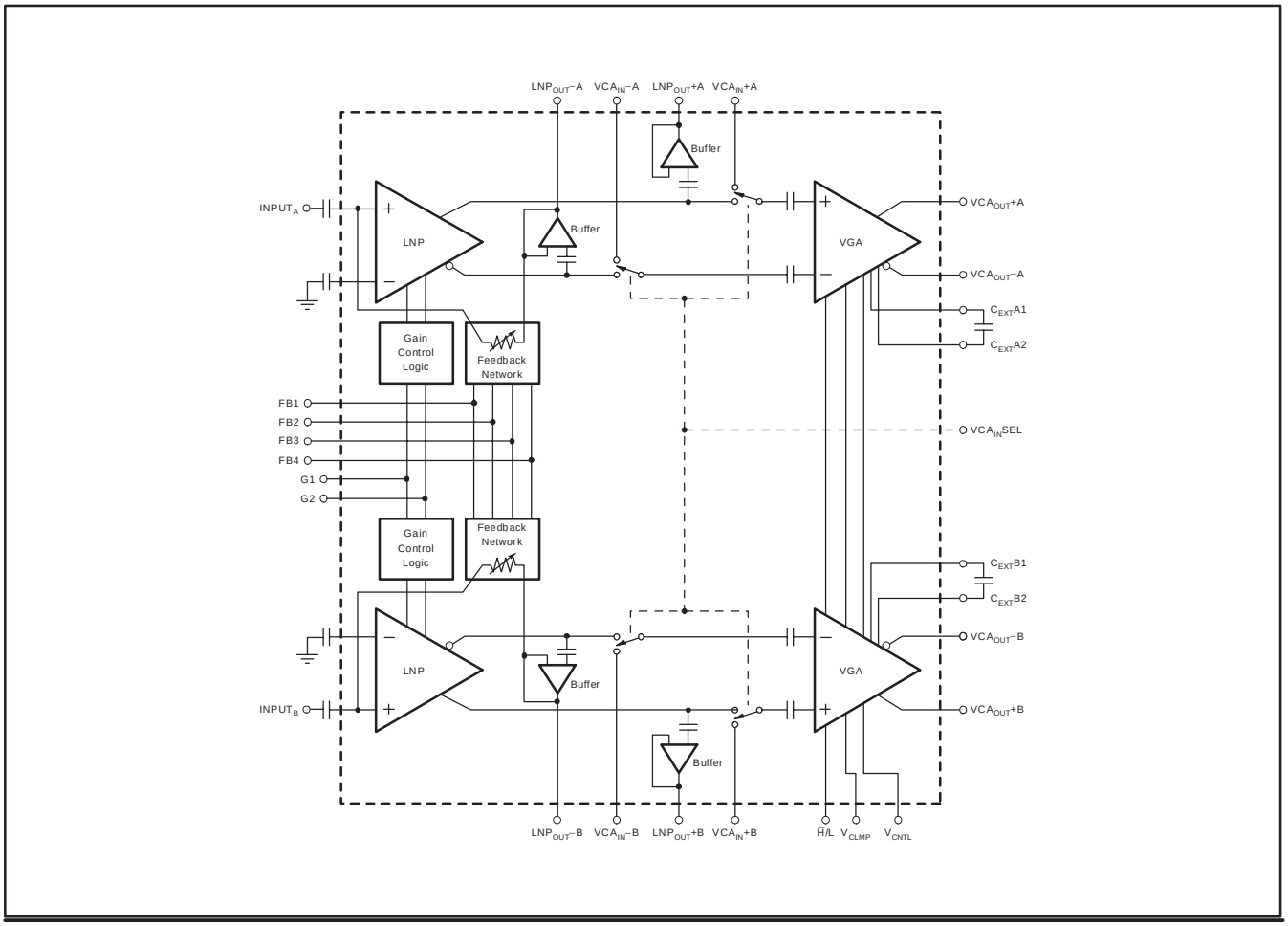
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA2615	QFN-48	RGZ	−40°C to +85°C	VCA2615	VCA2615RGZR	Tape and Reel, 2500
					VCA2615RGZT	Tape and Reel, 250
	TQFP-48	PFB	−40°C to +85°C	VCA2615	VCA2615PFBR	Tape and Reel, 1000
					VCA2615PFBT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, $\overline{H}/L$ = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

PARAMETER	CONDITIONS	VCA2615 MIN	VCA2615 TYP	VCA2615 MAX	UNIT
PREAMPLIFIER (LNP and Buffer)					
Input Resistance, R_{IN}	With Active Feedback Termination		See Note(1)		kΩ
Input Resistance	Feedback Termination Open		100		kΩ
Input Capacitance			45		pF
Maximum Input Voltage	LNP Gain (G1, G2) = 00 − Linear Operation(2)		2.3		V_{PP}
	LNP Gain (G1, G2) = 01 − Linear Operation(2)		0.78		V_{PP}
	LNP Gain (G1, G2) = 10 − Linear Operation(2)		0.39		V_{PP}
	LNP Gain (G1, G2) = 11 − Linear Operation(2)		0.23		V_{PP}
Maximum Input Voltage	Any LNP Gain − Overload (symmetrical clipping)		5		V_{PP}
Input Voltage Noise	R_S = 0Ω; Includes Buffer Noise, LNP Gain = 11		0.8		$nV/\sqrt{Hz}$
Input Current Noise			1		$pA/\sqrt{Hz}$
Bandwidth			50		MHz
2nd-Harmonic Distortion	f_{IN} = 5MHz		−55		dBc
3rd-Harmonic Distortion	f_{IN} = 5MHz		−55		dBc
LNP Gain Change Response Time	LNP Gain 00 to 11; to 90% Signal Level		0.1		µs
BUFFER (LNP_{OUT+}A/B, LNP_{OUT-}A/B)					
Output Signal Range(2)	R_L > = 500Ω		3.3		V_{PP}
Output Common-Mode Voltage			1.85		V
Output Short-Circuit Current			60		mA
Output Impedance			3		Ω
ACTIVE TERMINATION					
Feedback Resistance(3), R_F	FB (1-4) = 0111		1500		Ω
	FB (1-4) = 1011		1000		Ω
	FB (1-4) = 1101		500		Ω
	FB (1-4) = 1110		250		Ω
	FB (1-4) = 0000		130		Ω
VARIABLE-GAIN AMPLIFIER (VGA)					
Peak Input Voltage	Linear Operation(2), V_{CNTL} = 0.7V		2		V_{PP}
Upper −3dB Bandwidth			50		MHz
2nd-Harmonic Distortion	V_{CNTL} = 2.5V, $1V_{PP}$ Differential Output		−60		dBc
3rd-Harmonic Distortion	V_{CNTL} = 2.5V, $1V_{PP}$ Differential Output		−63		dBc
Slew-Rate			±100		V/µs
PREAMPLIFIER AND VARIABLE-GAIN AMPLIFIER (LNP AND VGA)					
Input Voltage Noise			0.7		$nV/\sqrt{Hz}$
Clipping Voltage Range (V_{CLMP})			0.25 to 2.6		V
Clipping Voltage Variation	V_{CLMP} = 0.5V, VCA_{OUT} = $1.0V_{PP}$		±50		mV
Output Impedance	f_{IN} = 5MHz, Single-Ended, Either Output		3		Ω
Output Short-Circuit Current			60		mA
Overload Distortion (2nd-Harmonic)	V_{IN} = $250mV_{PP}$		−44		dBc
Crosstalk	f_{IN} = 5MHz		−70		dBc
Delay Matching			±1		ns
Overload Recovery Time			25		ns
Maximum Output Load			100		Ω
Maximum Capacitive Output Loading	50Ω in Series		80		pF
Maximum Output Signal(2)			6		V_{PP}
Output Common-Mode Voltage			2.5		V
2nd-Harmonic Distortion	Input Signal = 5MHz, V_{CNTL} = 1V	−45	−55		dB
3rd-Harmonic Distortion	Input Signal = 5MHz, V_{CNTL} = 1V	−45	−55		dB
Upper −3dB Bandwidth	V_{CNTL} = 2.5V		42		MHz

(1)

$$R_{IN} = \frac{R_F}{(1 + \frac{A_{LNP}}{2})}$$

(2) 2nd−harmonic, 3rd-harmonic distortion less than or equal to −30dBc.
(3) See Table 5.
(4) Referred to best-fit dB linear curve.
(5) Parameters ensured by design; not production tested.
(6) Do not leave inputs floating; no internal pull-up/pull-down resistors.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, $\overline{H}$/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

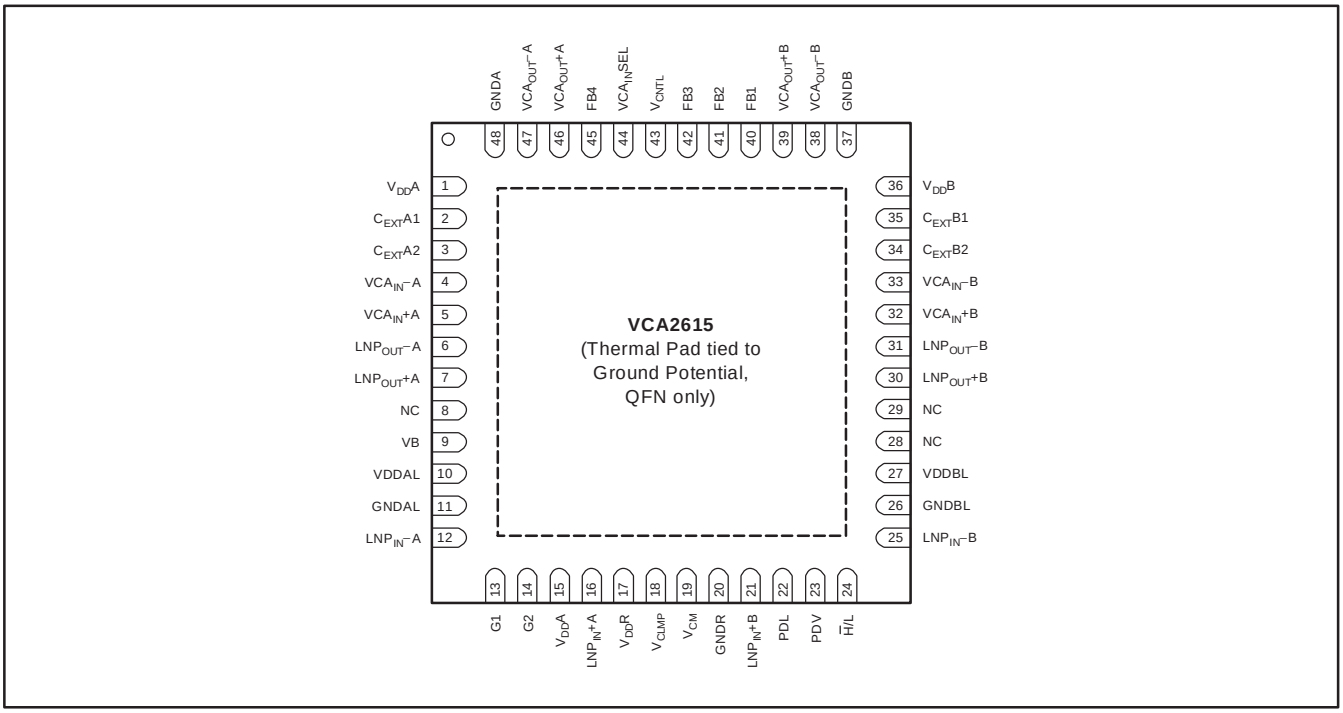
PARAMETER	CONDITIONS	VCA2615 MIN	VCA2615 TYP	VCA2615 MAX	UNIT
ACCURACY					
Gain Slope	V_{CNTL} = 0.4V to 2.0V		22		dB/V
Gain Error(4)	V_{CNTL} = 0.4V to 2.0V	−1.5	±0.9	+1.5	dB
Gain Range	V_{CNTL} = 0.2V to 2.5V		52		dB
Gain Range	V_{CNTL} = 0.4V to 2.0V		36.5		dB
Gain Range ($\overline{H}$/L)	$\overline{H}$/L = 0 (+6dB); VGA High Gain; V_{CNTL} = 0.2V to 2.5V		−12 to +40		dB
	$\overline{H}$/L = 1 (0dB); VGA Low Gain; V_{CNTL} = 0.2V to 2.5V		−18 to +34		dB
Output Offset Voltage, Differential			±50		mV
Channel-to-Channel Gain Matching	V_{CNTL} = 0.4V to 2.0V, CHA to CHB		±0.33		dB
GAIN CONTROL INTERFACE (V_{CNTL})					
Input Voltage Range			0.2 to 2.5		V
Input Resistance			1		MΩ
Response Time	V_{CNTL} = 0.2V to 2V; to 90% Signal Level		0.6		µs
DIGITAL INPUTS(5), (6)					
(G1, G2, PDL, PDV, $\overline{H}$/L, FB1-FB4, $VCA_{IN}SEL$)					
V_{IH}, High-Level Input Voltage		2.0			V
V_{IL}, Low-Level Input Voltage				0.8	V
Input Resistance			1		MΩ
Input Capacitance			5		pF
POWER SUPPLY					
Supply Voltage		4.75	5.0	5.25	V
Power-Up Response Time			25		µs
Power-Down Response Time			2		µs
Total Power Dissipation	PDV, PDL = 1		308	350	mW
VGA Power-Down	PDV = 0, PDL = 1		236		mW
LNP Power-Down	PDL = 0, PDV = 1		95		mW
THERMAL CHARACTERISTICS					
Temperature Range	Ambient, Operating	−40		+85	°C
Thermal Resistance, θ_{JA}	QFN−48 Soldered Pad; Four-Layer PCB with Thermal Vias		29.1		°C/W
θ_{JC}			2.2		°C/W
θ_{JA}	TQFP−48		58		°C/W

(1)

$$R_{IN} = \frac{R_F}{(1 + \frac{A_{LNP}}{2})}$$

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(4) Referred to best-fit dB linear curve.
(5) Parameters ensured by design; not production tested.
(6) Do not leave inputs floating; no internal pull-up/pull-down resistors.

PIN CONFIGURATION



PIN CONFIGURATION

PIN	DESIGNATOR	DESCRIPTION	PIN	DESIGNATOR	DESCRIPTION
1	$V_{DD}A$	Channel A + Supply	25	$LNP_{IN}-B$	Channel B LNP Inverting Input
2	$C_{EXT}A1$	External Capacitor	26	GNDBL	GND B Channel LNP
3	$C_{EXT}A2$	External Capacitor	27	VDDBL	VDD B Channel LNP
4	$VCA_{IN}-A$	Channel A VCA Negative Input	28	NC	Do Not Connect
5	$VCA_{IN}+A$	Channel A VCA Positive Input	29	NC	Do Not Connect
6	$LNP_{OUT}-A$	Channel A LNP Negative Output	30	$LNP_{OUT}+B$	Channel B LNP Positive Output
7	$LNP_{OUT}+A$	Channel A LNP Positive Output	31	$LNP_{OUT}-B$	Channel B LNP Negative Output
8	NC	Do Not Connect	32	$VCA_{IN}+B$	Channel B VCA Positive Input
9	VB	0.01µF Bypass	33	$VCA_{IN}-B$	Channel B VCA Negative Input
10	VDDAL	VDD A Channel LNP	34	$C_{EXT}B2$	External Capacitor
11	GNDAL	GND A Channel LNP	35	$C_{EXT}B1$	External Capacitor
12	$LNP_{IN}-A$	Channel A LNP Inverting Input	36	$V_{DD}B$	Channel B + Supply
13	G1	LNP Gain Setting Pin (MSB)	37	GNDB	Channel B Ground
14	G2	LNP Gain Setting Pin (LSB)	38	$VCA_{OUT}-B$	Channel B VCA Negative Output
15	$V_{DD}A$	Supply Pin for Gain Setting	39	$VCA_{OUT}+B$	Channel B VCA Positive Output
16	$LNP_{IN}+A$	Channel A LNP Noninverting Input	40	FB1	Feedback Control Pin
17	$V_{DD}R$	Supply for Internal Reference	41	FB2	Feedback Control Pin
18	V_{CLMP}	VCA Clamp Voltage Setting Pin	42	FB3	Feedback Control Pin
19	V_{CM}	0.1µF Bypass	43	V_{CNTL}	VCA Control Voltage Input
20	GNDR	Ground for Internal Reference	44	$VCA_{IN}SEL$	VCA Input Select, Hi = External
21	$LNP_{IN}+B$	Channel B LNP Noninverting Input	45	FB4	Feedback Control Pin
22	PDL	Power Down LNPs	46	$VCA_{OUT}+A$	Channel A VCA Positive Pin
23	PDV	Power Down VCAs	47	$VCA_{OUT}-A$	Channel A VCA Negative Pin
24	$\overline{H}/L$	VCA High/Low Gain Mode	48	GNDA	Channel A Ground

TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

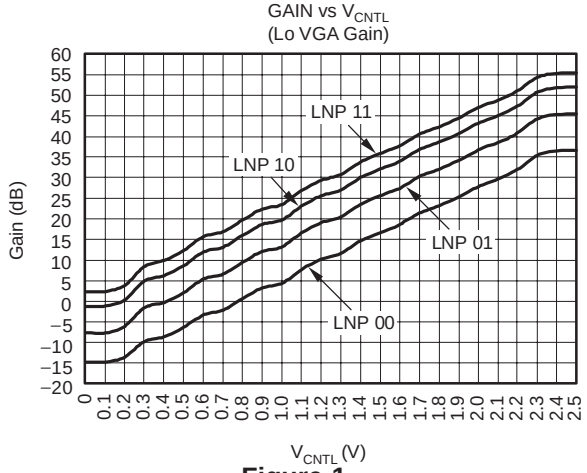


Figure 1

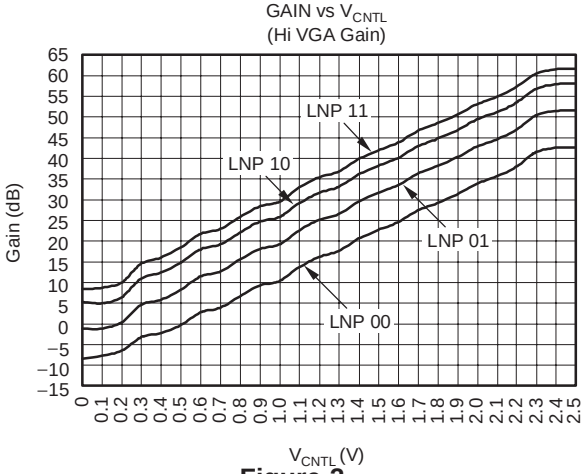


Figure 2

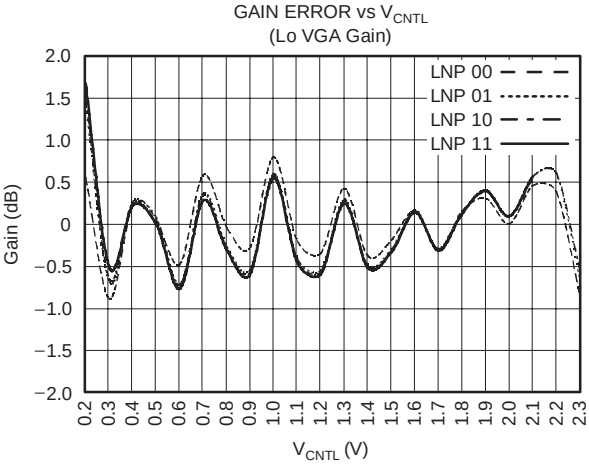


Figure 3

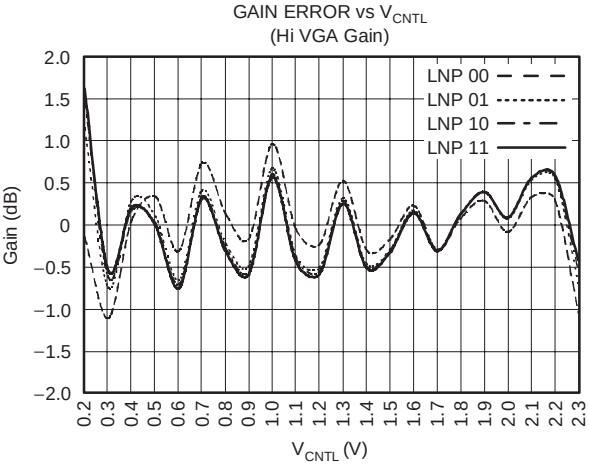


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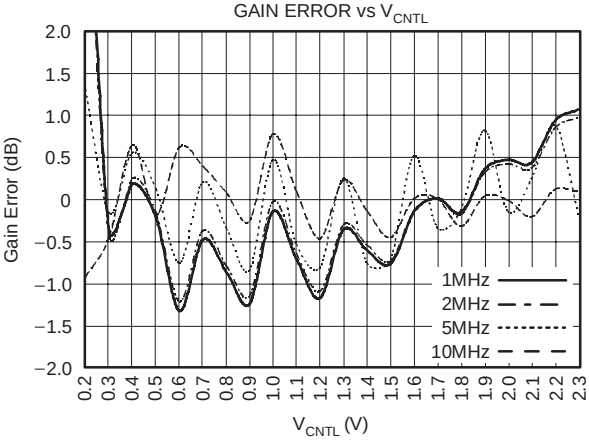


Figure 5

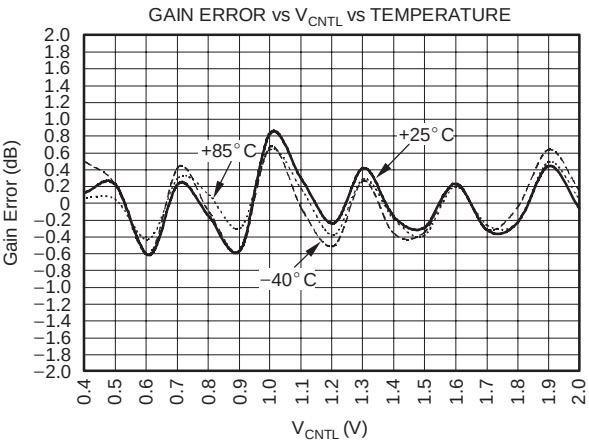


Figure 6

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

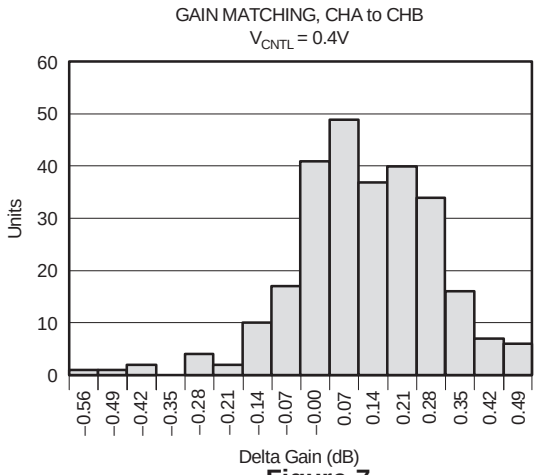


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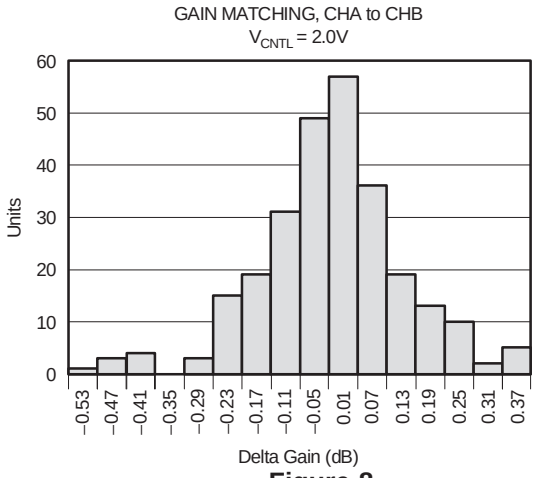


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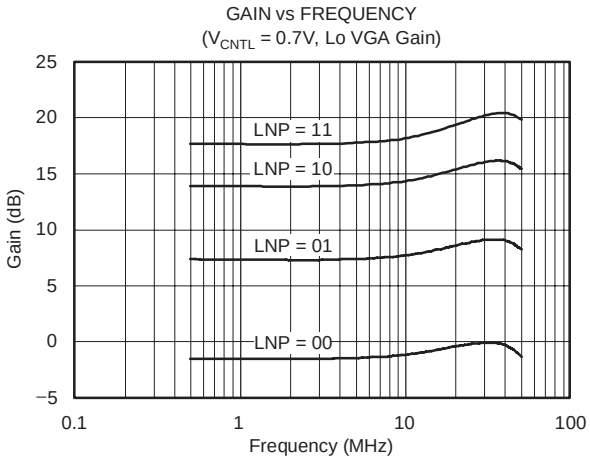


Figure 9

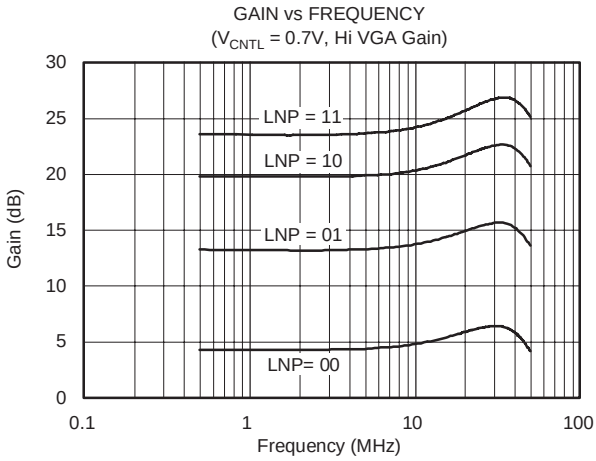


Figure 10

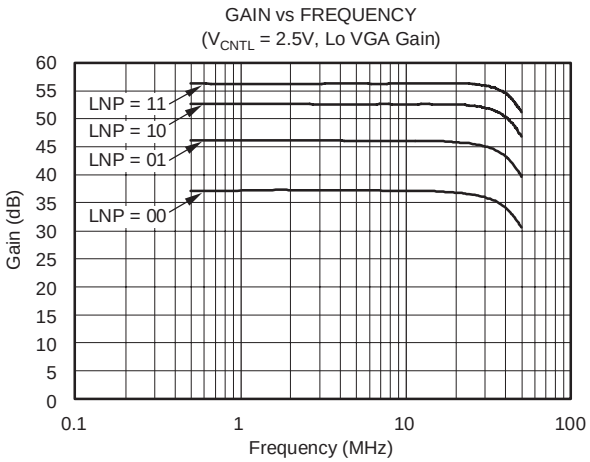


Figure 11

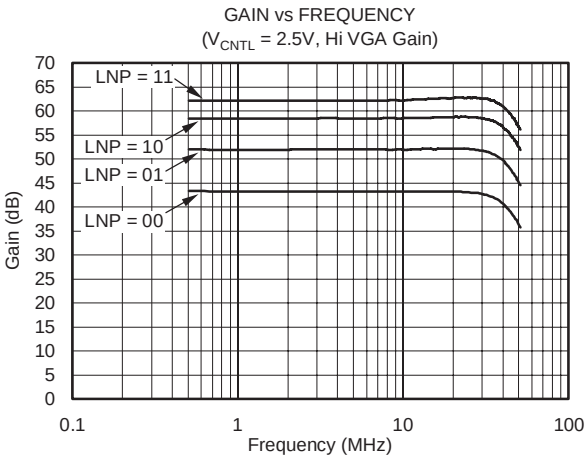


Figure 12

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

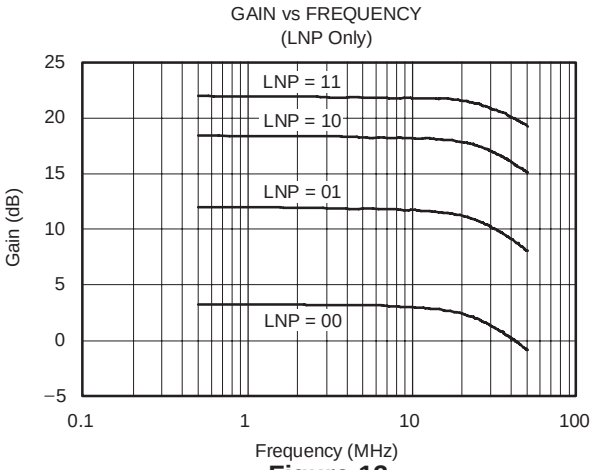


Figure 13

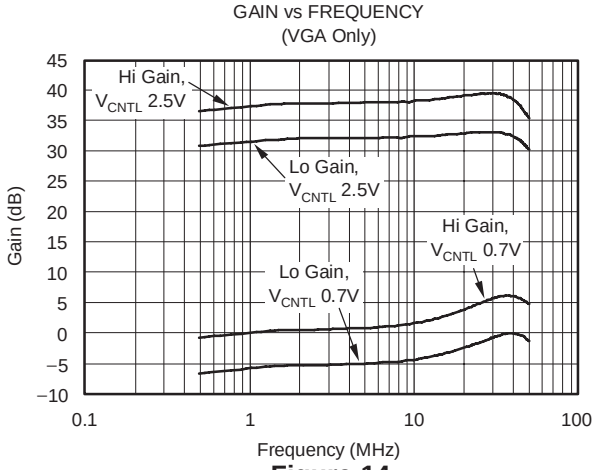


Figure 14

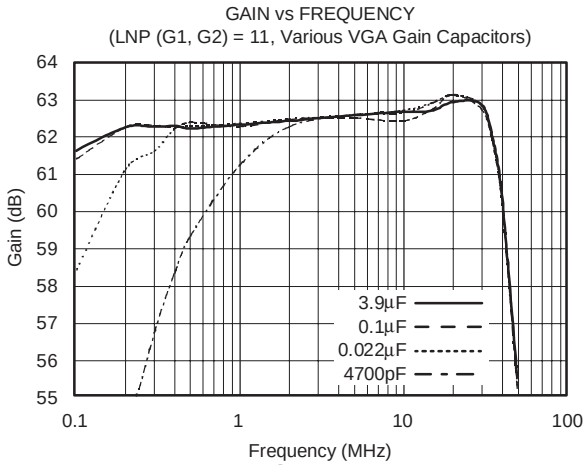


Figure 15

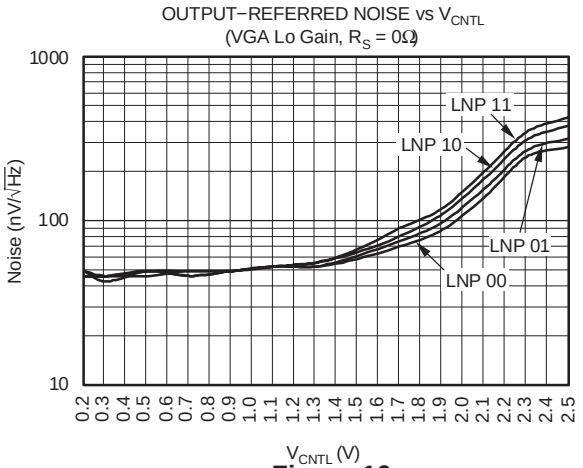


Figure 16

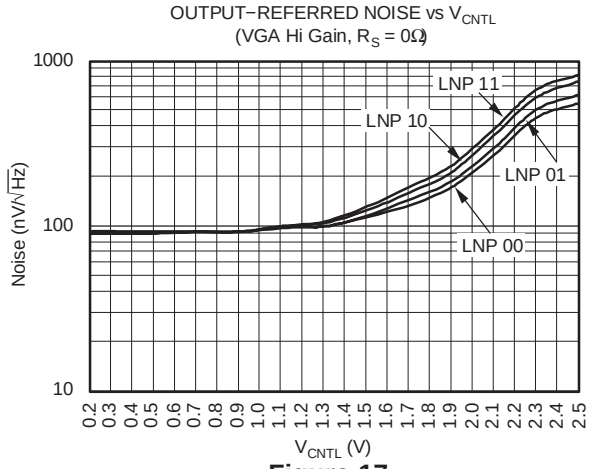


Figure 17

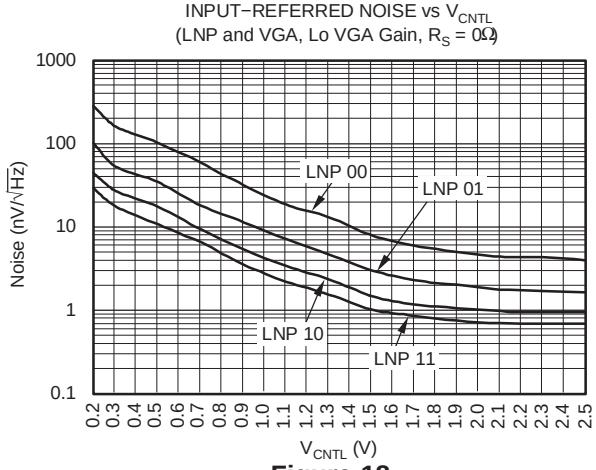


Figure 18

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

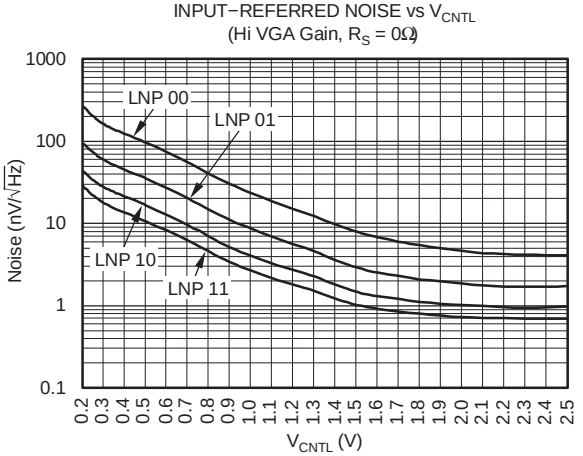


Figure 19

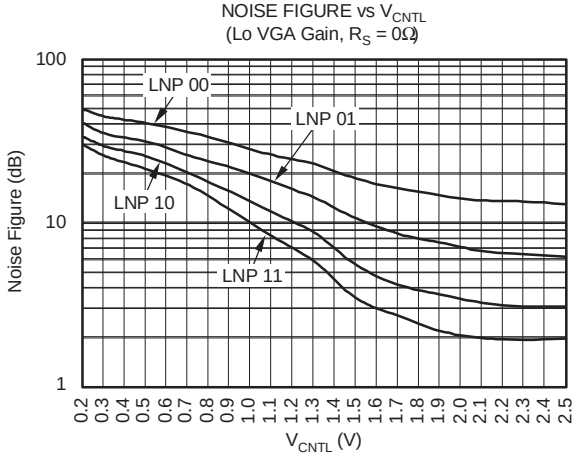


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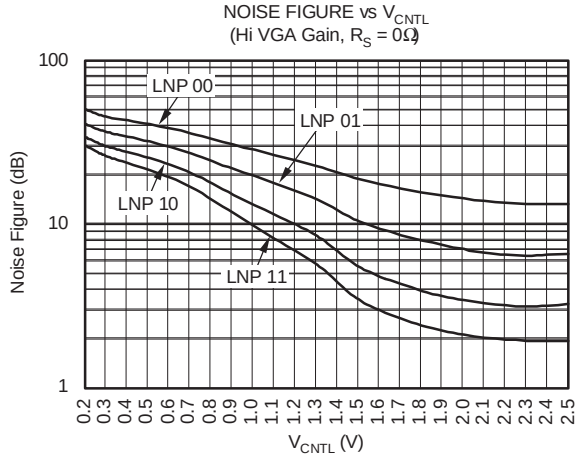


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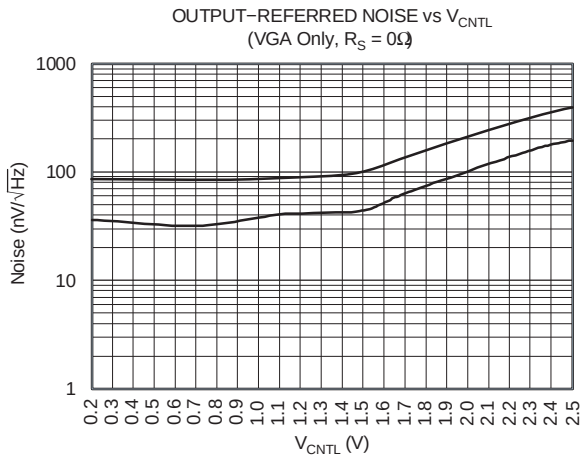


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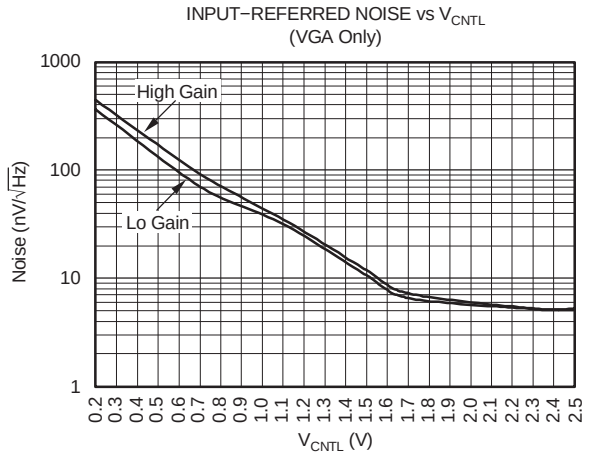


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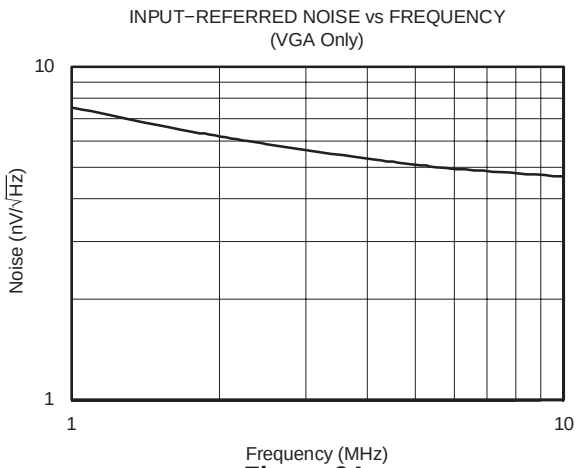


Figure 24

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

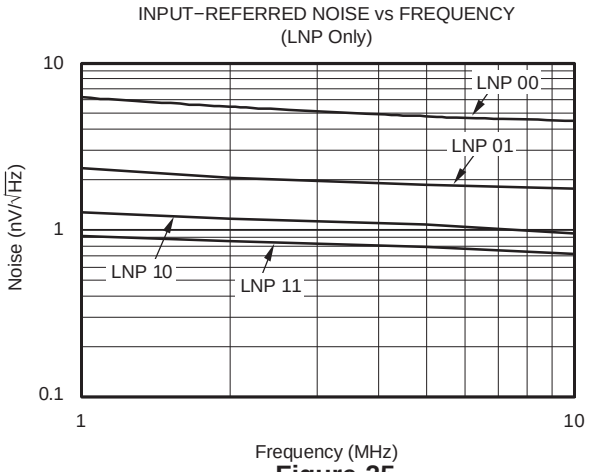


Figure 25

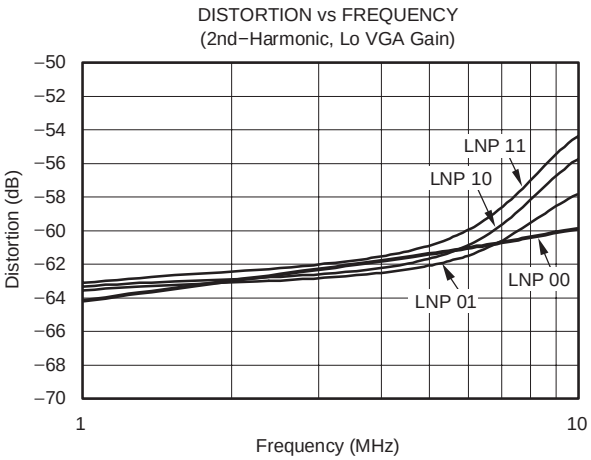


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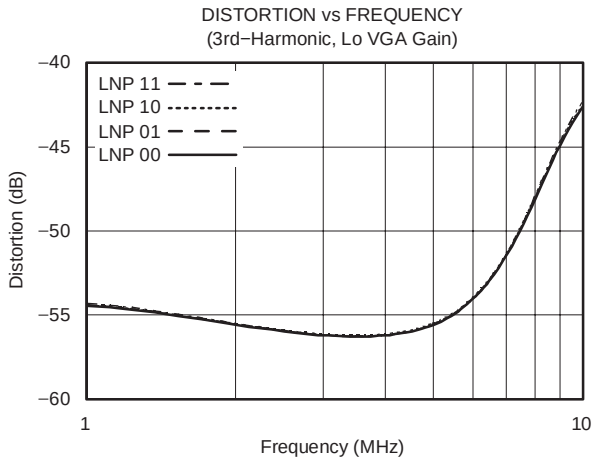


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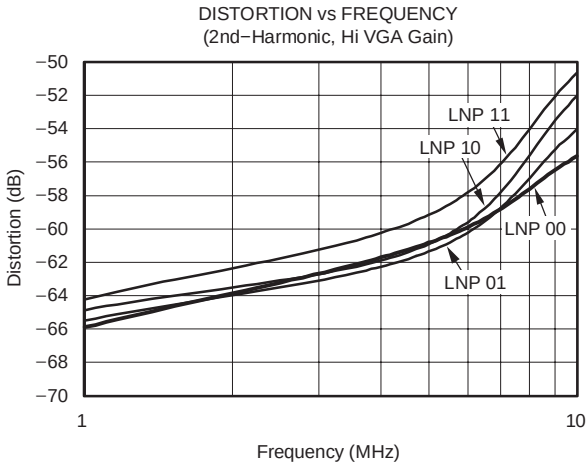


Figure 28

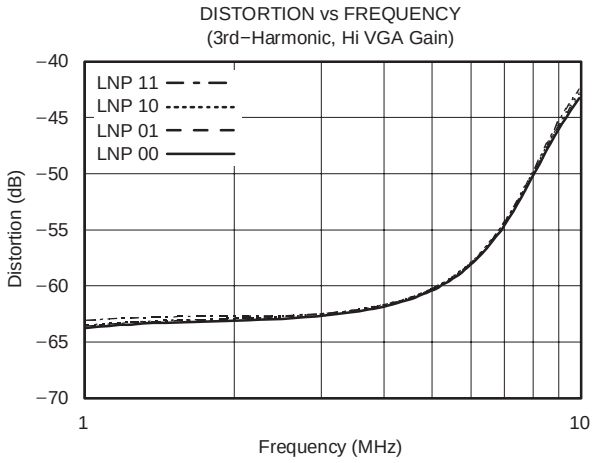


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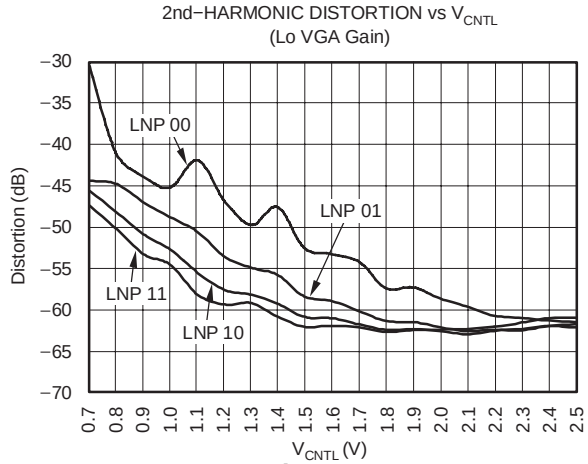


Figure 30

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

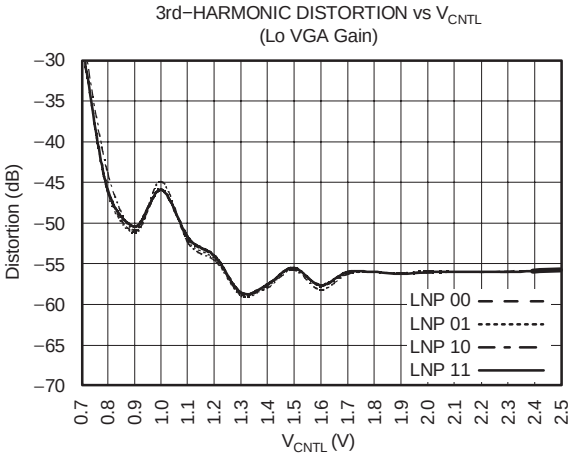


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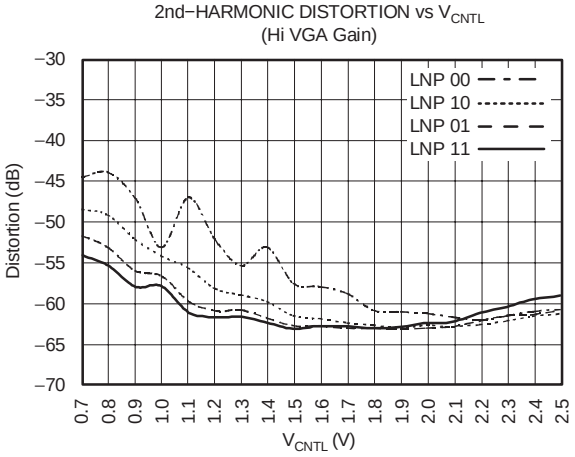


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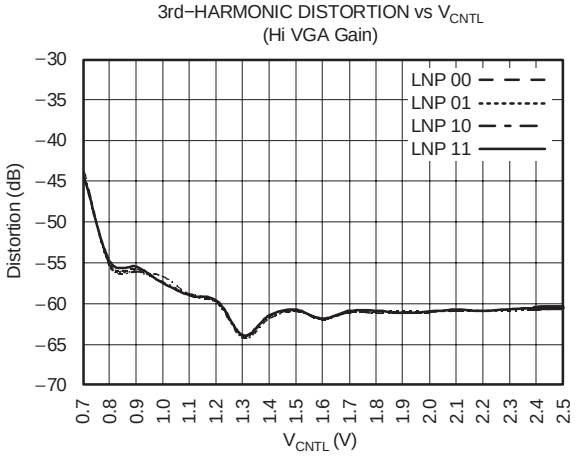


Figure 33

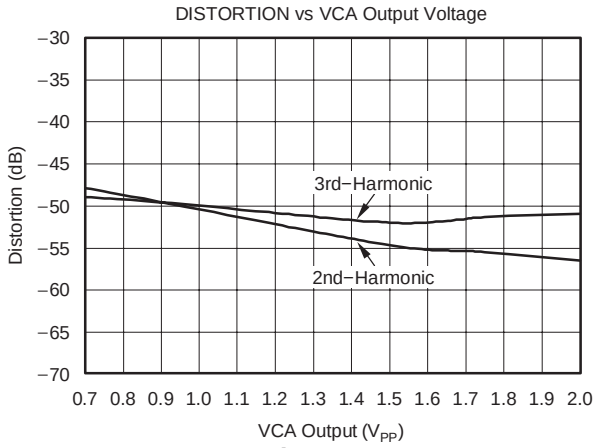


Figure 34

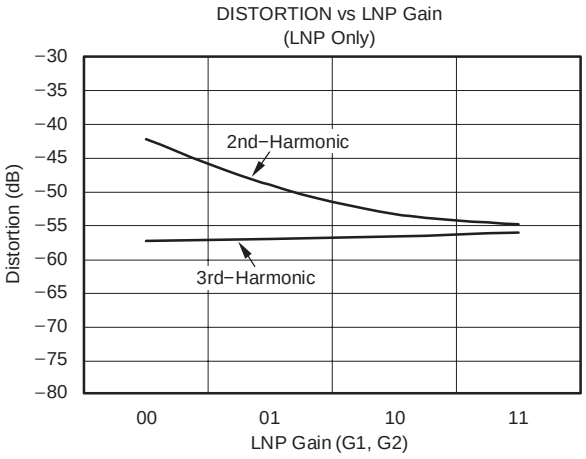


Figure 35

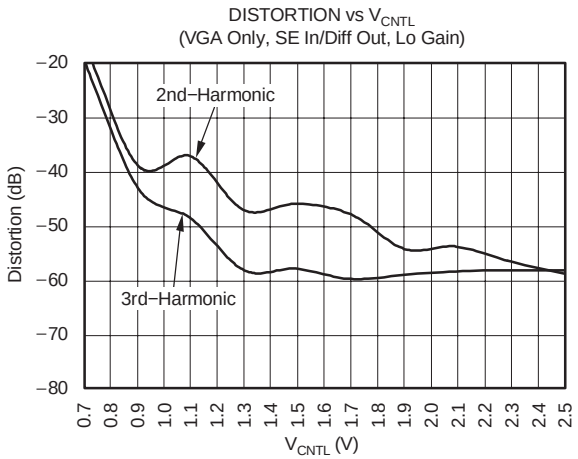


Figure 36

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, H/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

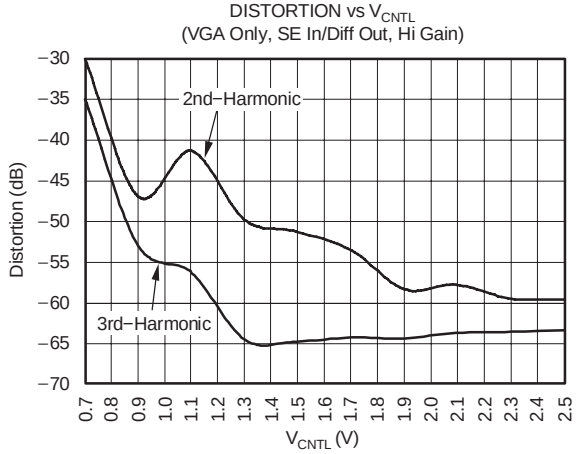


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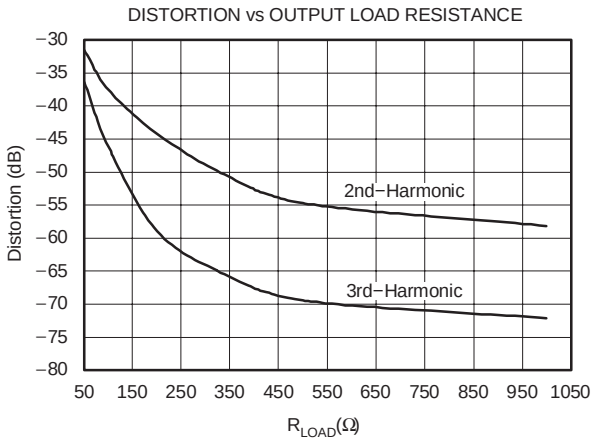


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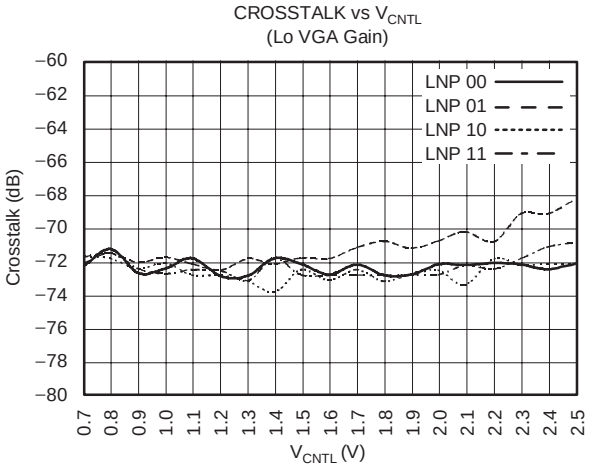


Figure 39

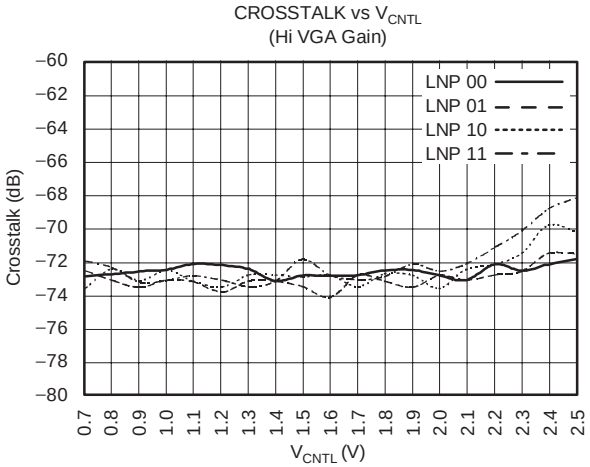


Figure 40

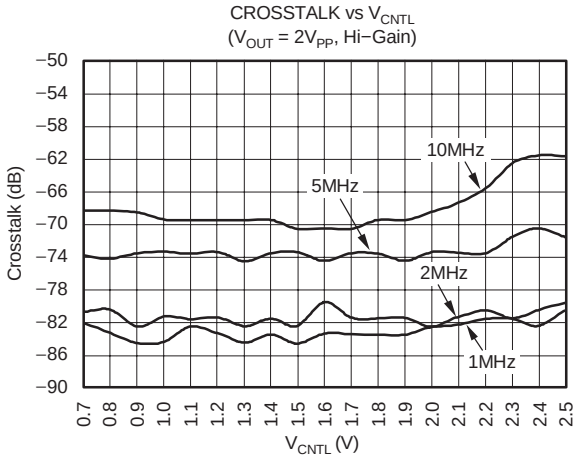


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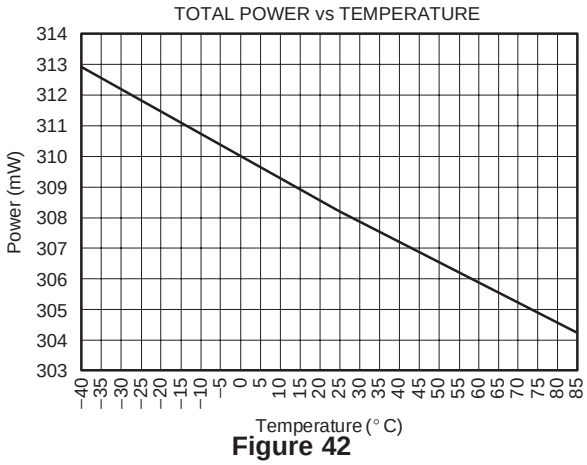


Figure 42

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, $\overline{H}/L$ = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

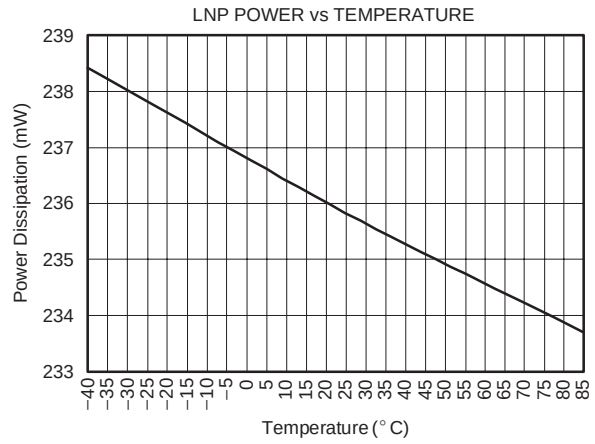


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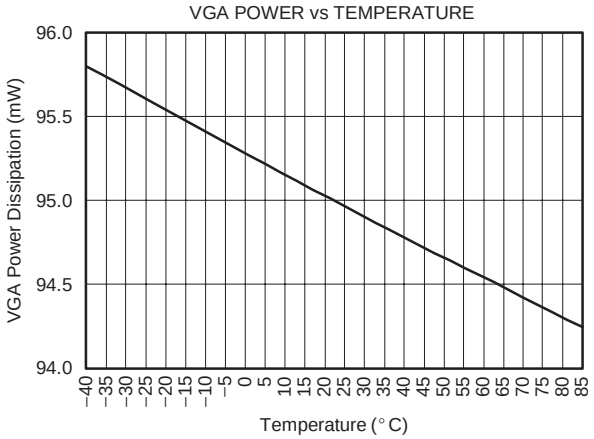


Figure 44

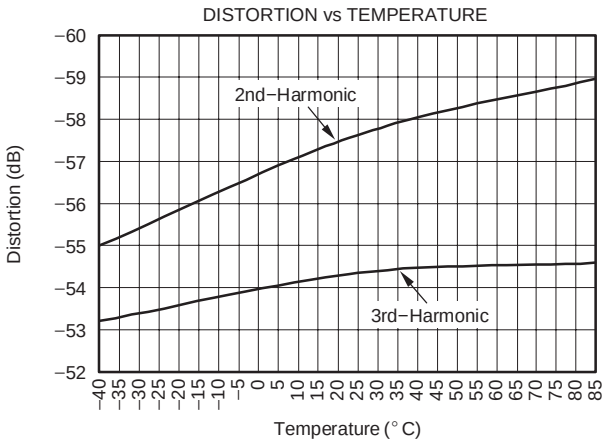


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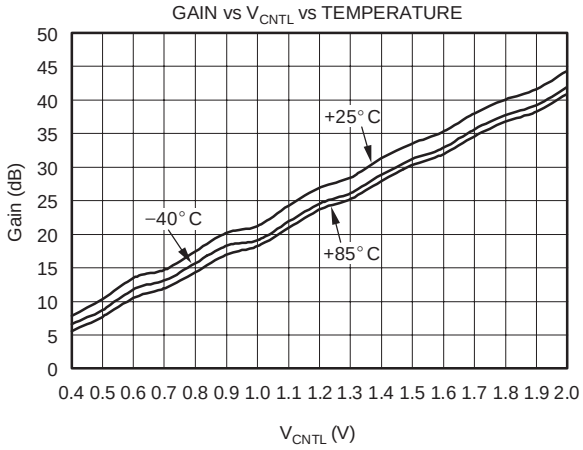


Figure 46

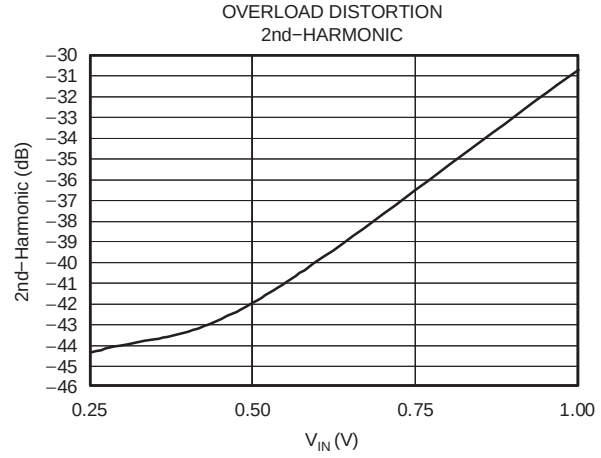


Figure 47

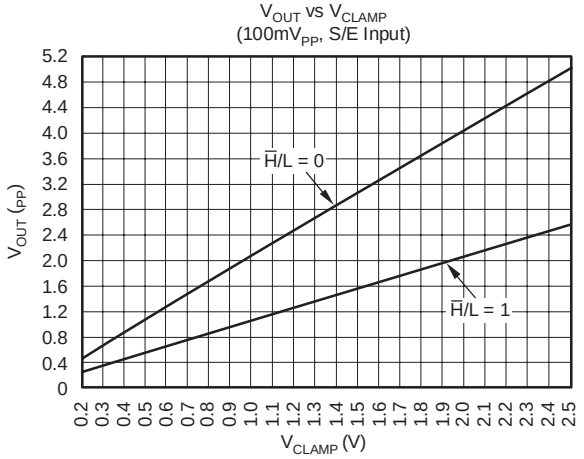


Figure 48

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{DD} = 5V, load resistance = 500Ω on each output to ground; the input to the preamp (LNP) is single-ended; f_{IN} = 5MHz, LNP Gain (G1, G2) = 10, $\overline{H}$/L = 0, V_{CNTL} = 2.5V; VCA output is $1V_{PP}$ differential; CA, CB = 3.9µF, unless otherwise noted.

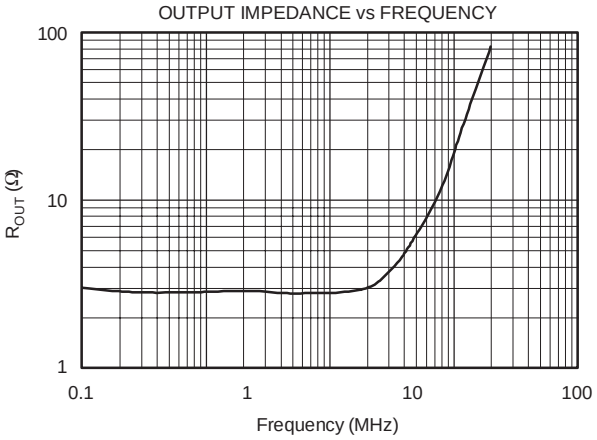


Figure 49

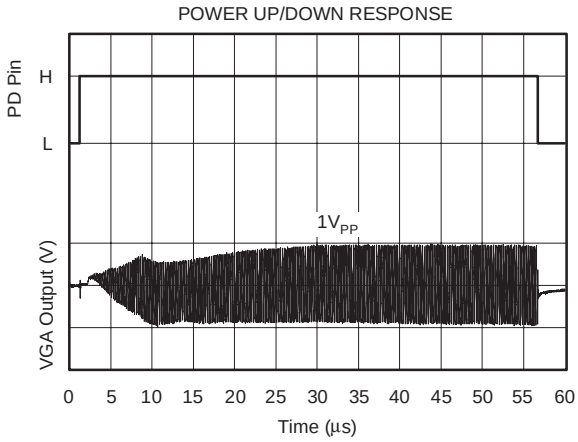


Figure 50

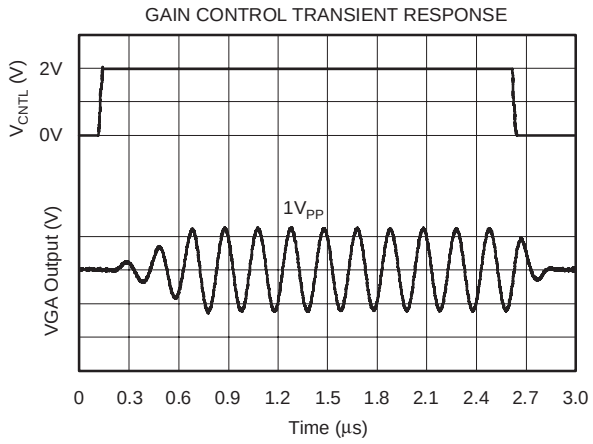


Figure 51

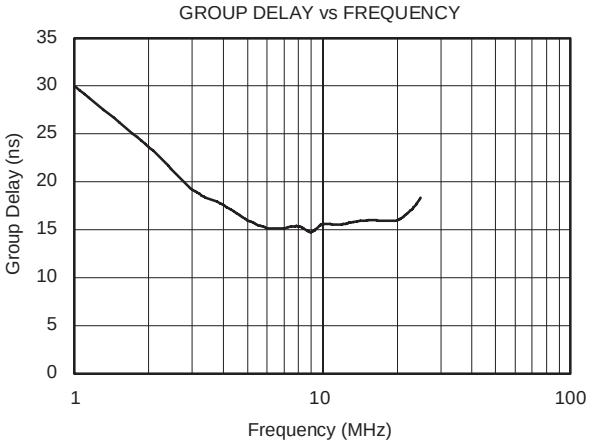


Figure 52

THEORY OF OPERATION

The VCA2615 is a dual-channel system consisting of two primary blocks: a low noise preamplifier (LNP) and a variable gain amplifier (VGA), which is driven from the LNP. The LNP is very flexible; both the gain and input impedance can be programmed digitally without using external components. The LNP is coupled to the VGA through a multiplexer to facilitate interfacing with an external signal processor. The VGA is a true variable-gain amplifier, achieving lower noise output at lower gains. The output amplifier has two gains, allowing for further optimization with different analog-to-digital converters. Figure 53 shows a simplified block diagram of a single channel of the dual-channel system. Both the LNP and the VGA can be powered down together or separately in order to conserve system power when necessary.

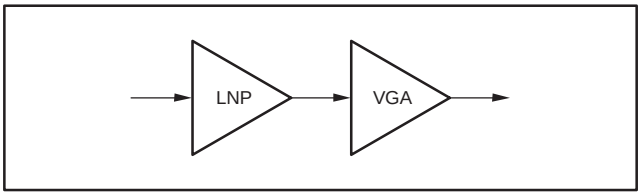


Figure 53. Simplified Block Diagram of VCA2615

LNP—OVERVIEW

The LNP has differential input and output capability. It also has exceptionally low noise voltage and input current noise. At the highest gain setting (of 22dB), the LNP achieves 0.7nV/$\sqrt{Hz}$ voltage noise and typically 1pA/$\sqrt{Hz}$ current noise. The LNP can process fully differential or single-ended signals in each channel. Differential signal processing reduces second harmonic distortion and offers improved rejection of common-mode and power-supply noise. The LNP gain can be electronically programmed to have one of four values that can be selected by a two-bit word (see Table 2). The gain of the LNP when driving the VGA is approximately 1dB higher because of the loss in the buffer.

The LNP also has four programmable feedback resistors that can be selected by a four-bit word to create 16 different values in order to facilitate the easy use of active feedback. With this combination of both programmable gain and feedback resistors, as many as 61 different values of input impedance can be created to provide a wide variety of input-matching resistors (see Table 5). By using active feedback with this wide selection of feedback resistors, the user is able to provide a low-noise means of terminating input signal while incurring only a 3dB loss in signal-to-noise ratio (SNR), instead of a 6dB loss in SNR which is usually associated with the conventional type of signal termination. More information is given in the section of this document that provides a detailed description of the LNP.

The LNP output drives a buffer that in turn drives the feedback network and supplies the LNP to a multiplexer. The multiplexer can be configured to supply the signal off-chip for further processing, or can be set to drive the internal VGA directly from the LNP. An external coupling capacitor is not required to couple the LNP to the VGA.

VGA—OVERVIEW

The VGA that is used with the VCA2615 is a true variable-gain amplifier; as the gain is reduced, the noise contribution from the VGA itself is also reduced. A block diagram of the VGA is shown in Figure 53. This design is in contrast with another popular device architecture (used by the VCA2616), where an effective VCA characteristic is obtained by a voltage variable-attenuator succeeded by a fixed-gain amplifier. At the highest gain, systems with either architecture are dominated by the noise produced by the LNP. At low gains, however, the noise output is dominated by the contribution from the VGA. Therefore, the overall system with lower VGA gain will produce less noise.

The following example will illustrate this point. Figure 53 shows a block diagram of an LNP driving a variable-gain amplifier; Figure 54 shows a block diagram of an LNP driving a variable attenuation attenuator followed by a fixed gain amplifier. For purposes of this example, let us assume the performance characteristics shown in Table 1; these values are the typical performance data of the VCA2615 and the VCA2616.

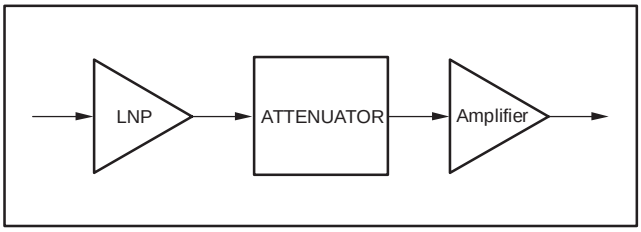


Figure 54. Block Diagram of Older VCA Models

Table 1. Gain and Noise Performance of Various VCA Blocks

BLOCK	GAIN (Loss) dB	NOISE nV/$\sqrt{Hz}$
LNP1 (VCA2615)	20	0.82
LNP2 (VCA2616)	20	1.1
Attenuator (VCA2616)	0	1.8
Attenuator (VCA2616)	−40	1.8
VCA1 (VCA2615)	40	3.8
VCA1 (VCA2615)	0	90
VCA2 (VCA2616)	40	2.0

When the block diagram shown in Figure 53 has a combined gain of 60dB, the noise referred to the input (RTI) is given by the expression:

$$\text{Total Noise (RTI)} = \sqrt{(\text{LNP Noise})^2 + (\text{VCA Noise}/\text{LNP Gain})^2} = \sqrt{(0.82)^2 + (3.8/10)^2} = 0.90\text{nV}/\sqrt{\text{Hz}} \quad (1)$$

When the block diagram shown in Figure 54 has the combined gain of 60dB, the noise referred to the input (RTI) is given by the expression:

$$\text{Total Noise (RTI)} = \sqrt{(\text{LNP Noise})^2 + (\text{ATTEN Noise}/\text{LNP Gain})^2 + (\text{VCA Noise}/\text{LNP Gain})^2} = \sqrt{(1.1)^2 + (1.8/10)^2 + (2.0/10)^2} = 1.13\text{nV}/\sqrt{\text{Hz}} \quad (2)$$

Repeating the above measurements for both VCA configurations when the overall gain is 20dB yields the following results:

For the VCA with a variable gain amplifier (Figure 53):

$$\text{Total Noise (RTI)} = \sqrt{(0.82)^2 + (90/10)^2} = 9.03\text{nV}/\sqrt{\text{Hz}} \quad (3)$$

For the VCA with a variable attenuation attenuator (Figure 54):

$$\text{Total Noise} = \sqrt{(1.1)^2 + (1.8/10)^2 + (2.0/0.10)^2} = 14\text{nV}/\sqrt{\text{Hz}} \quad (4)$$

The VGA has a continuously-variable gain range of 52dB with the ability to select either of two options. The gain of the VGA can either be varied from −12dB to 40dB, or from −18dB to 34dB. The VGA output can be programmed to clip precisely at a predetermined voltage that is selected by the user. When the user applies a voltage to pin 18 (V_{CLMP}), the output will have a peak-to-peak voltage that is given by the graph shown in Figure 48.

LOW NOISE PREAMPLIFIER (LNP)—DETAIL

The LNP is designed to achieve exceptionally low noise performance when employed with or without active feedback. The proprietary LNP architecture can be electronically programmed, eliminating the need for off-board components to alter the gain. A simplified schematic of this amplifier is shown in Figure 55. FET pairs Q1−Q2, Q3−Q4, Q5−Q6 and Q7−Q8 each represent a different LNP gain. The four switches are 22dB, 18dB, 12dB and 3dB. One of the unique gain settings is selected when one of the four switches Q9 through Q12 are selected. Table 2 shows the relationship between the gain selection bits, G1 and G2, and the corresponding gain.

Table 2. Gain Selection of LNP

G1	G2	LNP GAIN (dB)
0	0	3
0	1	12
1	0	18
1	1	22

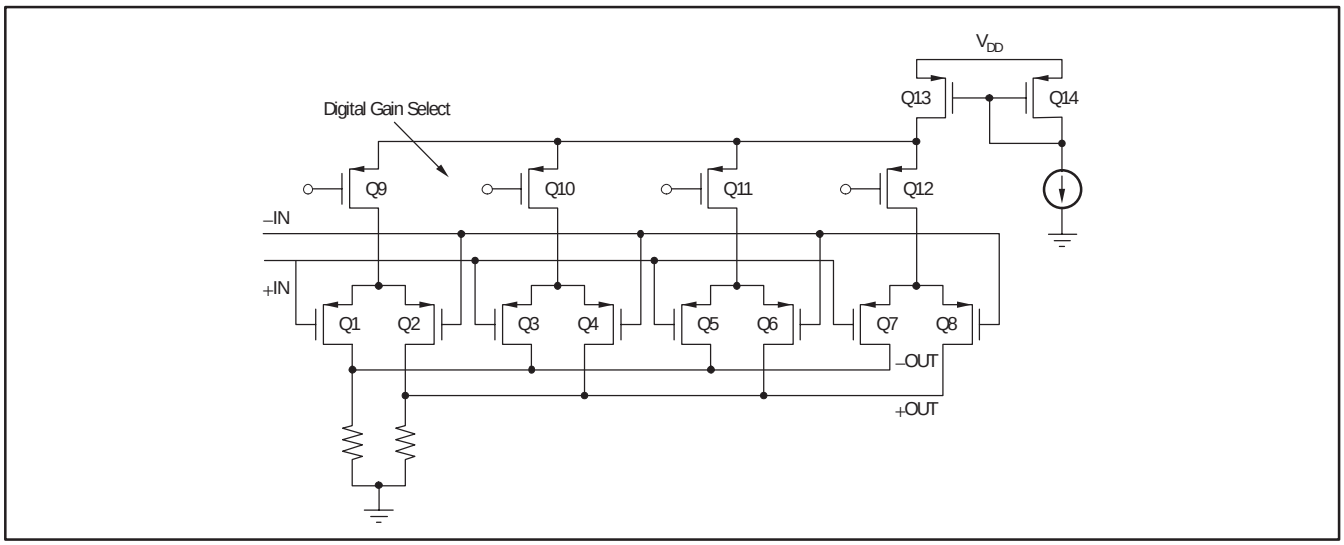


Figure 55. Programmable LNP

The ability to change the gain electronically offers additional flexibility for optimizing the gain in order to achieve either maximum signal-handling capability or maximum sensitivity. Table 3 lists the input and output signal-handling capability of the LNP.

Table 4 shows the voltage noise of the LNP for different gain settings.

Table 3. Signal Handling Capability of LNP

GAIN (dB)	G1, G2	MAX INPUT (V_{PP} Single-Ended)	MAX OUTPUT (V_{PP} Differential)
22	11	0.23	3.5
18	10	0.39	3.5
12	01	0.78	3.5
3	00	2.3	3.0

Table 4. LNP Gain vs Voltage Noise

LNP GAIN (dB)	VOLTAGE NOISE (nV/$\sqrt{Hz}$) at 5MHz
22	0.8
18	1.1
12	1.9
3	4.9

The current noise for the LNP is 1pA/$\sqrt{Hz}$ for all gain settings. The input capacitance of the LNP is 45pF.

The LNP output drives a buffer and a multiplexer (MUX) along with a feedback network that can be used to program the input impedance. Figure 56 shows a block diagram of how these circuits are connected together. The output of the LNP feeds a buffer to avoid the loading effect of the feedback resistors and to achieve a more robust capability for driving external circuits.

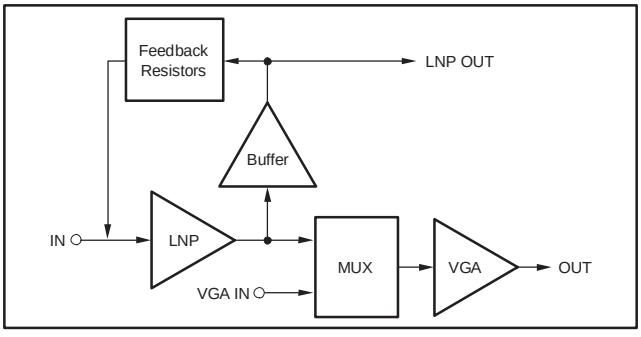


Figure 56. Block Diagram of LNP/VGA Interface

See Figure 57, which shows the response time of the LNP gain changing from minimum to maximum.

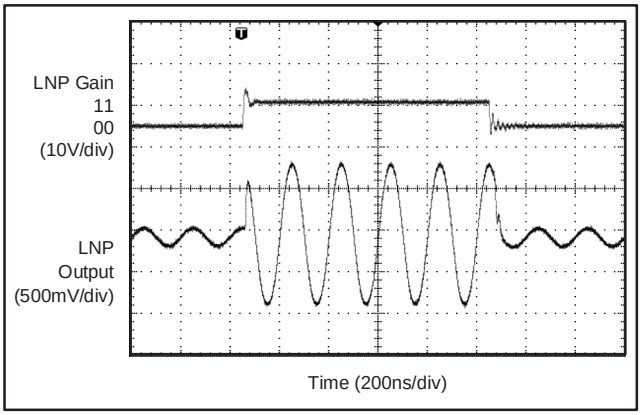


Figure 57. LNP Gain Change Response

The LNP also feeds a MUX, which accepts the LNP signal or can receive an external signal. When applying an external signal to the MUX (VCA_{IN}), the signal should be biased to a common-mode voltage in the range of 1.85V to 3.15V. This biasing could be accomplished by using the 2.5V level of the V_{CM} pin (19) of the VCA2615.

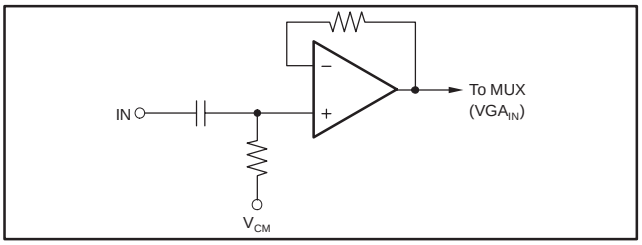


Figure 58. Recommended Circuit for Coupling an External Signal into the MUX

INPUT IMPEDANCE

Figure 59 shows a simplified schematic of the resistor feedback network along with Table 5 that relates the FB1, FB2, FB3 and FB4 code to the selected value. When the selection bits leave the feedback network in the open position, the input resistance of the LNP will become 100kΩ.

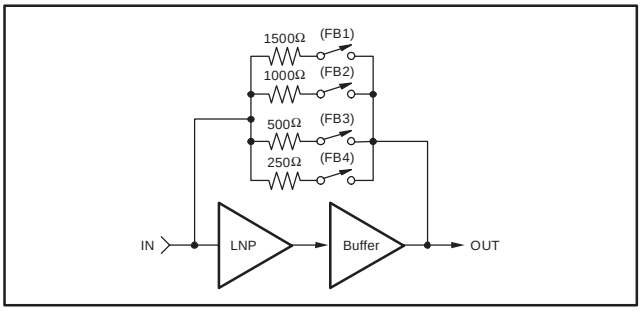


Figure 59. Feedback Resistor Network

Table 5. Feedback Resistor Settings

FEEDBACK RESISTOR (Ω)	FB4	FB3	FB2	FB1
130	0	0	0	0
143	0	0	0	1
150	0	0	1	0
167	0	0	1	1
176	0	1	0	0
200	0	1	0	1
214	0	1	1	0
250	0	1	1	1
273	1	0	0	0
333	1	0	0	1
375	1	0	1	0
500	1	0	1	1
600	1	1	0	0
1000	1	1	0	1
1500	1	1	1	0
Open	1	1	1	1

As explained previously, the LNP gain can have four different values while the feedback resistor can be programmed to have 16 different values. This variable gain means that the input impedance can take on 61 different values given by the formula shown below:

$$R_{IN} = \frac{R_F}{(1 + \frac{A_{LNP}}{2})} \quad (5)$$

Where R_F is the value of the feedback resistor and A_{LNP} is the differential gain of the LNP in volts/volt. The variable gain enables the user to most precisely match the LNP input impedance to the various probe and cable impedances to achieve optimum performance under a variety of conditions. No additional components are required in order to determine the input impedance.

The resistor values shown in Table 5 represent typical values. Due to process variation, the actual values of the resistance can differ by as much as 20%.

ACTIVE FEEDBACK TERMINATION

One of the key features of an LNP architecture is the ability to employ active-feedback termination in order to achieve superior noise performance. Active-feedback termination achieves a lower noise figure than conventional shunt termination essentially because no signal current is wasted in the termination resistor itself. Another example may clarify this point. First, consider that the input source, at the far end of the signal cable, has a cable-matching source resistance of R_S. Using a conventional shunt termination at the LNP input, a second terminating resistor R_S is connected to ground. Therefore, the signal loss is 6dB because of the voltage divider action of the series and shunt R_S resistors. The effective source resistance has been reduced by the same factor of two, but the noise contribution has been reduced only by the $\sqrt{2}$, which is only a 3dB reduction. Therefore, the net theoretical SNR degradation is 3dB, assuming a noise-free amplifier input. In practice, the amplifier noise contribution will degrade both the un-terminated and the terminated noise figures. Figure 60 shows an amplifier using active feedback.

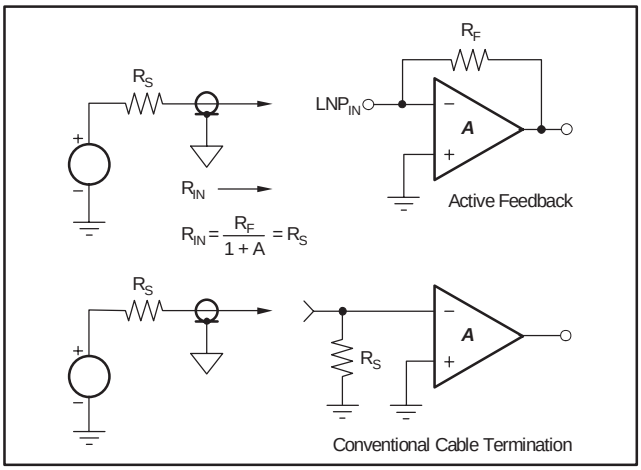


Figure 60. Configurations for Active Feedback and Conventional Cable Termination

This diagram appears very similar to a traditional inverting amplifier. However, ***A*** in this case is not a very large open-loop op-amp gain; rather, it is the relatively low and controlled gain of the LNP itself. Thus, the impedance at the inverting amplifier terminal will be reduced by a finite amount, as given in the familiar relationship of:

$$R_{IN} = \frac{R_F}{(1 + A)} \quad (6)$$

where R_F is the programmable feedback resistor, ***A*** is the user-selected gain of the LNP, and R_{IN} is the resulting amplifier input impedance with active feedback.

In this case, unlike the conventional termination shown in Figure 60, both the signal voltage and the R_S noise are attenuated by the same factor of two (or 6dB) before being re-amplified by the ***A*** gain setting. This configuration avoids the extra 3dB degradation because of the square-root effect described above, which is the key advantage of the active termination technique. As noted, the previous explanation ignored the input noise contribution of the LNP itself. Also, the noise contribution of the feedback resistor must be included for a completely correct analysis. The curves shown in Figure 61 and Figure 62 allow the VCA2615 user to compare the achievable noise figure for active and conventional termination methods.

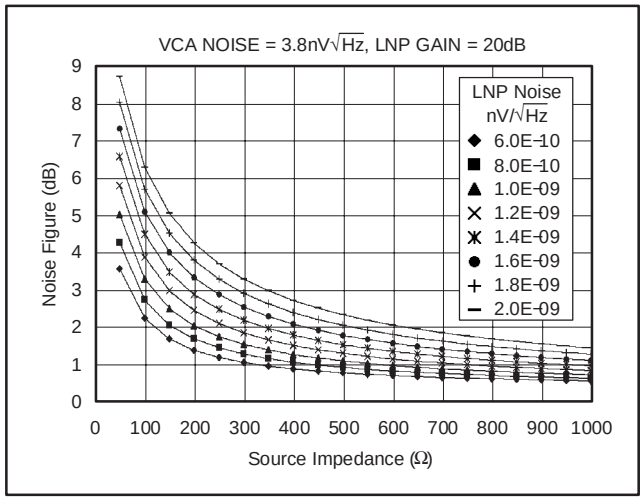


Figure 61. Noise Figure for Active Termination

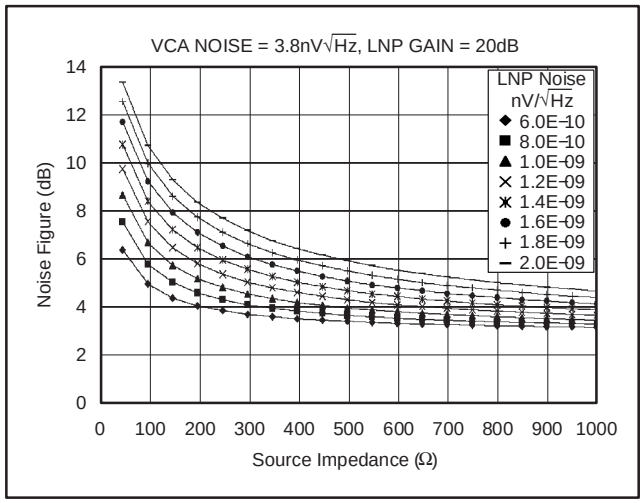


Figure 62. Noise Figure for Conventional Termination

VOLTAGE-CONTROLLED AMPLIFIER (VCA)—DETAIL

Figure 63 shows a simplified schematic of the VCA. The VCA2615 is a true voltage-controlled amplifier, with the gain expressed in dB directly proportional to a control signal. This architecture compares to the older VCA products where a voltage-controlled attenuator was followed by a fixed-gain amplifier. With a variable-gain amplifier, the output noise diminishes as the gain reduces. A variable-gain amplifier, where the output amplifier gain is fixed, will not show diminished noise in this manner. Refer to Table 6, which shows a comparison between the noise performance at different gains for the VCA2615 and the older VCA2616.

Table 6. Noise vs Gain (R_G = 0)

PRODUCT	GAIN (dB)	NOISE RTI (nV/√Hz)
VCA2615	60	0.7
VCA2615	20	9.0
VCA2616	60	1.1
VCA2616	20	14.0

The VCA accepts a differential input at the +IN and −IN terminals. Amplifier A1, along with transistors Q2 and Q3, forms a voltage follower that buffers the +IN signal to be able to drive the voltage-controlled resistor. Amplifier A3, along with transistors Q27 and Q28, plays the same role as A1. The differential signal applied to the voltage-controlled resistor network is converted to a current that flows through transistors Q1 through Q4. Through the mirror action of transistors Q1/Q5 and Q4/Q6, a copy of this same current flows through Q5 and Q6. Assuming that the signal current is less than the programmed clipping current (that is, the current flowing through transistors Q7 and Q8), the signal current will then go through the diode bridge (D1 through D4) and be sent through either R2 or R1, depending upon the state of Q9. This signal current multiplied by the feedback resistor associated with amplifier A2, determines the signal voltage that is designated −OUT. Operation of the circuitry associated with A3 and A4 is identical to the operation of the previously described function to create the signal +OUT.

A1 and its circuitry form a voltage-to-current converter, while A2 and its circuitry form a current-to-voltage converter. This architecture was adapted because it has excellent signal-handling capability. A1 has been designed to handle a large voltage signal without overloading, and the various mirroring devices have also been sized to handle large currents. Good overload capability is achieved as both the input and output amplifier are not required to amplify voltage signals.

Voltage amplification occurs when the input voltage is converted to a current; this current in turn is converted back to a voltage as amplifier A2 acts as a transimpedance amplifier. The overall gain of the output amplifier A2 can be altered by 6dB by the action of the $\overline{H}$/L signal. This enables more optimum performance when the VCA interfaces with either a 10-bit or 12-bit analog-to-digital converter (ADC). An external capacitor (C) is required to provide a low impedance connection to join the two sections of the resistor network. Capacitor C could be replaced by a short-circuit. By providing a DC connection, the output offset will be a function of the gain setting. Typically, the offset at this point is ±10mV; thus, if the gain varies from 1 to 100, the output offset would vary from ±10mV to ±100mV.

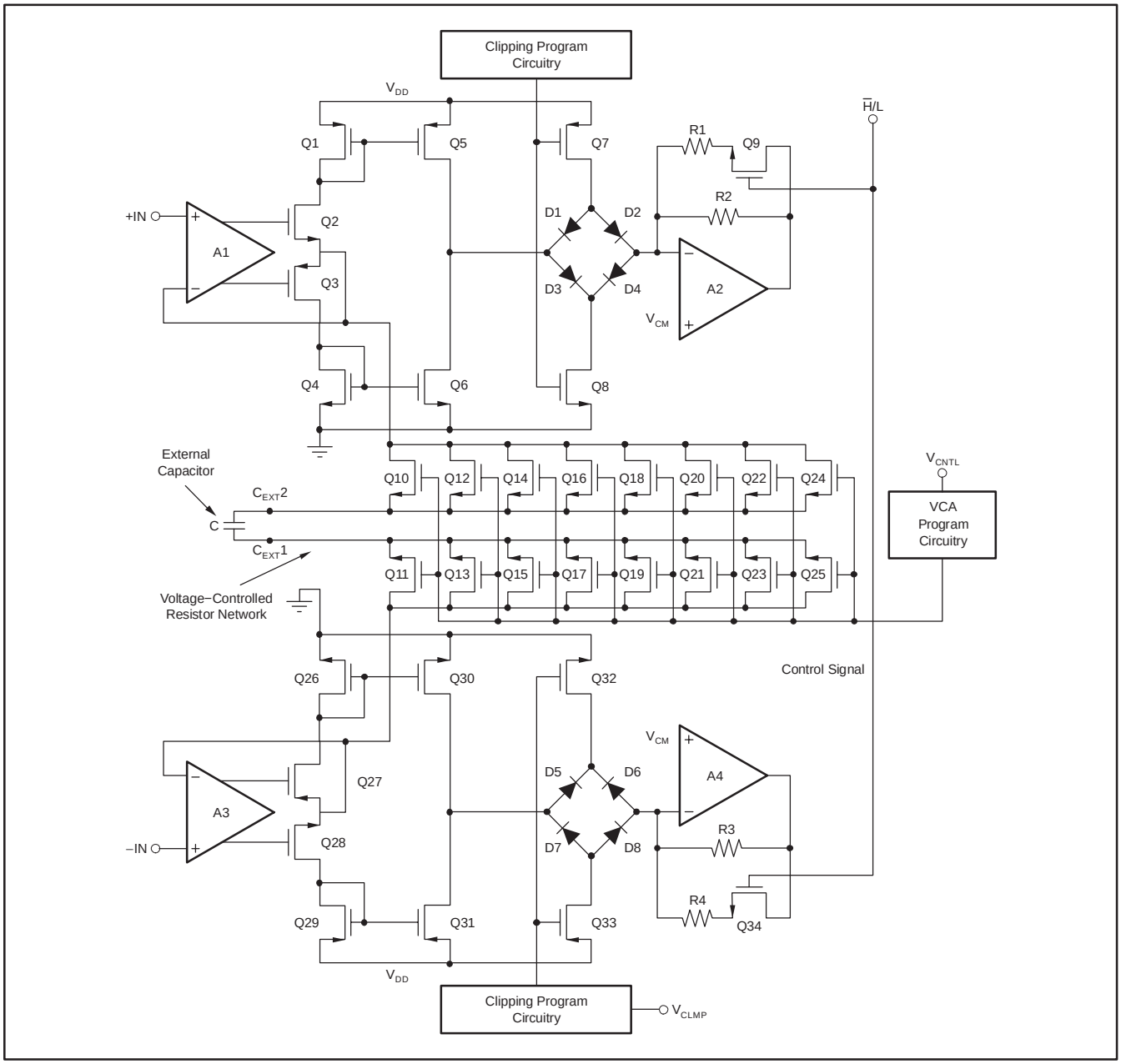


Figure 63. Block Diagram of VCA

VARIABLE GAIN CHARACTERISTICS

Transistors Q10, Q12, Q14, Q16, Q18, Q20, Q22, and Q24 form a variable resistor network that is programmed in an exponential manner to control the gain. Transistors Q11, Q13, Q15, Q17, Q19, Q21, Q23, and Q25 perform the same function. These two groups of FET variable resistors are configured in this manner to balance the capacitive loading on the total variable-resistor network. This balanced configuration is used to keep the second harmonic component of the distortion low. The common source connection associated with each group of FET variable resistors is brought out to an external pin so that an external capacitor can be used to make an AC connection. This connection is necessary to achieve an adequate low-frequency bandwidth because the coupling capacitor would be too large to include within the monolithic chip. The value of this variable resistor ranges in value from 15Ω to 5000Ω to achieve a gain range of about 44dB. The low-frequency bandwidth is then given by the formula:

$$\text{Low Frequency BW} = 1/2\pi RC \quad (7)$$

where:

R is the value of the attenuator.

C is the value of the external coupling capacitor.

For example, if a low-frequency bandwidth of 500kHz was desired and the value of R was 15Ω, then the value of the coupling capacitor would be approximately 22nF.

One of the benefits of this method of gain control is that the output offset is independent of the variable gain of the output amplifier. The DC gain of the output amplifier is extremely low; any change in the input voltage is blocked by the coupling capacitor, and no signal current flows through the variable resistor. This method also means that any offset voltage existing in the input is stored across this coupling capacitor; when the resistor value is changed, the DC output will not change. Therefore, changes in the control voltage do not appear in the output signal. Figure 64 shows the output waveform resulting from a step change in the control voltage, and Figure 65 shows the output voltage resulting when the control voltage is a full-scale ramp.

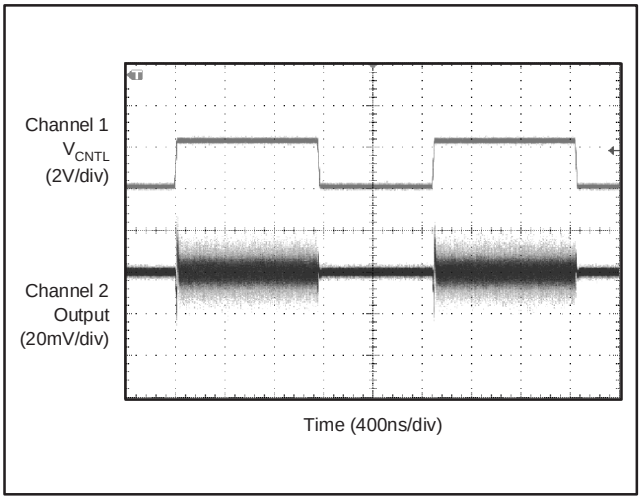


Figure 64. Response to Step Change of V_{CNTL}

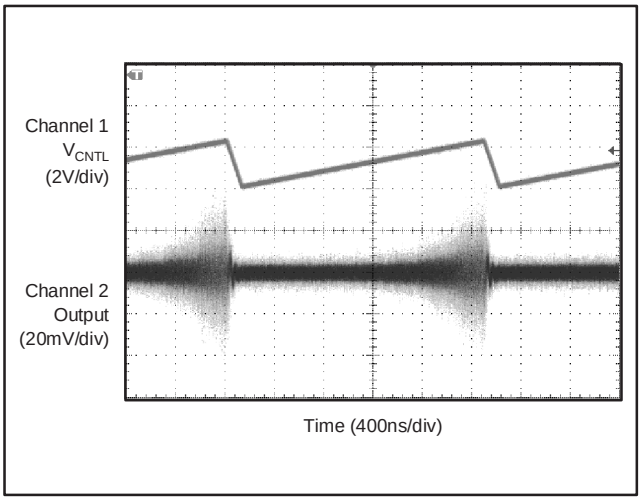


Figure 65. Response to Ramp Change of V_{CNTL}

The exponential gain control characteristic is achieved through a piecewise approximation to a perfectly smooth exponential curve. Eight FETs, operated as variable resistors whose value is progressively 1/2 of the value of the adjacent parallel FET, are turned on progressively, or their value is lowered to create the exponential gain characteristic. This characteristic can be shown in the following way. An exponential such as $y = e^x$ increases in the y dimension by a constant ratio as the x dimension increases by a constant linear amount. In other words, for a constant ($x1 - x2$), the ratio e^{x1}/e^{x2} remains the same. When FETs used as variable resistors are placed in parallel, the attenuation characteristic that is created behaves according to this same exponential characteristic at discrete points as a function of the control voltage. It does not perfectly obey an ideal exponential characteristic at other points; however, an 8-section approximation yields a ±1dB error to an ideal curve.

PROGRAMMABLE CLIPPING

The clipping level of the VCA can be programmed to a desired output. The programming feature is useful when matching the clipped level from the output of the VCA to the full-scale range of a subsequent VCA, in order to prevent the VCA from generating false spectral signals; see the circuit diagram shown in Figure 66. The signal node at the drain junction of Q5 and Q6 is sent to the diode bridge formed by diode-connected transistors, D1 through D4. The diode bridge output is determined by the current that flows through transistors Q7 and Q8. The maximum current that can then flow into the summing node of A2 is this same current; consequently, the maximum voltage output of A2 is this same current multiplied by the feedback resistor associated with A2. The maximum output voltage of A2, which would be the clipped output, can then be controlled by adjusting the current that flows through Q7 and Q8; see the circuit diagram shown in Figure 63. The circuitry of A1, R2, and Q2 converts the clamp voltage (V_{CLMP}) to a current that controls equal and opposite currents flowing through transistors Q5 and Q6.

When $\overline{H}/L$ = 0, the previously described circuitry is designed so that the value of the V_{CLMP} signal is equal to the peak differential signal developed between $+V_{OUT}$ and $-V_{OUT}$. When $\overline{H}/L$ = 1, the differential output will be equal to the clamp voltage. This method of controlled clipping also achieves fast and clean settling waveforms at the output of the VCA, as shown in Figure 67 through Figure 70. The sequence of waveforms demonstrate the clipping performance during various stages of overload. The V_{CLMP} pin represents a high impedance input (> 100kΩ).

In a typical application, the VCA2615 will drive an anti-aliasing filter, which in turn will drive an ADC. Many modern ADCs, such as the ADS5270, are well-behaved with as much as 2x overload. This means that the clipping level of the VCA should be set to overcome the loss in the filter such that the clipped input to the ADC is just slightly over the full-scale input. By setting the clipping level in this manner, the lowest harmonic distortion level will be achieved without interfering with the overload capability of the ADC.

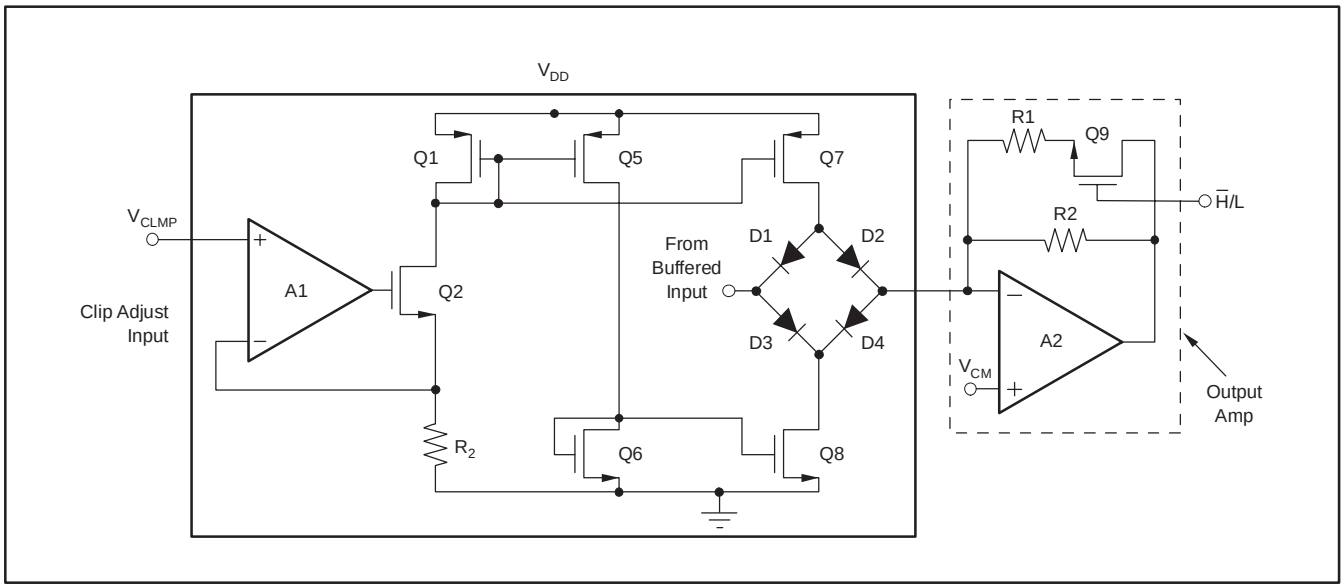


Figure 66. Clipping Level Adjust Circuitry

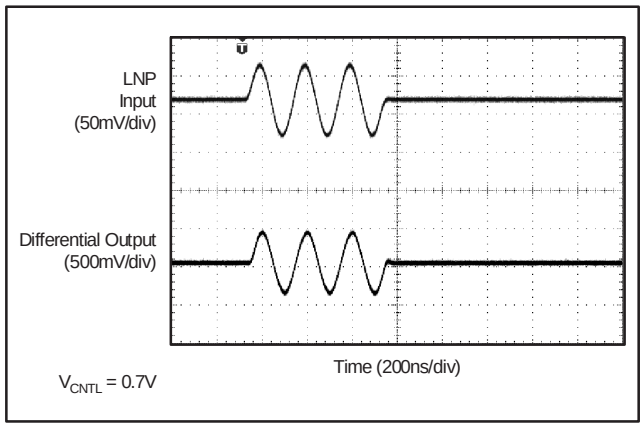


Figure 67. Before Overload (100mV$_{PP}$ Input)

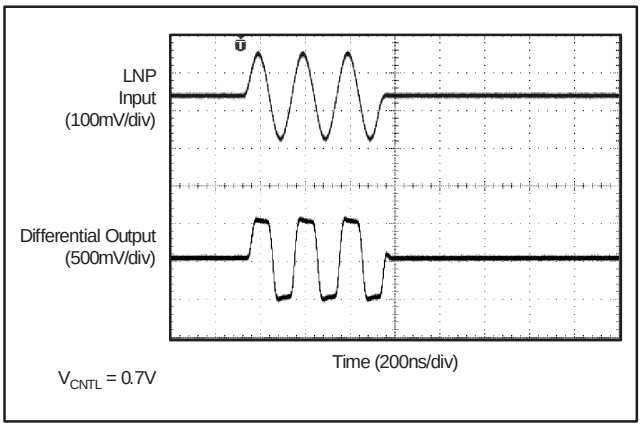


Figure 69. Overload (240mV$_{PP}$ Input)

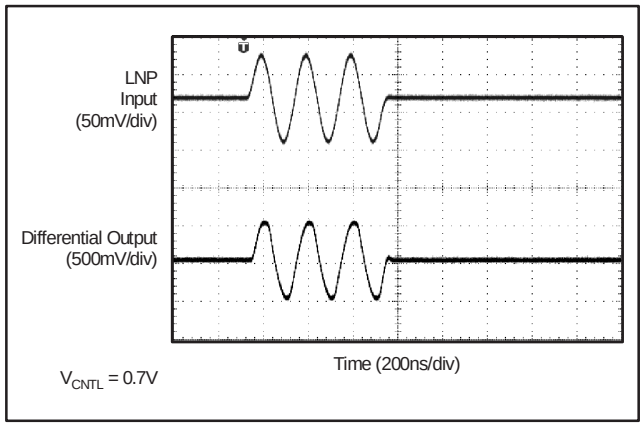


Figure 68. Approaching Overload (120mV$_{PP}$ Input)

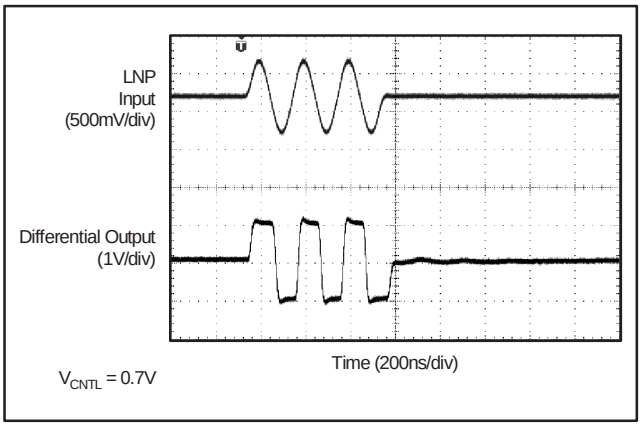


Figure 70. Extreme Overload (2V$_{PP}$ Input)

POWER-DOWN MODES

When V_{DD} (5V) is applied to the VCA2615, the total power dissipation is typically 308mW. When the power is initially applied to the VCA2615 with both PDV and PDL pins at a logic low, the typical power dissipation will be 5mW. After the VCA2615 has been enabled, if the PDL line is low with the PDV line high, the typical power dissipation will be approximately 100mW. After the VCA2615 has been enabled, if the PDV line is low with the PDL line high, the typical power dissipation will be approximately 200mW.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
10/08	D	1	Features	Deleted SMALL QFN−48 PACKAGE (7x7mm)
		1	Description	Text added to last paragraph.
		2	Package/Ordering	Added TQFP−48 package information.
		4	Electrical Characteristics	Thermal Characteristics section; added text.
8/05	C	1	Features	Changed 20dB/V to 22dB/V under LOW-NOISE VARIABLE-GAIN AMPLIFIER
		3	Electrical Characteristics	Added CA, CB = 3.9µF to the overall conditions.
		4	Electrical Characteristics	Accuracy section; moved Gain Slope line under accurary, added "V_{CNTL} = 0.4V to 2.0V" to conditions, and changed typical value from 20dBv to 22dB/V. Thermal Characteristics section; removed "Specified" and added "Operating" to conditions.
		5	Pin Configuration	Pin 19 description; changed 0.01µF to 0.1µF.
		22	Programmable Clipping	Reworded paragraph three to clarify description of setting VCA clipping level.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
VCA2615PFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA2615	Samples
VCA2615PFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA2615	Samples
VCA2615RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA 2615	Samples
VCA2615RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA 2615	Samples
VCA2615RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA 2615	Samples
VCA2615RGZTG4	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA 2615	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

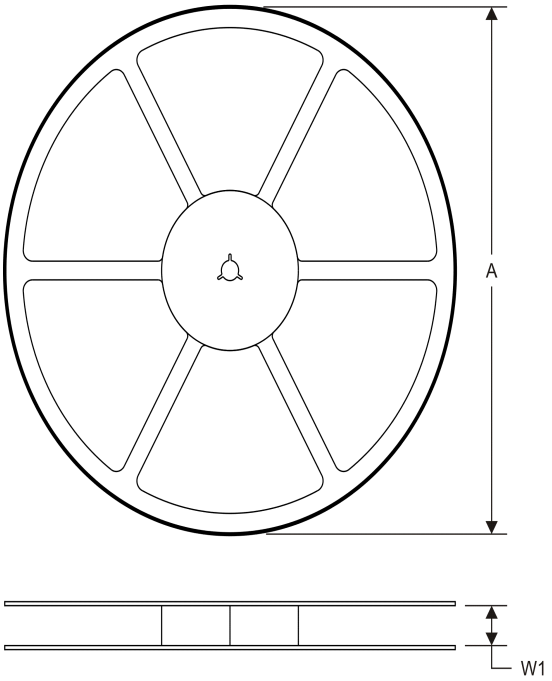
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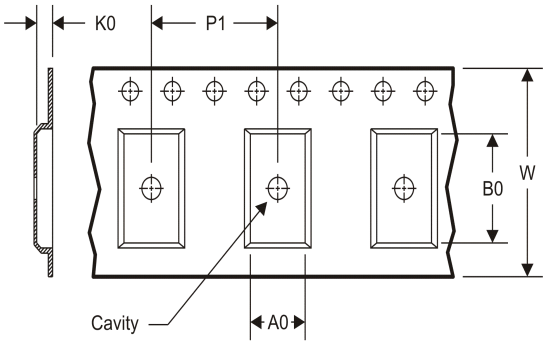
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



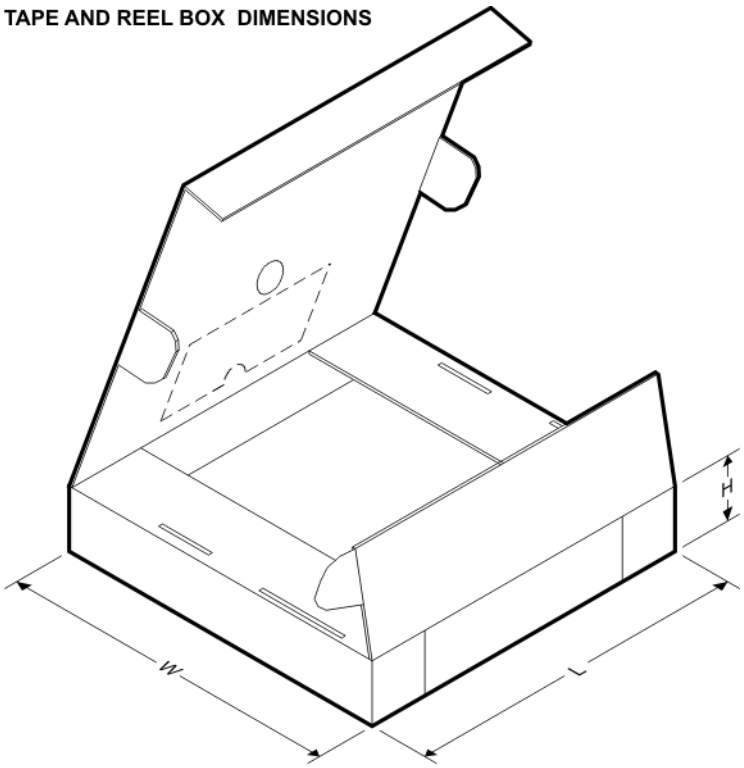
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA2615PFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
VCA2615PFBT	TQFP	PFB	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
VCA2615RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
VCA2615RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

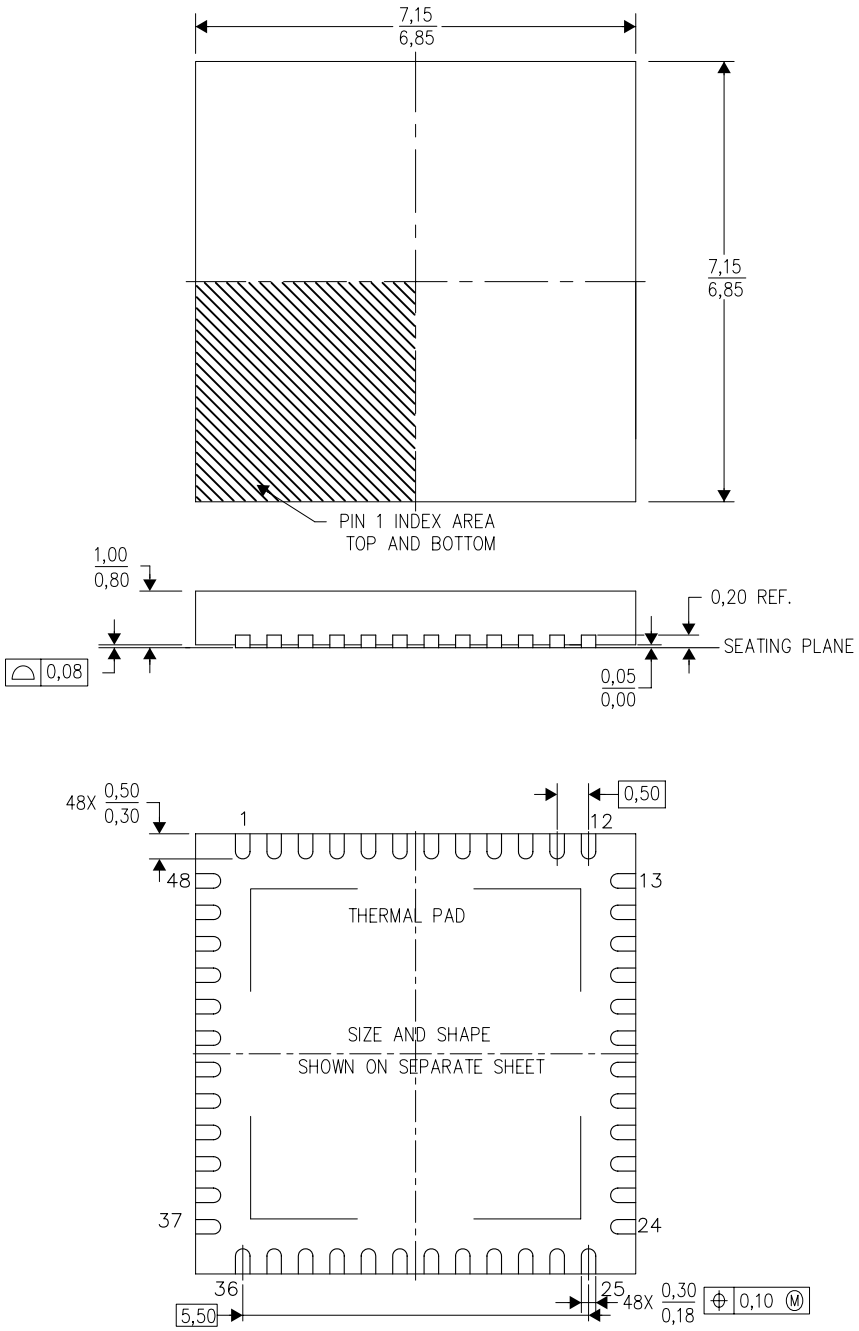
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA2615PFBR	TQFP	PFB	48	1000	367.0	367.0	38.0
VCA2615PFBT	TQFP	PFB	48	250	367.0	367.0	38.0
VCA2615RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
VCA2615RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

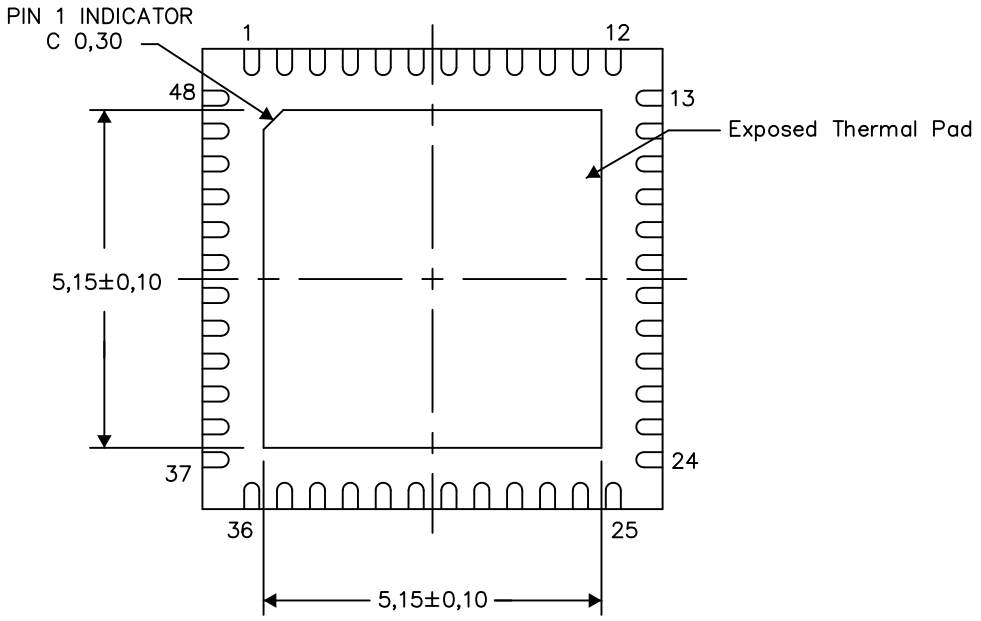
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



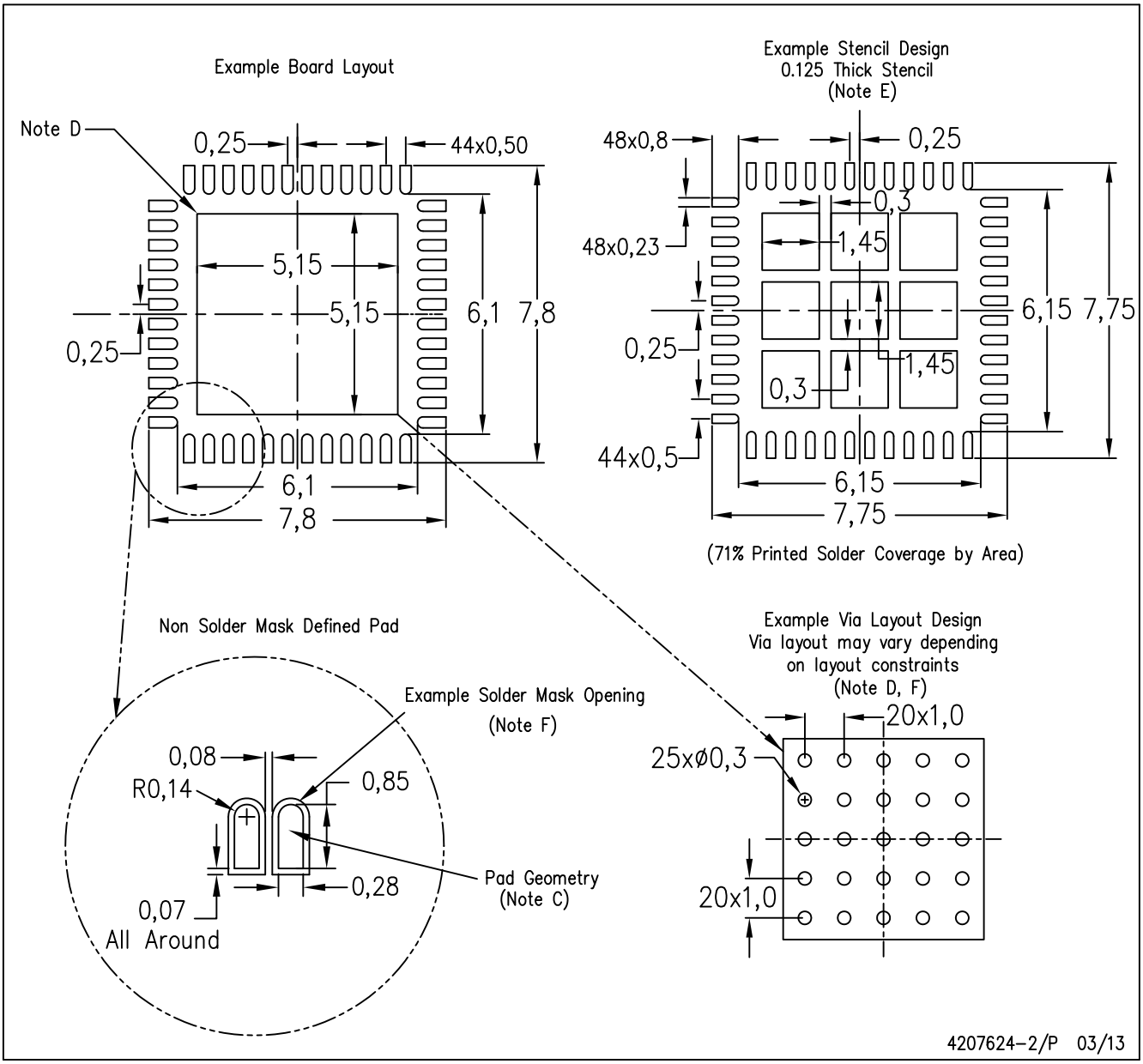
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/T 03/13

NOTE: All linear dimensions are in millimeters

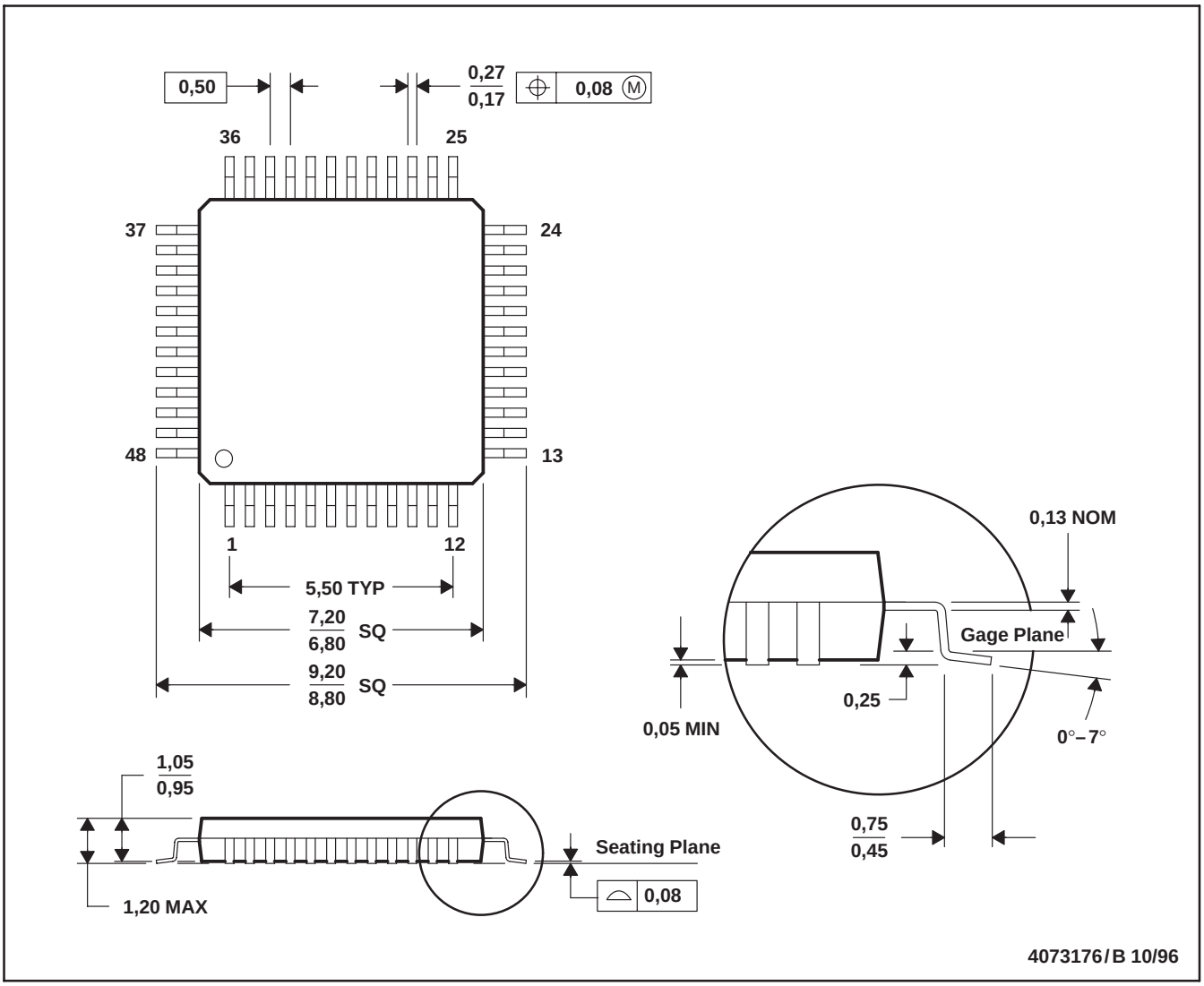
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

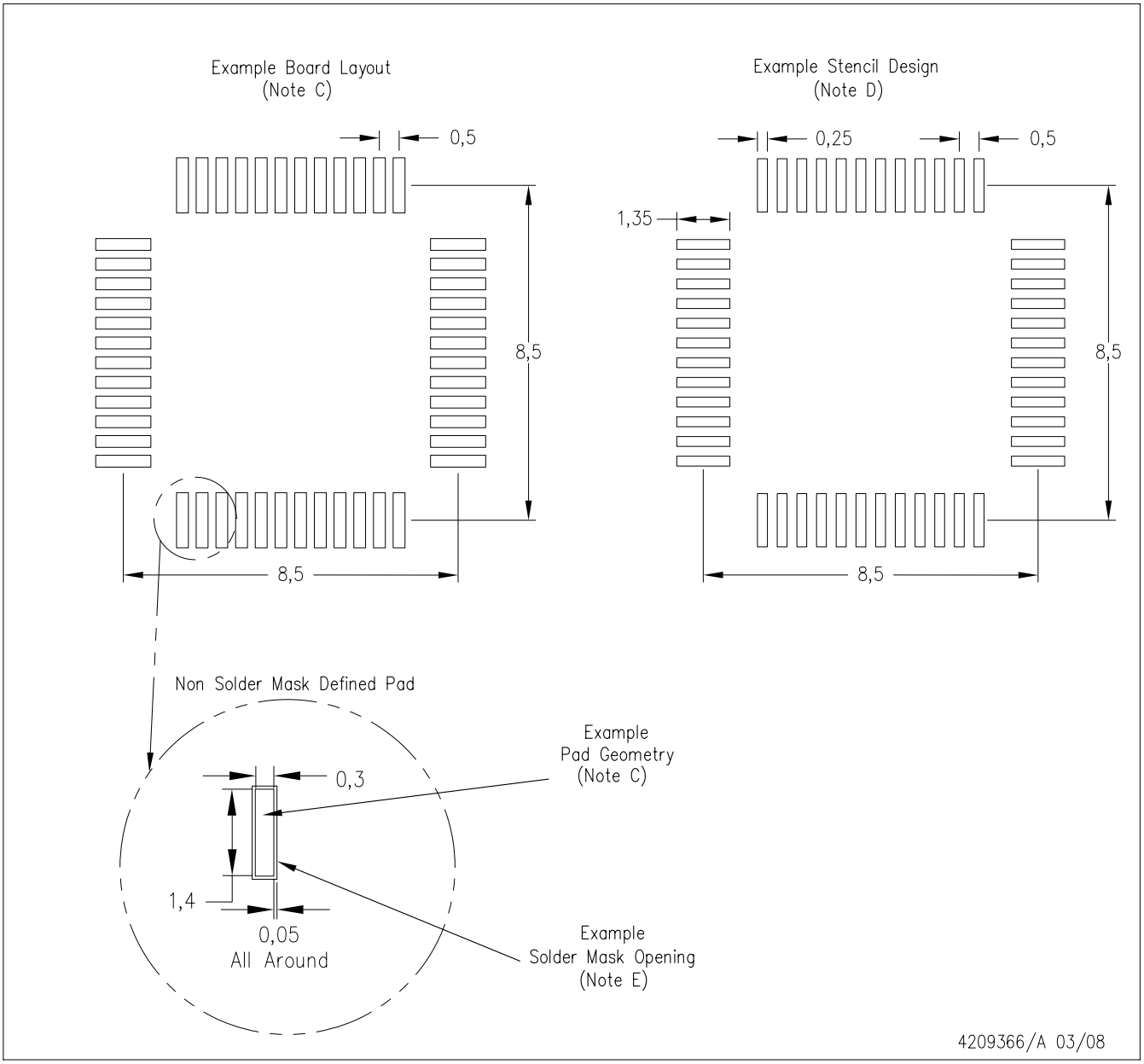
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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