3.3-V Dual Differential LVPECL/LVDS Buffer to LVTTL Translator

FEATURES

- **Dual 3.3-V Differential LVPECL/LVDS to LVTTL Buffer Translator**
- **24-mA LVTTL Ouputs**
- **Operating Range**
  - **PECL V_{CC} = 3 V to 3.6 V With GND = 0 V**
- **Support for Clock Frequencies to >180 MHz**
- **2-ns Typical Propagation Delay**
- **Internal Input Pullup and Pulldown Resistors**
- **Built-in Temperature Compensation**
- **Drop-In Compatible to MC100LVELT23**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65LVELT23 is a low-power dual LVPECL/LVDS to LVTTL translator device. The device includes circuitry to maintain inputs at $V_{CC}/2$ when left open. The SN65LVELT23 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 option.

PINOUT ASSIGNMENT

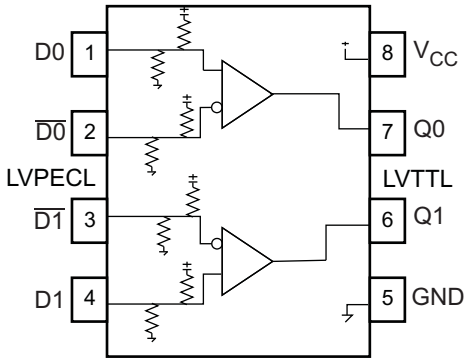


Table 1. PIN DESCRIPTION

PIN	FUNCTION
D_0, $\overline{D}_0$, D_1, $\overline{D}_1$	PECL inputs
Q_0, Q_1	TTL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVELT23D	LVEL23	SOIC	NiPdAu
SN65LVELT23DGK	SIMI	MSOP	NiPdAu

(1) Devices with lead (Pb)-bearing terminals not initially available; contact TI sales representative for further information.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, V_{CC}		3.8	V
Absolute input voltage, V_I	GND = 0 and Vi ≤ V_{CC}	0 to 3.8	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT-BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79	°C/W
		MSOP	120	
θ_{JC}	Junction-to-case thermal resistance	SOIC	98	°C/W
		MSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Level 1
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in. (3.18 mm)
ESD human-body model	2 kV
ESD charged-device model	1.5 kV
Internal pulldown resistor	50 kΩ
Internal pullup resistor	50 kΩ
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

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LVTTL OUTPUT DC CHARACTERISTICS(1) (V_{CC} = 3.3 V; GND = 0 V)(2)

PARAMETER		CONDITION	–40°C			25°C			85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Output short-circuit current		–120		–30		–120	–30	–120		–30	mA
V_{OH}	Output high voltage(3)	I_{OH} = –3.0 mA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 24 mA			0.5			0.5			0.5	V

(1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) All values vary 1:1 with Vcc; Vcc can vary ±0.3 V
(3) LVTTL output R_L = 500 Ω to GND

LVPECL INPUT DC CHARACTERISTICS(1) (V_{CC} = 3.3 V; GND = 0.0 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH}	Power-supply current (outputs set to high)	10	21	25	10	21	25	10	21	25	mA
I_{CCL}	Power-supply current (outputs set to low)	15	21	27	15	21	27	15	21	27	mA
V_{IH}	Input high voltage(3)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input low voltage(3)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input high-voltage common-mode range (differential) (4)	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input high current			150			150			150	µA
I_{IL}	Input low current	–150			–150			–150			µA

(1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
(3) LVTTL output R_L = 500 Ω to GND
(4) V_{IHCMR} minimum varies 1:1 with GND, V_{IHCMR} maximum varies 1:1 with V_{CC}.

AC CHARACTERISTICS(1) (V_{CC} = 3.3 V; GND = 0.0 V)(2) (3)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency(4)	180	300		180	300		180	300		MHz
t_{PLH}/t_{PHL}	Propagation delay to output at 1.5 V	1.2	1.6	2.2	1.2	1.7	2.2	1.2	1.8	2.2	ns
t_{SK++}	Output-to-output skew++		30	160		30	150		30	150	ps
t_{SK--}	Output to output skew– –		45	180		45	160		45	135	ps
t_{SKPP}	Part- to-part skew (5)		60	200		60	200		70	200	ps
t_{JITTER}	Random clock jitter (RMS)		4	10		4	10		4	10	ps
V_{PP}	Input voltage swing (6)	200	800	1000	200	800	1000	200	800	1000	mV
t_r/t_f	Output rise/fall times (0.8 V – 2 V)	330	585	900	330	600	900	330	630	900	ps

(1) Device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
(3) TTL output R_L = 500 Ω to GND and C_L = 20 pF to GND; see Figure 1.
(4) f_{max} measured for V_{OL} < 0.5 V and V_{OH} > 2.4 V. See Figure 5.
(5) Skews are measured between outputs under identical conditions.
(6) 200-mV input assured full logic swing at the output.

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Typical Output Loading Used for Device Evaluation

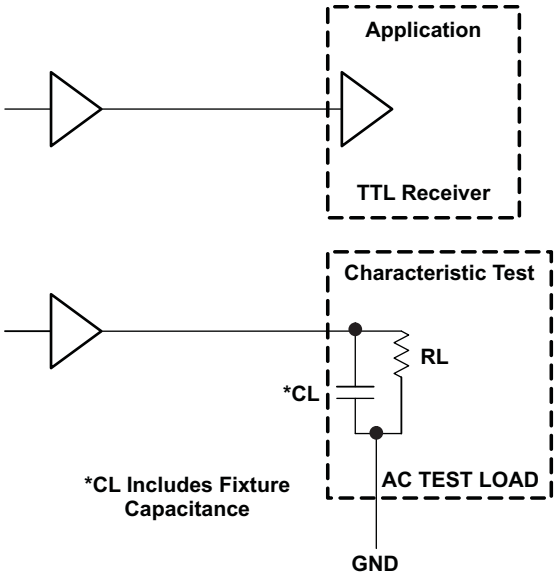


Figure 1. TTL Output Loading Used for Device Evaluation

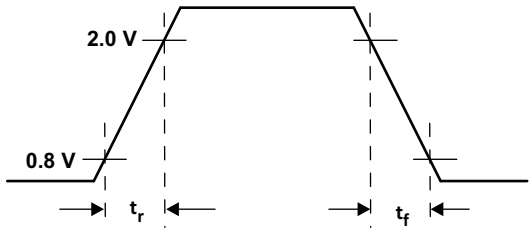


Figure 2. Output Rise and Fall Times

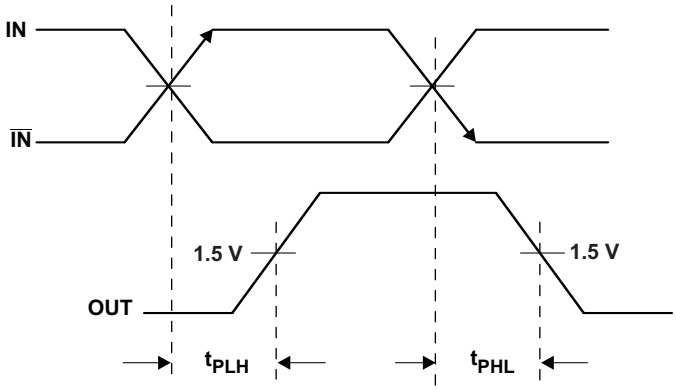


Figure 3. Output Propagation Delay

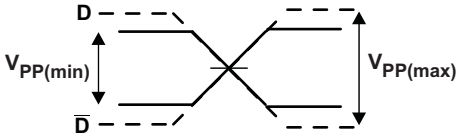


Figure 4. Input Voltage Swing

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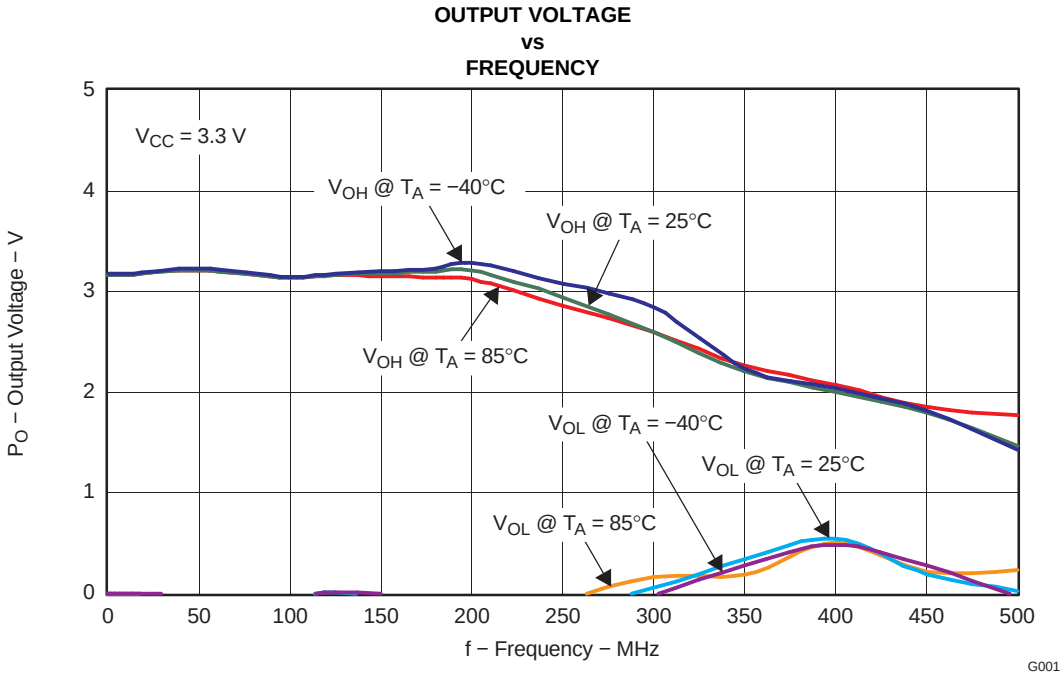

OUTPUT VOLTAGE
vs
FREQUENCY
V_{CC} = 3.3 V
V_{OH} @ T_A = −40°C
V_{OH} @ T_A = 25°C
V_{OH} @ T_A = 85°C
V_{OL} @ T_A = −40°C
V_{OL} @ T_A = 25°C
V_{OL} @ T_A = 85°C
P_O − Output Voltage − V
f − Frequency − MHz
0
1
2
3
4
5
0
50
100
150
200
250
300
350
400
450
500
G001

Figure 5.

REVISION HISTORY

Changes from Revision Original (June 2009) to Revision A	Page
• Changed MIN and MAX values for t_{PLH}/t_{PHL} in AC CHARACTERISTICS table	3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65LVELT23D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVELT23DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVELT23DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVELT23DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

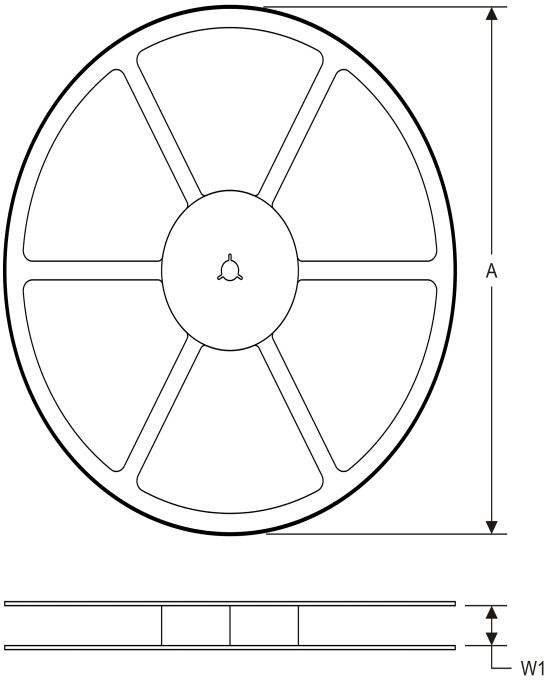
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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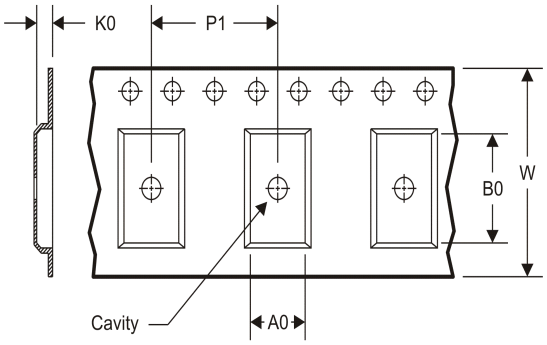
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



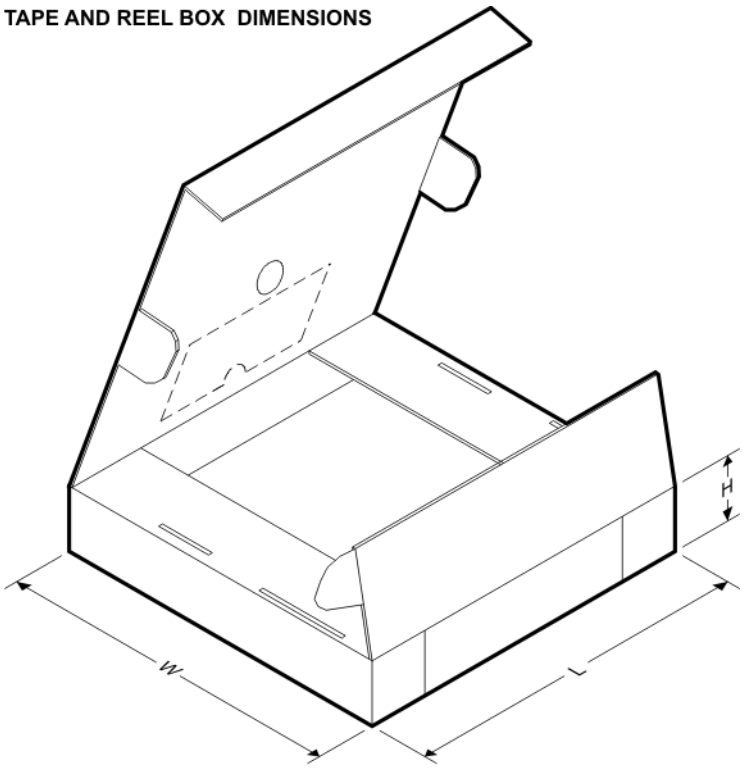
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVELT23DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVELT23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

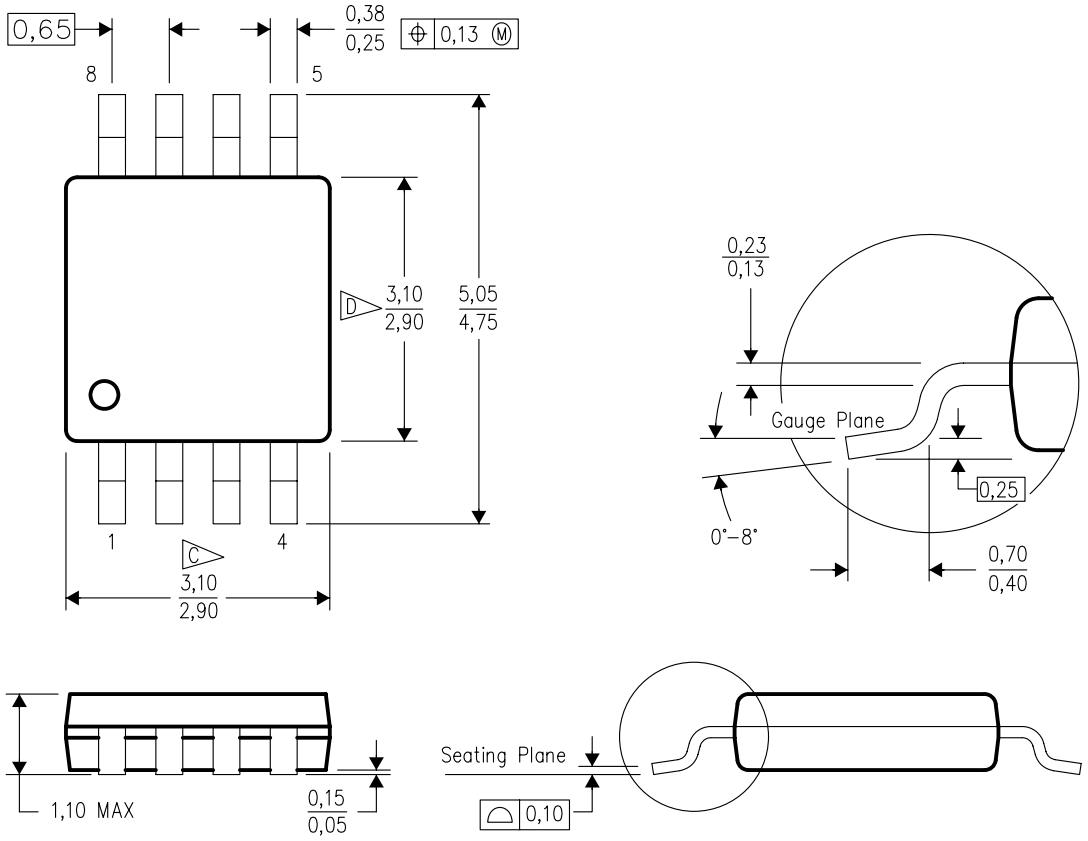
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVELT23DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65LVELT23DR	SOIC	D	8	2500	367.0	367.0	35.0

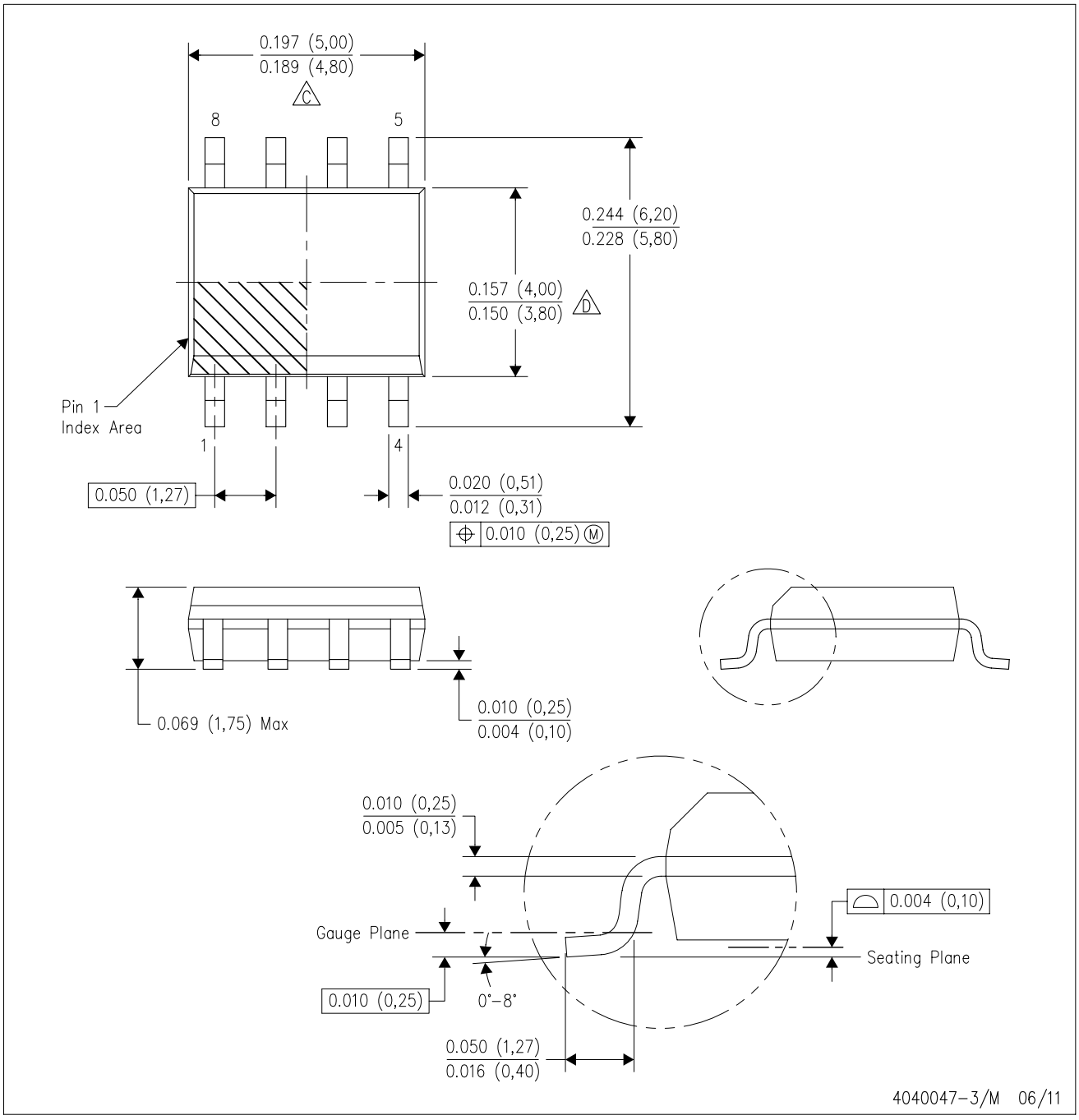
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

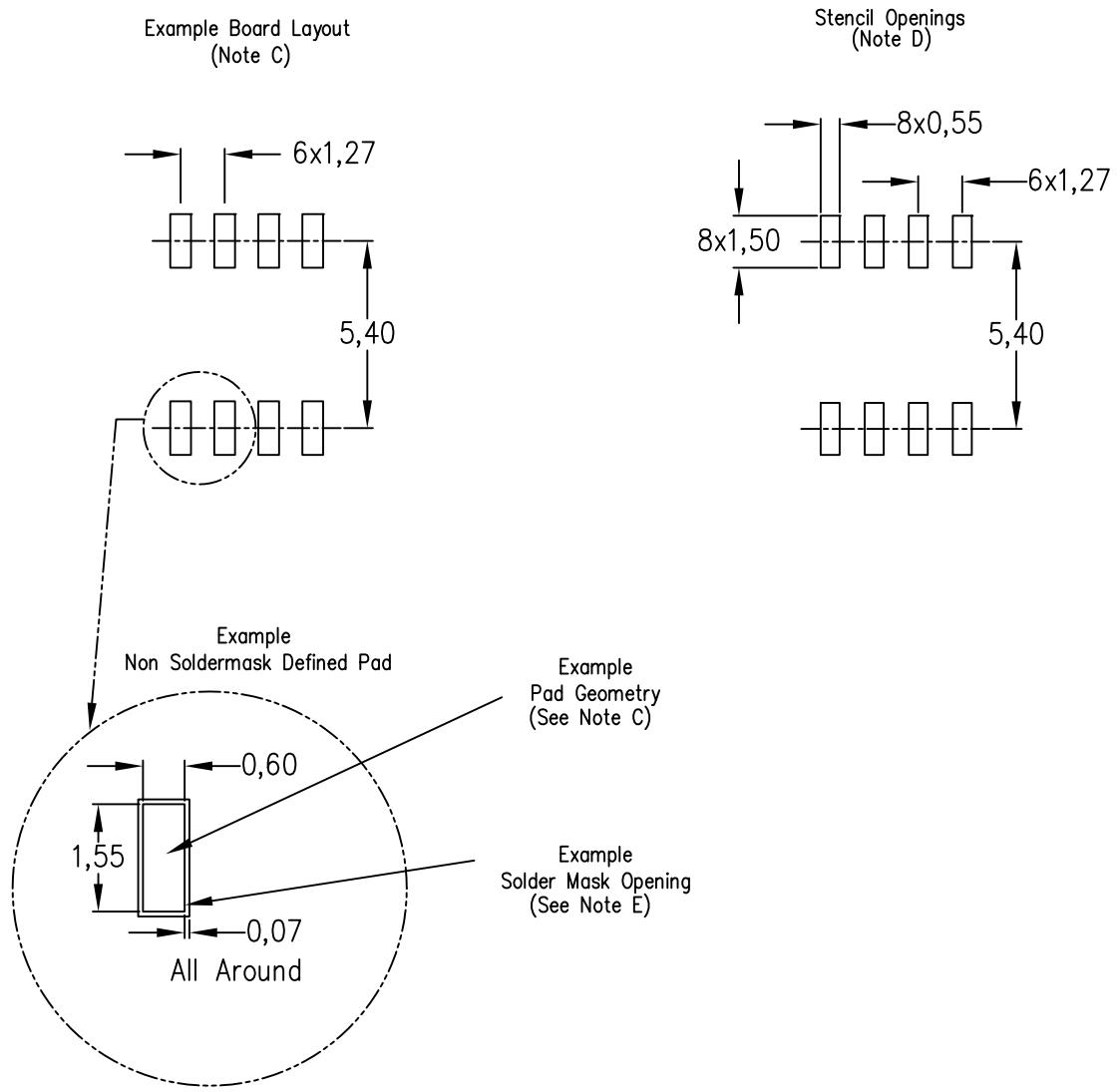
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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