50 MHz to 3.5 GHz, 45 dB RF Detector

AD8312

FEATURES

Complete RF detector function
Typical range: −45 dBm to 0 dBm, re 50 Ω
Frequency response from 50 MHz to 3.5 GHz
Temperature-stable linear-in-dB response
Accurate to 3.5 GHz
Rapid response: 85/120 ns (rise/fall)
Low power: 12 mW at 2.7 V

APPLICATIONS

Cellular handsets (GSM, CDMA, WCDMA)
RSSI and TSSI for wireless terminal devices
Transmitter power measurement

GENERAL DESCRIPTION

The AD8312 is a complete, low cost subsystem for the measurement of RF signals in the frequency range of 50 MHz to 3.5 GHz. It has a typical dynamic range of 45 dB and is intended for use in a wide variety of cellular handsets and other wireless devices. It provides a wider dynamic range and better accuracy than possible using discrete diode detectors. In particular, its temperature stability is excellent over the full operating range of −40°C to +85°C.

Its high sensitivity allows measurement at low power levels, thus reducing the amount of power that needs to be coupled to the detector. It is essentially a voltage-responding device, with a typical signal range of 1.25 mV to 224 mV rms or −45 dBm to 0 dBm, re 50 Ω.

For convenience, the signal is internally ac-coupled, using a 5 pF capacitor to a load of 3 kΩ in shunt with 1.3 pF. This high-pass coupling, with a corner at approximately 16 MHz, determines the lowest operating frequency. Therefore, the source may be dc grounded.

The AD8312 output, VOUT, increases from close to ground to about 1.2 V because the input signal level increases from 1.25 mV to 224 mV. A capacitor may be connected between the VOUT and CFLT pins when it is desirable to increase the time interval over which averaging of the input waveform occurs.

The AD8312 is available in a 6-ball, 1.0 mm × 1.5 mm, wafer-level chip scale package and consumes 4.2 mA from a 2.7 V to 5.5 V supply.

FUNCTIONAL BLOCK DIAGRAM

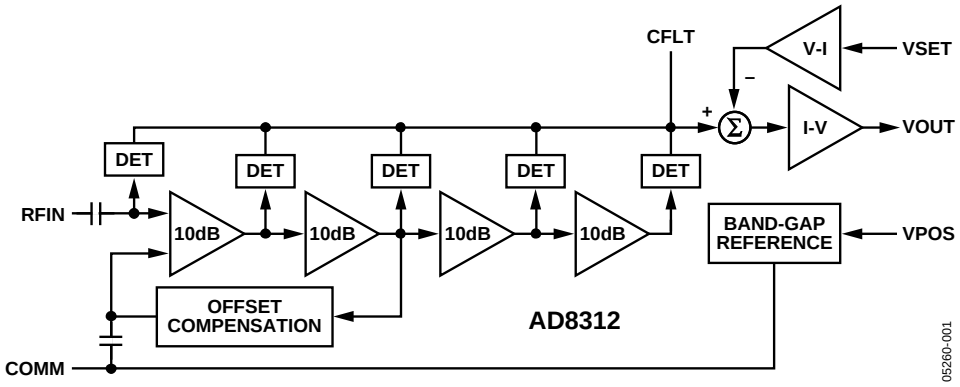


Figure 1.

Rev. A
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TABLE OF CONTENTS

Specifications ... 3
Absolute Maximum Ratings ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 8
General Description ... 12
Applications ... 13
Basic Connections ... 13
Transfer Function in Terms of Slope and Intercept ... 13
Filter Capacitor ... 14
Input Coupling Options ... 14
Increasing the Logarithmic Slope ... 15
Effect of Waveform Type on Intercept ... 15
Temperature Drift ... 16
Operation Above 2.5 GHz ... 16
Device Handling ... 16
Evaluation Board ... 16
Outline Dimensions ... 19
Ordering Guide ... 19

REVISION HISTORY

1/11—Rev. 0 to Rev. A

Changes to Figure 29 ... 16
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

4/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = 3 V, CFLT = open, T_A = 25°C, light condition = 600 LUX, 52.3 Ω termination resistor at RFIN, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	RFIN (Pin 6)				
Specified Frequency Range		0.05		3.5	GHz
Input Voltage Range	Internally ac-coupled	1.25		224	mV rms
Equivalent Power Range	52.3 Ω external termination	−45		0	dBm
DC Resistance to COMM			100		kΩ
MEASUREMENT MODE	VOUT (Pin 2) shorted to VSET (Pin 3), sinusoidal input signal				
f = 50 MHz					
Input Impedance			3050 || 1.4		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		50		dB
	−40°C < T_A < +85°C		42		dB
Maximum Input Level	±1 dB error		3		dBm
Minimum Input Level	±1 dB error		−47		dBm
Slope			20.25		mV/dB
Intercept			−51.5		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.841		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		0.232		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		0.0010		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0073		dB/°C
f = 100 MHz					
Input Impedance			2900 || 1.3		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		48		dB
	−40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		2		dBm
Minimum Input Level	±1 dB error		−46		dBm
Slope		19.0	21.0	23.0	mV/dB
Intercept		−56.0	−50.5	−47.0	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.850		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		0.222		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		0.0002		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0060		dB/°C
f = 900 MHz					
Input Impedance			890 || 1.15		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		49		dB
	−40°C < T_A < +85°C		42		dB
Maximum Input Level	±1 dB error		1		dBm
Minimum Input Level	±1 dB error		−48.0		dBm
Slope			20.25		mV/dB
Intercept			−51.9		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.847		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		0.237		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.0019		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0010		dB/°C

Parameter	Conditions	Min	Typ	Max	Unit
f = 1.9 GHz					
Input Impedance			450 || 1.13		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		48		dB
	−40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		1		dBm
Minimum Input Level	±1 dB error		−47		dBm
Slope			19.47		mV/dB
Intercept			−52.4		dBm
Output Voltage – High Power In	P_{IN} = −10 dBm		0.826		V
Output Voltage – Low Power In	P_{IN} = −40 dBm		0.240		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.004		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.005		dB/°C
f = 2.2 GHz					
Input Impedance			430 || 1.09		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		48		dB
	−40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		1		dBm
Minimum Input Level	±1 dB error		−47		dBm
Slope			19.1		mV/dB
Intercept			−52.1		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.803		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		0.230		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		−0.0023		dB/°C
	−40°C ≤ T_A ≤ +25°C		0.0055		dB/°C
f = 2.5 GHz					
Input Impedance			400 || 1.03		Ω || pF
±1 dB Dynamic Range	T_A = 25°C		49		dB
	−40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		1		dBm
Minimum Input Level	±1 dB error		−48		dBm
Slope			18.6		mV/dB
Intercept			−51.2		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.762		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		0.204		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 85°C		0.005		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0126		dB/°C
OUTPUT INTERFACE	VOUT (Pin 2)				
Minimum Output Voltage	No signal at RFIN, R_L ≥ 10 kΩ		0.02	0.2	V
Maximum Output Voltage[1]	R_L ≥ 10 kΩ	1.8	2.0		V
General Limit	2.7 V ≤ V_S ≤ 5.5 V	V_S – 1.2	V_S – 1		V
Available Output Current	Sourcing/sinking		2/0.1		mA
Residual RF (at 2f)	f = 0.1 GHz (worst condition)		100		µV
Output Noise	RF input = 2.2 GHz, −10 dBm, f_{NOISE} = 100 kHz, CFLT open		1.4		µV/√Hz
Fall Time	Input level = off to 0 dBm, 90% to 10%		120		ns
Rise Time	Input level = 0 dBm to off, 10% to 90%		85		ns
VSET INTERFACE	VSET (Pin 3)				
Input Resistance			13		kΩ
Bias Current Source	RFIN = −10 dBm; VSET = 1.2 V		75		µA

Parameter	Conditions	Min	Typ	Max	Unit
POWER INTERFACE	VPOS (Pin 1)				
Supply Voltage		2.7	3.0	5.5	V
Quiescent Current		2.8	4.2	5.7	mA
vs. Temperature	$-40°C \le T_A \le +85°C$		4.3		mA

[1] Increased output is possible when using an attenuator between VOUT and VSET to raise the slope.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Value
Supply Voltage VPOS	5.5 V
VOUT, VSET	0 V, VPOS
Input Voltage	1.6 V rms
Equivalent Power	17 dBm
Internal Power Dissipation	200 mW
θ_{JA} (WLCSP)	200°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

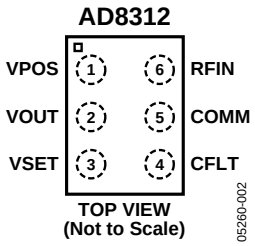


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Ball No.	Mnemonic	Description
1	VPOS	Positive Supply Voltage (V_S), 2.7 V to 5.5 V.
2	VOUT	Logarithmic Output. Output voltage increases with increasing input amplitude.
3	VSET	Setpoint Input. Connect VSET to VOUT for measurement-mode operation. The nominal logarithmic slope of 20 mV/dB can be increased to an arbitrarily high value by attenuating the signal between VOUT and VSET (see the Increasing the Logarithmic Slope section).
4	CFLT	Connection for an External Capacitor to Slow the Response of the Output. Capacitor is connected between CFLT and VOUT.
5	COMM	Device Common (Ground).
6	RFIN	RF Input.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3 V; T_A = 25°C; C_{FLT} = open; light condition = 600 LUX, 52.3 Ω termination; unless otherwise noted. Colors: +25°C = Black, −40°C = Blue, +85°C = Red.

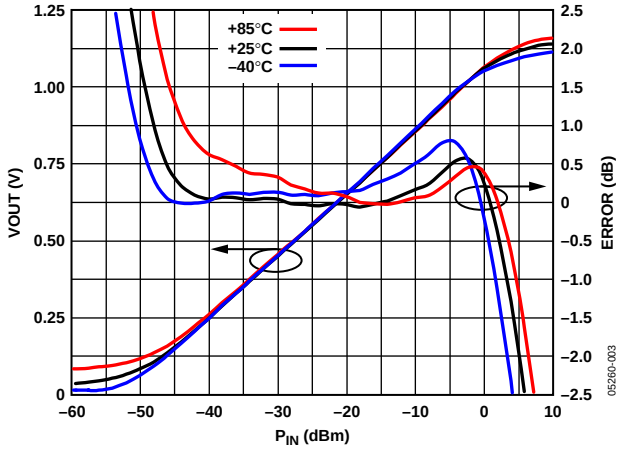


Figure 3. VOUT and Log Conformance vs. Input Amplitude at 50 MHz; Typical Device at −40°C, +25°C, and +85°C

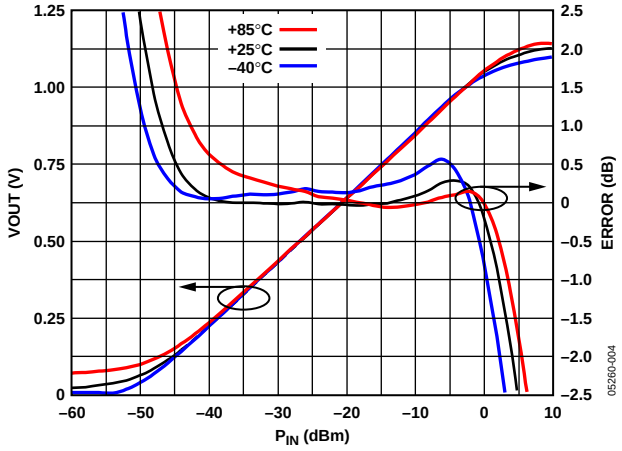


Figure 4. VOUT and Log Conformance vs. Input Amplitude at 100 MHz; Typical Device at −40°C, +25°C, and +85°C

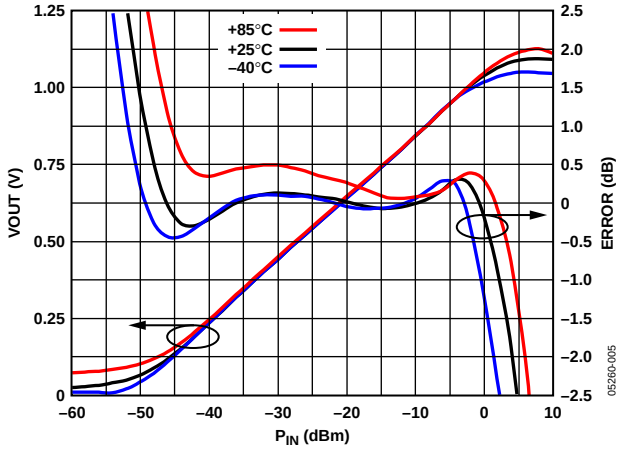


Figure 5. VOUT and Log Conformance vs. Input Amplitude at 900 MHz; Typical Device at −40°C, +25°C, and +85°C

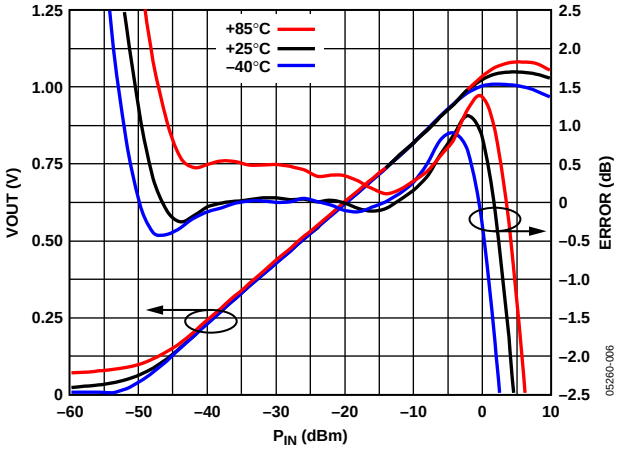


Figure 6. VOUT and Log Conformance vs. Input Amplitude at 1.9 GHz; Typical Device at −40°C, +25°C, and +85°C

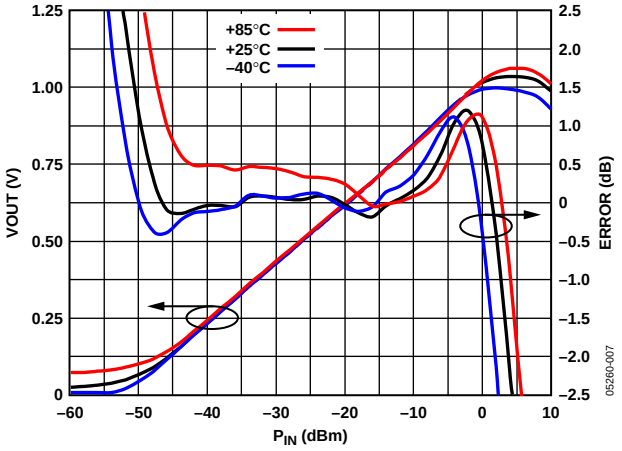


Figure 7. VOUT and Log Conformance vs. Input Amplitude at 2.2 GHz; Typical Device at −40°C, +25°C, and +85°C

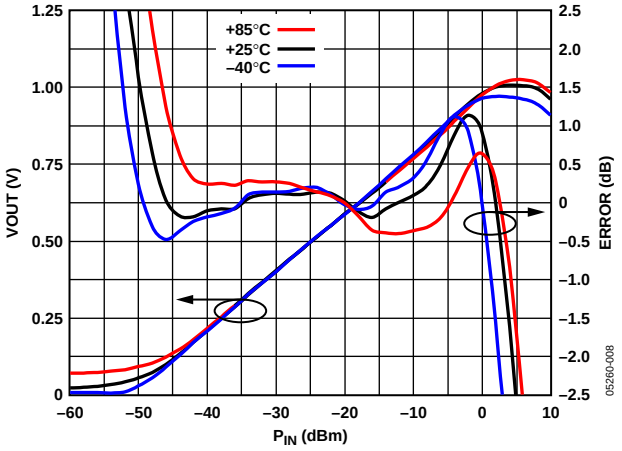


Figure 8. VOUT and Log Conformance vs. Input Amplitude at 2.5 GHz; Typical Device at −40°C, +25°C, and +85°C

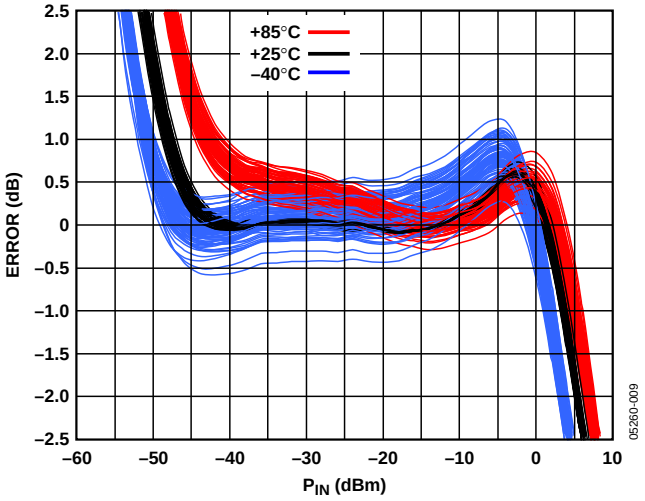


Figure 9. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 50 MHz for 80 Devices

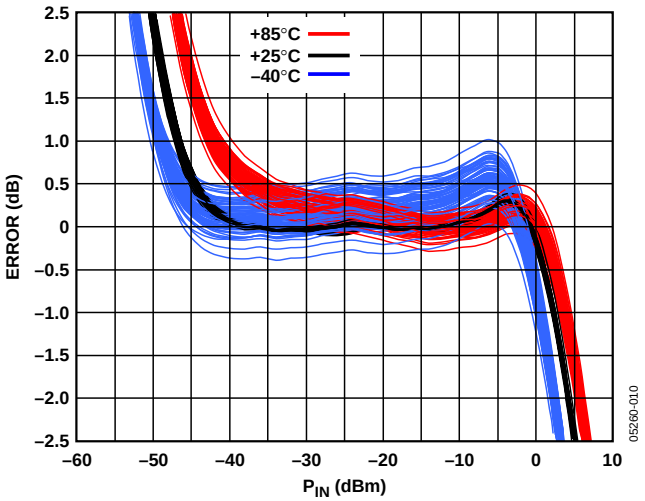


Figure 10. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 100 MHz for 80 Devices

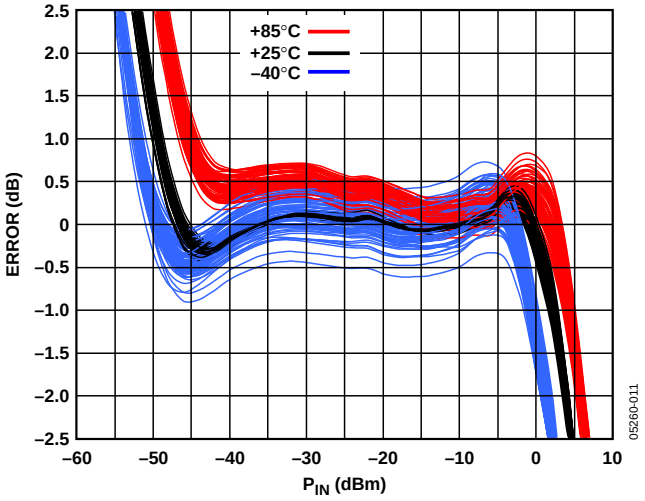


Figure 11. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 900 MHz for 80 Devices

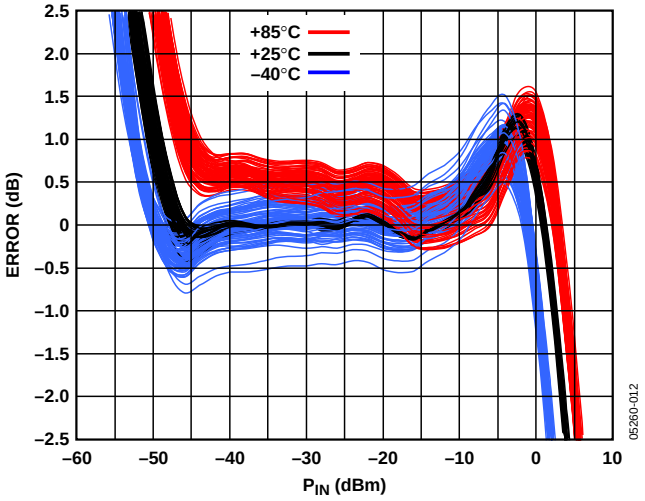


Figure 12. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 1.9 GHz for 80 Devices

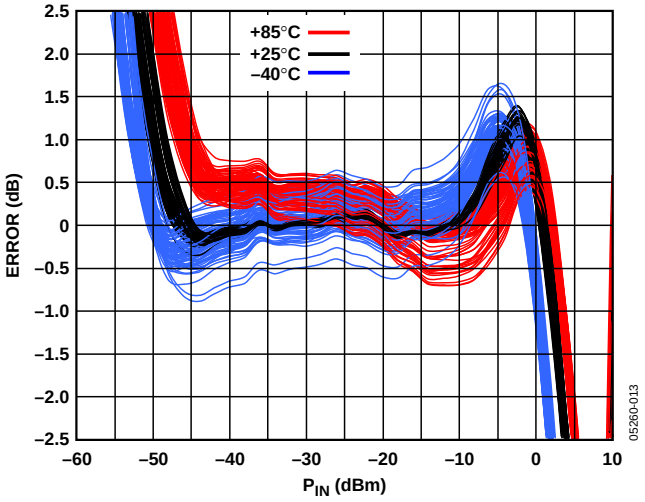


Figure 13. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 2.2 GHz for 80 Devices

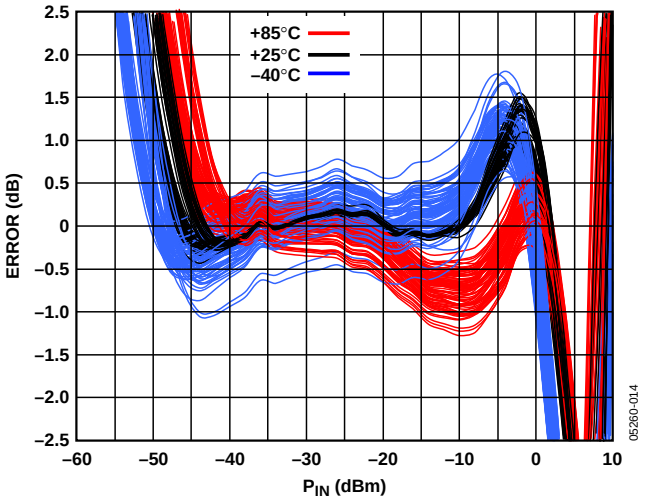


Figure 14. Distribution of Error at −40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 2.5 GHz for 80 Devices

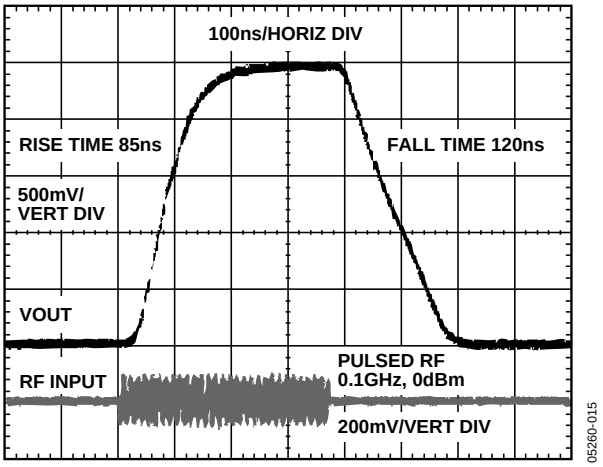


Figure 15. VOUT Response Time, RF Off to 0 dBm

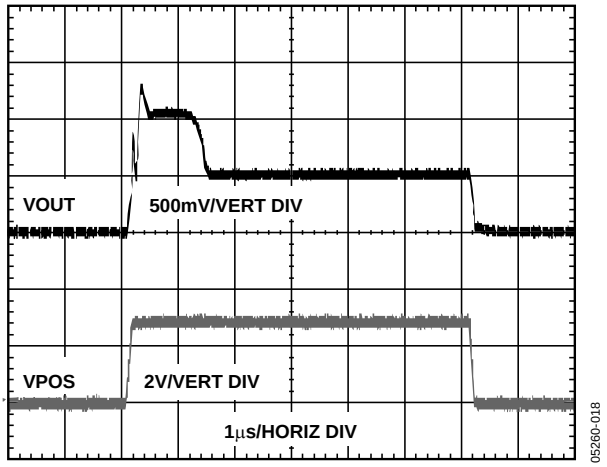


Figure 18. Power-On and Power-Off Response

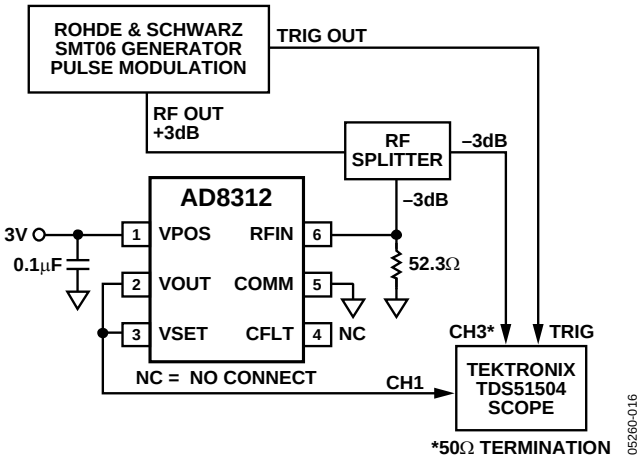


Figure 16. Test Setup for Pulse Response

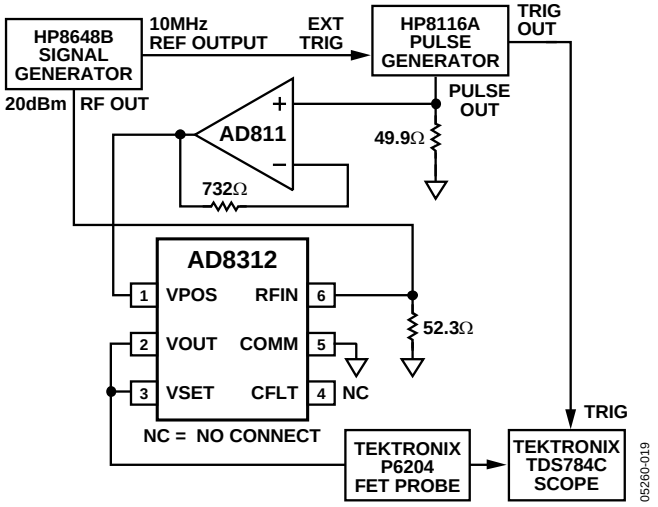


Figure 19. Test Setup for Power-On and Power-Off Response

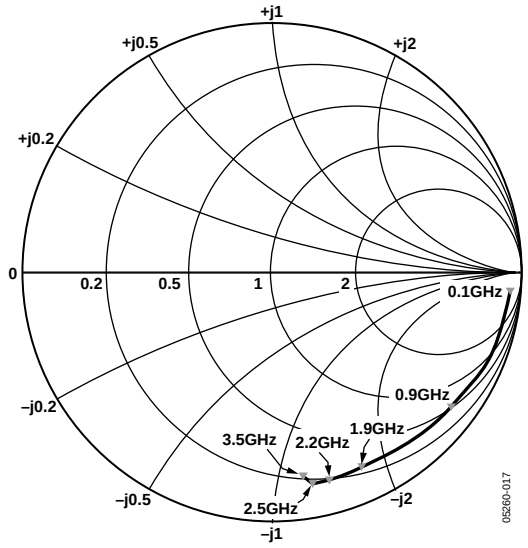


Figure 17. Input Impedance vs. Frequency; No Termination Resistor on RFIN

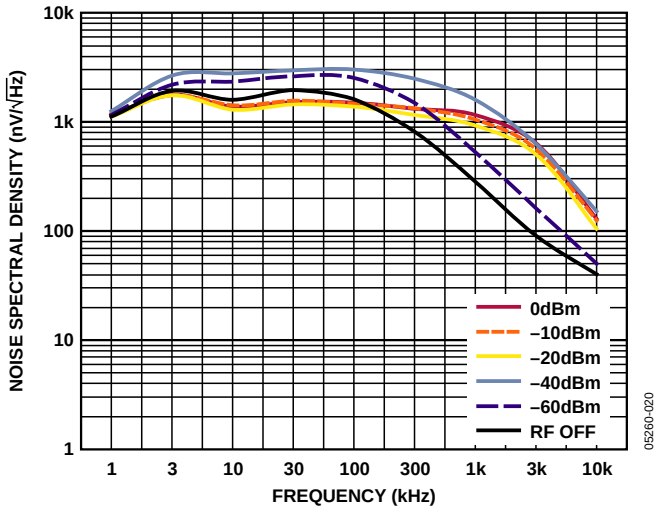


Figure 20. Noise Spectral Density of Output; CFLT = Open

Table 4. Typical Specifications at Selected Frequencies at 25°C (Mean and Σ)

	Slope (mV/dB)		Intercept (dBm)		±1 dB Dynamic Range[1] (dBm)			
					High Point		Low Point	
Frequency (GHz)	μ	σ	μ	σ	μ	σ	μ	σ
0.05	20.25	0.3	−51.5	0.4	+3.0	0.12	−48.0	0.13
0.1	21.0	0.2	−50.5	0.4	+2.0	0.1	−46.0	0.1
0.9	20.25	0.3	−51.9	0.4	+0.2	0.1	−49.0	0.2
1.9	19.47	0.3	−52.4	0.6	+1.5	0.12	−48.8	0.3
2.2	19.1	0.4	−52.1	0.85	+1.5	0.2	−48.5	0.4
2.5	18.6	0.6	−51.2	1.2	+2.0	0.3	−47.7	0.5
3.0	17.5	0.7	−46.9	2.5	−4	0.3	−46	0.4
3.5	17.1	0.7	−42.6	2.5	−1	0.3	−39	0.3

[1] Refer to Figure 23.

GENERAL DESCRIPTION

The AD8312 is a logarithmic amplifier (log amp) similar in design to the AD8313; further details about the structure and function may be found in the AD8313 data sheet and the data sheets of other log amplifiers produced by ADI. Figure 21 shows the main features of the AD8312 in block schematic form.

The AD8312 combines two key functions needed for the measurement of signal level over a moderately wide dynamic range. First, it provides the amplification needed to respond to small signals in a chain of four amplifier/limiter cells, each having a small-signal gain of 10 dB and a bandwidth of approximately 3.5 GHz. At the output of each amplifier stage is a full-wave rectifier, essentially a square-law detector cell, which converts the RF signal voltages to a fluctuating current with an average value that increases with signal level. A further passive detector stage is added ahead of the first stage. Therefore, there are five detectors, each separated by 10 dB, spanning some 50 dB of dynamic range. The overall accuracy at the extremes of this total range, viewed as the deviation from an ideal logarithmic response, that is, the law-conformance error, can be judged by reference to Figure 3 through Figure 8, which show that errors across the central 40 dB are moderate. These figures show how the conformance to an ideal logarithmic function varies with temperature and frequency.

The output of these detector cells is in the form of a differential current, making their summation a simple matter. It can easily be shown that such summation closely approximates a logarithmic function. This result is then converted to a voltage at the VOUT pin through a high gain stage. In measurement modes, this output is connected back to a voltage-to-current (V-to-I) stage, in such a manner that VOUT is a logarithmic measure of the RF input voltage with a slope and intercept controlled by the design. For a fixed termination resistance at the input of the AD8312, a given voltage corresponds to a certain power level.

The external termination added before the AD8312 determines the effective power scaling. This often takes the form of a simple resistor (52.3 Ω provides a net 50 Ω input), but more elaborate matching networks may be used. This impedance determines the logarithmic intercept, the input power for which the output would cross the baseline (VOUT = 0) if the function were continuous for all values of input. Since this is never the case for a practical log amp, the intercept refers to the value obtained by the minimum-error, straight-line fit to the actual graph of VOUT vs. input power. The quoted values assume a sinusoidal (CW) signal. Where there is complex modulation, as in CDMA, the calibration of the power response needs to be adjusted accordingly. Where a true power (waveform-independent) response is needed, the use of an rms-responding detector, such as the AD8361, should be considered.

However, in terms of the logarithmic slope, the amount by which the output VOUT changes for each decibel of input change (voltage or power), is, in principle, independent of waveform or termination impedance. In practice, it usually falls off at higher frequencies because of the declining gain of the amplifier stages and other effects in the detector cells. For the AD8312, the slope at low frequencies is nominally 21.0 mV/dB, falling almost linearly with frequency to about 18.6 mV/dB at 2.5 GHz. These values are sensibly independent of temperature and almost totally unaffected by supply voltages of 2.7 V to 5.5 V.

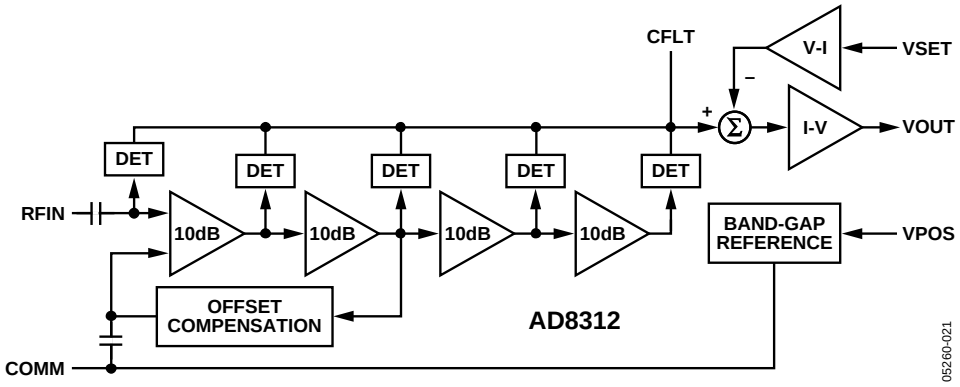


Figure 21. Block Schematic

APPLICATIONS

BASIC CONNECTIONS

Figure 22 shows the basic connections for measurement mode. A supply voltage of 2.7 V to 5.5 V is required. The supply to the VPOS pin should be decoupled with a low inductance 0.1 μF surface-mount ceramic capacitor. A series resistor of about 10 Ω may be added; this resistor slightly reduces the supply voltage to the AD8312 (maximum current into the VPOS pin is approximately 5.7 mA). Its use should be avoided in applications where the power supply voltage is very low (that is, 2.7 V). A series inductor provides similar power supply filtering with minimal drop in supply voltage.

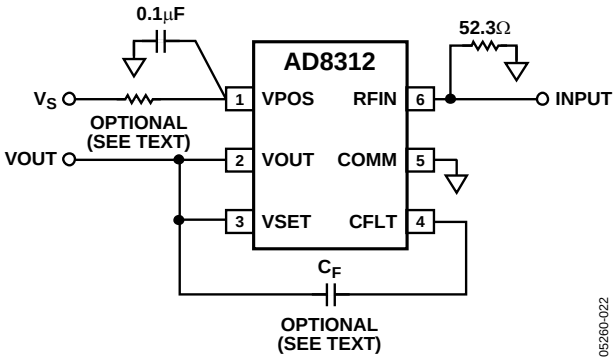


Figure 22. Basic Connections for Operation in Measurement Mode

The AD8312 has an internal input coupling capacitor. This eliminates the need for external ac coupling. In this example, a broadband input match is achieved by connecting a 52.3 Ω resistor between RFIN and ground. This resistance combines with the internal input impedance of approximately 3 kΩ to give an overall broadband input resistance of 50 Ω. Several other coupling methods are possible; these are described in the Input Coupling Options section.

The measurement mode is selected by connecting VSET to VOUT, which establishes a feedback path and sets the logarithmic slope to its nominal value. The peak voltage range of the measurement extends from −49 dBm to 0 dBm at 0.9 GHz and is only slightly less at higher frequencies up to 2.5 GHz. At a slope of 21.0 mV/dB, this would amount to an output span of 1.029 V. Figure 23 shows the transfer function for VOUT at a supply voltage of 2.7 V and an input frequency of 900 MHz.

The load resistance on VOUT should not be lower than 4 kΩ so that the full-scale output can be generated with the limited available current of 1 mA maximum. Figure 23 shows the logarithmic conformance under the same conditions.

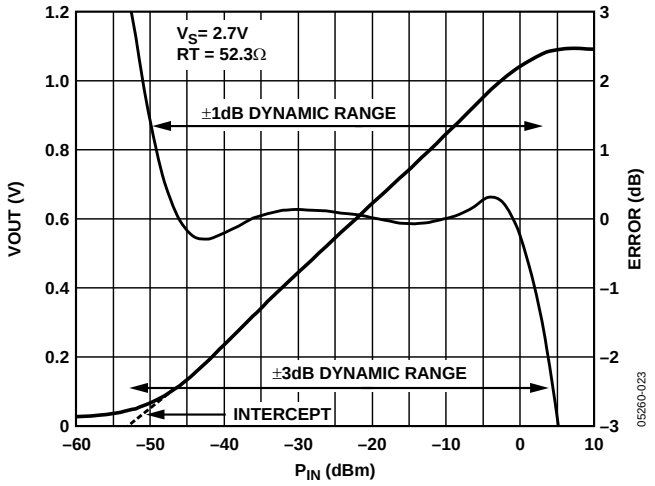


Figure 23. VOUT and Log Conformance Error vs. Input Level vs. Input Level at 900 MHz

TRANSFER FUNCTION IN TERMS OF SLOPE AND INTERCEPT

The transfer function of the AD8312 is characterized in terms of its slope and intercept. The logarithmic slope is defined as the change in the RSSI output voltage for a 1 dB change at the input. For the AD8312, the slope is nominally 20 mV/dB. Therefore, a 10 dB change at the input results in a change at the output of approximately 200 mV. Figure 23 shows the range over which the device maintains its constant slope. The dynamic range can be defined as the range over which the error remains within a certain band, usually ±1 dB or ±3 dB. In Figure 23, for example, the ±1 dB dynamic range is approximately 51 dB (from −49 dBm to +2 dBm).

The intercept is the point at which the extrapolated linear response would intersect the horizontal axis (see Figure 23). Using the slope and intercept, the output voltage can be calculated for any input level within the specified input range by

$$VOUT = V_{SLOPE} \times (P_{IN} - P_O)$$

where:

VOUT is the demodulated and filtered RSSI output.

V_{SLOPE} is the logarithmic slope, expressed in V/dB.

P_{IN} is the input signal, expressed in decibels relative to some reference level (dBm in this case).

P_O is the logarithmic intercept, expressed in decibels relative to the same reference level.

For example, at an input level of −27 dBm, the output voltage is

$$VOUT = 0.020 \text{ V/dB} \times [-27 \text{ dBm} - (-50 \text{ dBm})] = 0.46 \text{ V}$$

Filter Capacitor

The video bandwidth of VOUT is approximately 3.5 MHz. In CW applications where the input frequency is much higher than this, no further filtering of the demodulated signal is required. Where there is a low frequency modulation of the carrier amplitude, however, the low-pass corner must be reduced by the addition of an external filter capacitor, C_F (see Figure 22). The video bandwidth is related to C_F by

$$Video\ Bandwidth = \frac{1}{2\pi \times 13\ \text{k}\Omega \times (3.5\ \text{pF} + C_F)}$$

Input Coupling Options

The internal 5 pF coupling capacitor of the AD8312, along with the low frequency input impedance of 3 kΩ, gives a high-pass input corner frequency of approximately 16 MHz. This sets the minimum operating frequency. Figure 24 to Figure 26 show three options for input coupling. A broadband resistive match can be implemented by connecting a shunt resistor to ground at RFIN (see Figure 24). This 52.3 Ω resistor (other values can also be used to select different overall input impedances) combines with the input impedance of the AD8312 (2.9 kΩ || 1.3 pF) to give a broadband input impedance of 50 Ω. While the input resistance and capacitance (R_{IN} and C_{IN}) varies by approximately ±20% from device to device, the dominance of the external shunt resistor means that the variation in the overall input impedance is close to the tolerance of the external resistor.

At frequencies above 2 GHz, the input impedance drops below 450 Ω; therefore, it is appropriate to use a larger shunt resistor value. This value is calculated by plotting the input impedance (resistance and capacitance) on a Smith Chart and by choosing the best shunt resistor value to bring the input impedance closest to the center of the chart (see Figure 17). At 2.5 GHz, a shunt resistor of 57.6 Ω is recommended.

A reactive match can also be implemented as shown in Figure 25. This is not recommended at low frequencies because device tolerances dramatically vary the quality of the match due to the large input resistance. For low frequencies, Figure 24 or Figure 26 is recommended.

In Figure 25, the matching components are drawn as general reactances. Depending on the frequency, the input impedance at that frequency and the availability of standard value components, either a capacitor or an inductor, is used. As in the previous case, the input impedance at a particular frequency is plotted on a Smith Chart and matching components are chosen (Shunt or Series L, or Shunt or Series C) to move the impedance to the center of the chart. Matching components for specific frequencies can be calculated using the Smith Chart (see Figure 17). Table 5 outlines the input impedances for some commonly used frequencies.

The impedance matching characteristics of a reactive matching network provide voltage gain ahead of the AD8312, which increases device sensitivity (see Table 5). The voltage gain is calculated by

$$Voltage\ Gain_{\text{dB}} = 20 \log_{10} \sqrt{\frac{R2}{R1}}$$

where:

R2 is the input impedance of the AD8312.

R1 is the source impedance to which the AD8312 is being matched.

Note that this gain is only achieved for a perfect match. Component tolerances and the use of standard values tend to reduce gain.

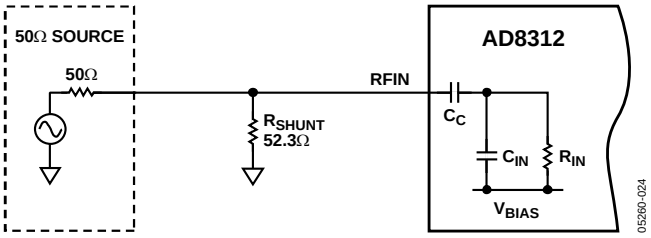


Figure 24. Broadband Resistive Method for Input Coupling

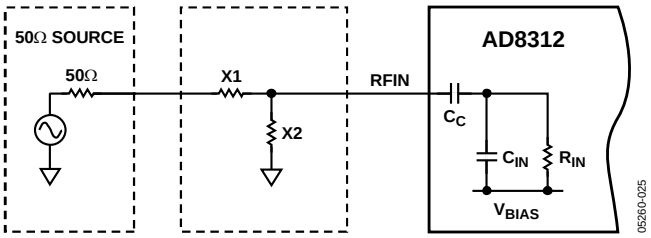


Figure 25. Narrow-Band Reactive Method for Input Coupling

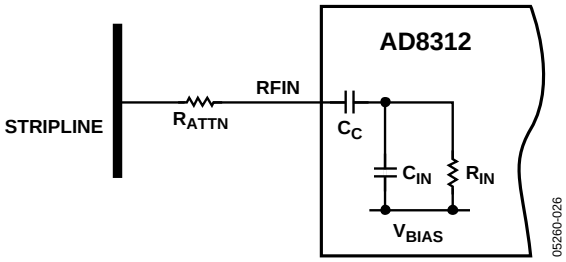


Figure 26. Series Attenuation Method for Input Coupling

Figure 26 shows a third method for coupling the input signal into the AD8312, which is applicable in applications where the input signal is larger than the input range of the log amp. A series resistor, connected to the RF source, combines with the input impedance of the AD8312 to resistively divide the input signal being applied to the input. This has the advantage of very little power being tapped off in RF power transmission applications.

Table 5. Input Impedance for Select Frequency

Frequency	S11		Impedance Ω
(GHz)	Real	Imaginary	(Series)
0.05	0.967	−0.043	1090 – j 1461
0.1	0.962	−0.081	422.6 – j 1015
0.9	0.728	−0.535	25.6 – j 148.5
1.9	0.322	−0.891	11.5 – j 72.69
2.2	0.230	−0.832	9.91 – j 64.74
2.5	0.165	−0.845	9.16 – j 59.91
3.0	0.126	−0.849	8.83 – j 57.21
3.5	0.146	−0.826	10.5 – j 58.54

Increasing the Logarithmic Slope

The nominal logarithmic slope of 20 mV/dB can be increased to an arbitrarily high value by attenuating the signal between VOUT and VSET, as shown in Figure 27. The ratio R1/R2 is set by

$$R1/R2 = \left(\frac{New\ Slope}{Original\ Slope} \right) - 1$$

In the example shown, two 2 kΩ resistors combine to change the slope at 1900 MHz from approximately 20 mV/dB to 40 mV/dB. Note that R2 is in parallel with the input resistance of VSET, typically 13 kΩ. Therefore, the exact R1/R2 ration may vary.

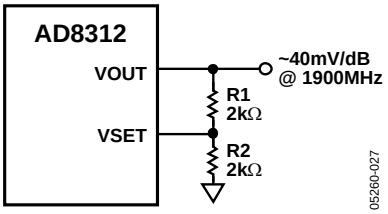


Figure 27. Increasing the Output Slope

The slope can be increased to higher levels, as shown in Figure 28. This, however, reduces the usable dynamic range of the device, depending on the supply voltage.

Output loading should be considered when choosing resistor values for slope adjustment to ensure proper output swing. Note that the load resistance on VOUT should not be lower than 4 kΩ in order that the full-scale output can be generated with the limited available current of 1 mA.

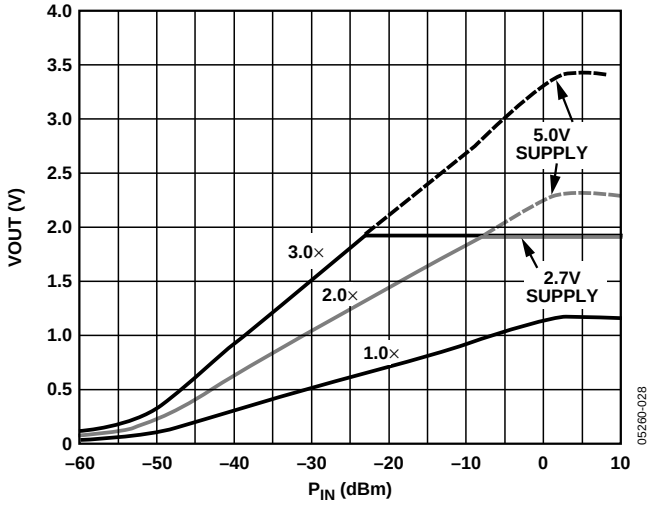


Figure 28. VOUT vs. Input Level at Various Logarithmic Slopes

Effect of Waveform Type on Intercept

Although specified for input levels in dBm (dB relative to 1 mW), the AD8312 fundamentally responds to voltage and not to power. A direct consequence of this characteristic is that input signals of equal rms power but differing crest factors, produce different results at the log amplifier's output.

The effect of differing signal waveforms is to shift the effective value of the intercept upwards or downwards. Graphically, this looks like a vertical shift in the log amplifier's transfer function. The logarithmic slope, however, is not affected. For example, consider the case of the AD8312 being alternately fed by an unmodulated sine wave and by a 64 QAM signal of the same rms power. The AD8312's output voltage differs by the equivalent of 1.6 dB (31 mV) over the complete dynamic range of the device (with the output for a 64 QAM input being lower).

Figure 29 shows the transfer function of the AD8312 when driven by both an unmodulated sine wave and several different signal waveforms. For precision operation, the AD8312 should be calibrated for each signal type that is driving it. To measure the rms power of a 64 QAM input, for example, the mV equivalent of the dB value (19.47 mV/dB × 1.6 dB) should be subtracted from the output voltage of the AD8312.

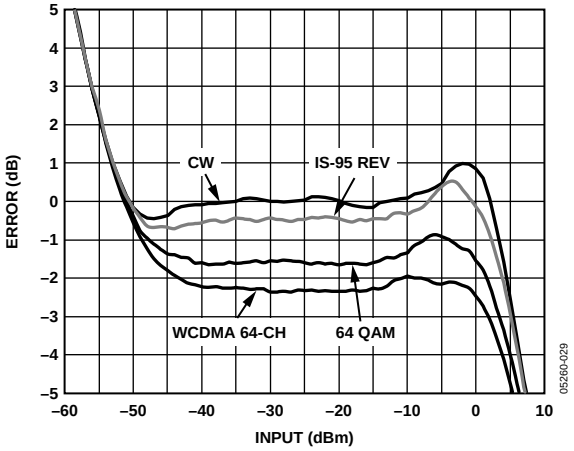


Figure 29. Shift in Transfer Function due to Several Different Signal Waveforms

Temperature Drift

Figure 30 shows the log slope and error over temperature for a 0.9 GHz input signal. Error due to drift over temperature consistently remains within ±0.5 dB and only begins to exceed this limit when the ambient temperature goes above 70°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

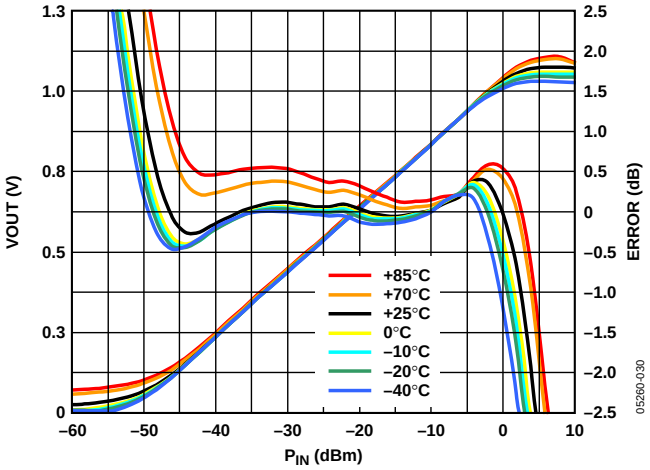


Figure 30. Typical Drift at 900 GHz for Various Temperatures

Operation Above 2.5 GHz

The AD8312 works at high frequencies, but exhibits slightly higher output voltage temperature drift. Figure 31 and Figure 32 show the transfer functions and error distributions of a large population of devices at 3.0 GHz and 3.5 GHz over temperature. Due to the repeatability of the drift from part-to-part, compensation can be applied to reduce the effects of temperature drift. In the case of the 3.5 GHz distribution, an intercept correction of 2.0 dB at 85°C would improve the accuracy of the distribution to ±2 dB over a +40 dB range.

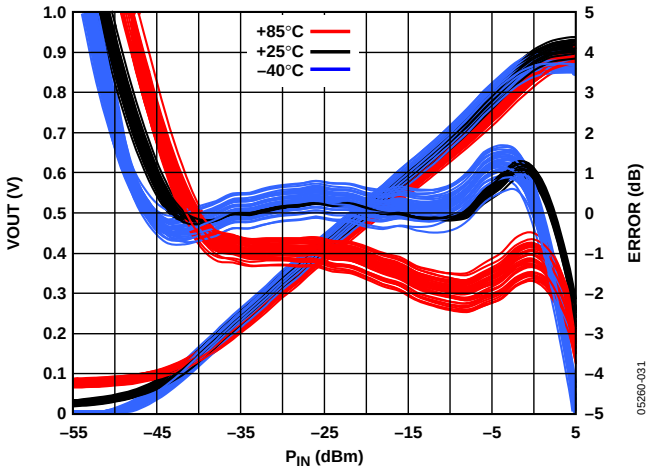


Figure 31.Output Voltage and Error at –40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 3.0 GHz for 60 Devices

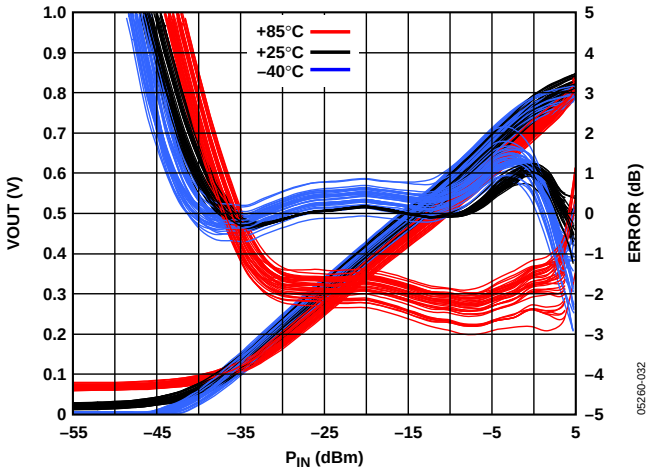


Figure 32. Output Voltage and Error at –40°C, +25°C, and +85°C After Ambient Normalization vs. Input Amplitude at 3.5 GHz for 30 Devices

Device Handling

The wafer-level chip scale package consists of solder bumps connected to the active side of the die. The part is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP package can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 application note for additional information. WLCSP devices are bumped die, and exposed die can be sensitive to light condition, which can influence specified limits.

Evaluation Board

Figure 33 shows the schematic of the AD8312 evaluation board. The layout and silkscreen of the component and circuit sides are shown in Figure 34 to Figure 37. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by a single 0.1 µF capacitor.

Table 6 details the various configuration options of the evaluation board.

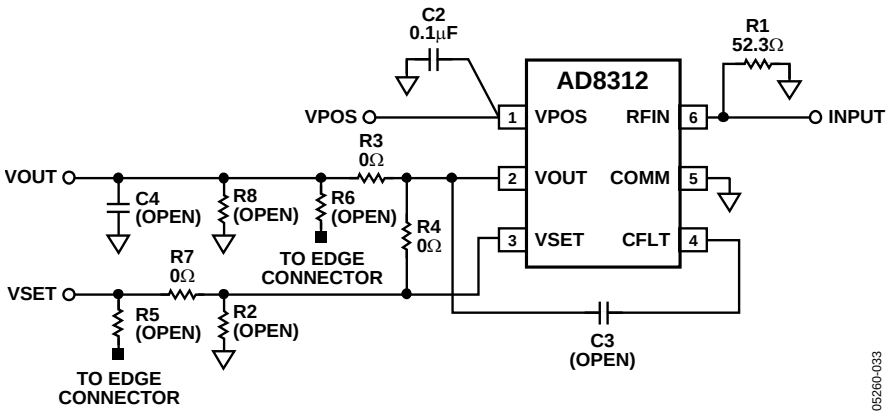


Figure 33. Evaluation Board Schematic

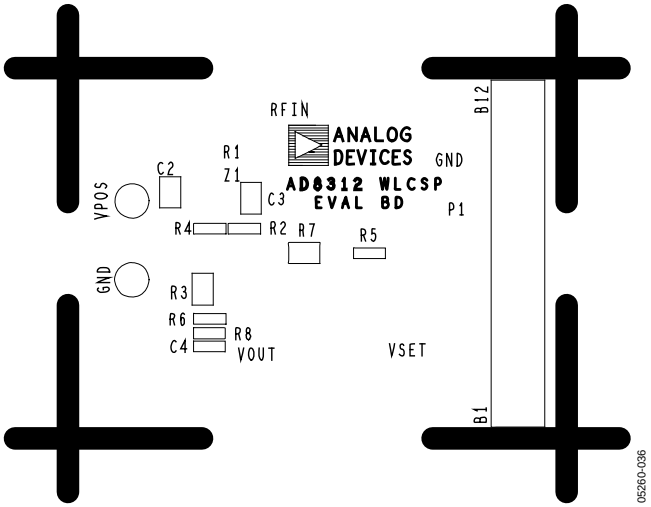


Figure 34. Silkscreen of Component Side (WLCSP)

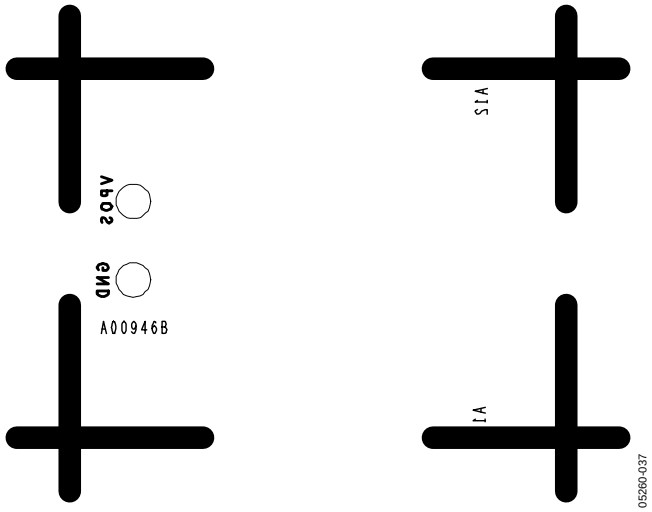


Figure 36. Silkscreen of Circuit Side (WLCSP)

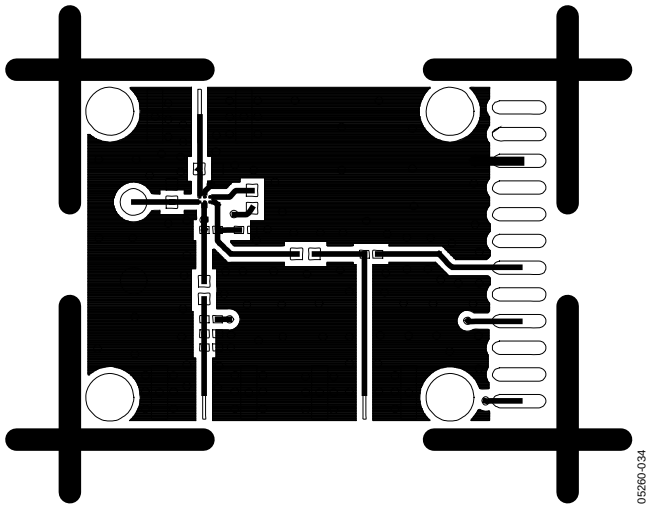


Figure 35. Layout of Component Side (WLCSP)

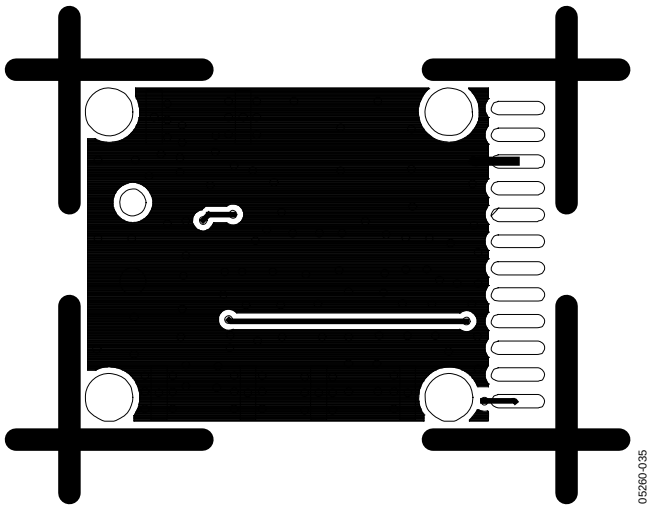


Figure 37. Layout of Circuit Side (WLCSP)

Table 6. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Supply and Ground Vector Pins.	Not Applicable
C2	Power Supply Decoupling. The nominal supply decoupling consists of a 0.1 µF capacitor (C1).	C2 = 0.1 µF (Size 0603)
R1	Input Interface. The 52.3 Ω resistor in Position R1 combines with the AD8312's internal input impedance to give a broadband input impedance of around 50 Ω.	R1 = 52.3 Ω (Size 0603)
R2, R4	Slope Adjust. By installing resistors in R2 and R4, the nominal slope of 20 mV/dB can be changed. See the Increasing the Logarithmic Slope section for more details.	R2 = Open (Size 0402) R4 = 0 Ω (Size 0402)
C3	Filter Capacitor. The response time of VOUT can be modified by placing a capacitor between CFLT (Pin 4) and VOUT (Pin 2).	C3 = Open (Size 0603)
R3, R8, C4	Output Interface. R3, R8, and C4 can be used to check the response of VOUT to capacitive and resistive loading. R3/R8 can be used to attenuate VOUT.	R3 = 0 Ω (Size 0603) R8 = C4 = Open (Size 0402)
R7	VSET Interface. R7 can be used to reduce capacitive loading from transmission lines.	R7 = 0 Ω (Size 0603)
R5, R6	Alternate Interface. R5 and R6 allow for VOUT and VSET to be accessible from the edge connector, which is only used for characterization.	R5 = R6 = Open (Size 0402)

OUTLINE DIMENSIONS

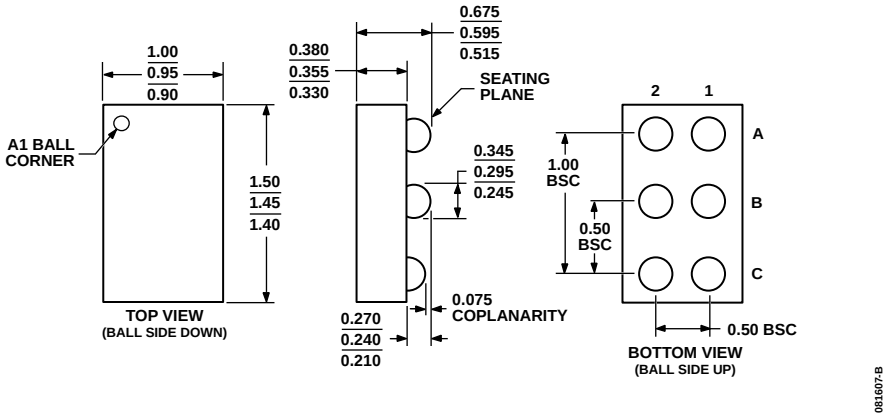


Figure 38. 6-Ball Wafer-Level Chip Scale Package [WLCSP]
(CB-6-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Outline	Branding Information	Ordering Quantity
AD8312ACBZ-P7	–40°C to +85°C	6-Ball WLCSP, 7″ Pocket Tape and Reel	CB-6-2	Q00	3000
AD8312ACBZ-P2	–40°C to +85°C	6-Ball WLCSP, 7″ Pocket Tape and Reel	CB-6-2	Q00	250
AD8312-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

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D05260–0–1/11(A)

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