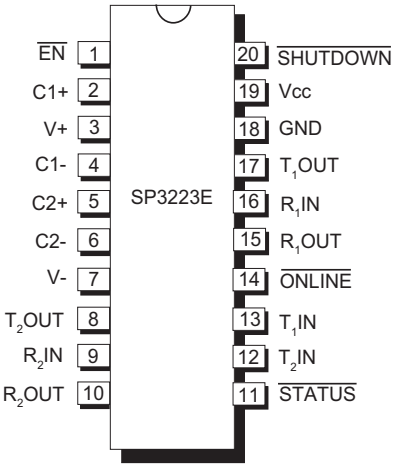
SP3223E/EB/EU

Intelligent +3.0V to +5.5V RS-232 Transceivers

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- AUTO ON-LINE® circuitry automatically wakes up from a 1µA shutdown
- Minimum 250Kbps data rate under load (EB)
- 1 Mbps data rate for high speed RS-232 (EU)
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- ESD Specifications:
  - ±15KV Human Body Model
  - ±15KV IEC61000-4-2 Air Discharge
  - ±8KV IEC61000-4-2 Contact Discharge



Now Available in Lead Free Packaging

DESCRIPTION

The **SP3223** products are RS-232 transceiver solutions intended for portable applications such as notebook and hand held computers. These products use an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and **Exar's** driver architecture allow the **SP3223** series to deliver compliant RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The **SP3223** is a 2-driver/2-receiver device ideal for laptop/notebook computer and PDA applications.

The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shut-down state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1µA.

SELECTION TABLE

Device	Power Supplies	RS- 232 Drivers	RS-232 Receivers	AUTO ON-LINE ®	TTL 3-state	Data Rate (kbps)
SP3223E	+3.0V to +5.5V	2	2	YES	YES	120
SP3223EB	+3.0V to +5.5V	2	2	YES	YES	250
SP3223EU	+3.0V to +5.5V	2	2	YES	YES	1000

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages
TxIN, $\overline{\text{ONLINE}}$,
$\overline{\text{SHUTDOWN}}$, EN.....-0.3V to Vcc + 0.3V
RxIN.....±15V

Output Voltages
TxOUT.....±13.2V
RxOUT, $\overline{\text{STATUS}}$.....-0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package

20-pin SSOP (derate 9.25mW/°C above +70°C)..750mW
20-pin TSSOP (derate 11.1mW/°C above +70°C..900mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C (Note 2).

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS Supply Current, AUTO ON-LINE®		1.0	10	µA	All RxIN open, $\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = Vcc, TxIN = Vcc or GND, Vcc = +3.3V, T_{AMB} = +25ºC
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{SHUTDOWN}}$ = GND, TxIN = Vcc or GND, Vcc = +3.3V, T_{AMB} = +25ºC
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}}$ = $\overline{\text{SHUTDOWN}}$ = Vcc, No Load, Vcc = +3.3V, T_{AMB} = +25ºC
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 GND 2.0		 0.8 Vcc	V	Vcc = 3.3V or 5.0V, TxIN, $\overline{\text{EN}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{ONLINE}}$
Input Leakage Current		+/-0.01	+/-1.0	µA	TxIN, $\overline{\text{EN}}$, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, T_{AMB} = +25ºC, Vin = 0V to Vcc
Output Leakage Current		+/-0.05	+/-10	µA	Receivers disabled, Vout = 0V to Vcc
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	Vcc - 0.6	Vcc - 0.1		V	I_{OUT} = -1.0mA

NOTE 2: C1 - C4 = 0.1µF, tested at 3.3V ±10%.
C1 = 0.047µF, C2-C4 = 0.33µF, tested at 5V±10%.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C (Note 2).

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Driver Outputs Output Voltage Swing	+/-5.0	+/-5.4		V	All Driver outputs loaded with 3kΩ to GND, T_{AMB} = +25ºC
Output Resistance	300			Ω	Vcc = V+ = V- = 0V, Vout = +/-2V
Output Short-Circuit Current		+/-35	+/-60	mA	Vout = 0V
Output Leakage Current			+/-25	µA	Vcc = 0V or 3.0V to 5.5V, Vout = +/-12V, Driver disabled
RECEIVER INPUTS Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.6	1.2		V	Vcc = 3.3V
Input Threshold LOW	0.8	1.5		V	Vcc = 5.0V
Input Threshold HIGH		1.5	2.4	V	Vcc = 3.3V
Input Threshold HIGH		1.8	2.4	V	Vcc = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k Ω	
AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = Vcc)					
$\overline{\text{STATUS}}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{\text{STATUS}}$ Output Voltage HIGH	Vcc - 0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{ONLINE})		200		µs	Figure 15
Receiver Positive or Negative Threshold to $\overline{\text{STATUS}}$ HIGH (t_{STSH})		0.5		µs	Figure 15
Receiver Positive or Negative Threshold to $\overline{\text{STATUS}}$ LOW (t_{STSL})		20		µs	Figure 15

NOTE 2: C1 - C4 = 0.1µF, tested at 3.3V ±10%.
C1 = 0.047µF, C2-C4 = 0.33µF, tested at 5V±10%.

TIMING CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Maximum Data Rate					
SP3223E	120	235		kbps	RL = 3kΩ, C_L = 1000pF, One Driver active
SP3223EB	250				
SP3223EU	1000				RL = 3kΩ, C_L = 250pF, One Driver active
Receiver Propagation Delay					
t_{PHL} and t_{PLH}		0.15		µA	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal Operation
Receiver Output Disable Time		200		ns	Normal Operation
Driver Skew					
E, EB		100	500	ns	$\lvert t_{PHL} - t_{PLH} \rvert$, T_{AMB} = 25°C
EU		50	100	ns	
Receiver Skew					
E, EB, EU		200	1000	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate					
E, EB			30	V/µs	Vcc = 3.3V, RL = 3kΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V
EU		90			

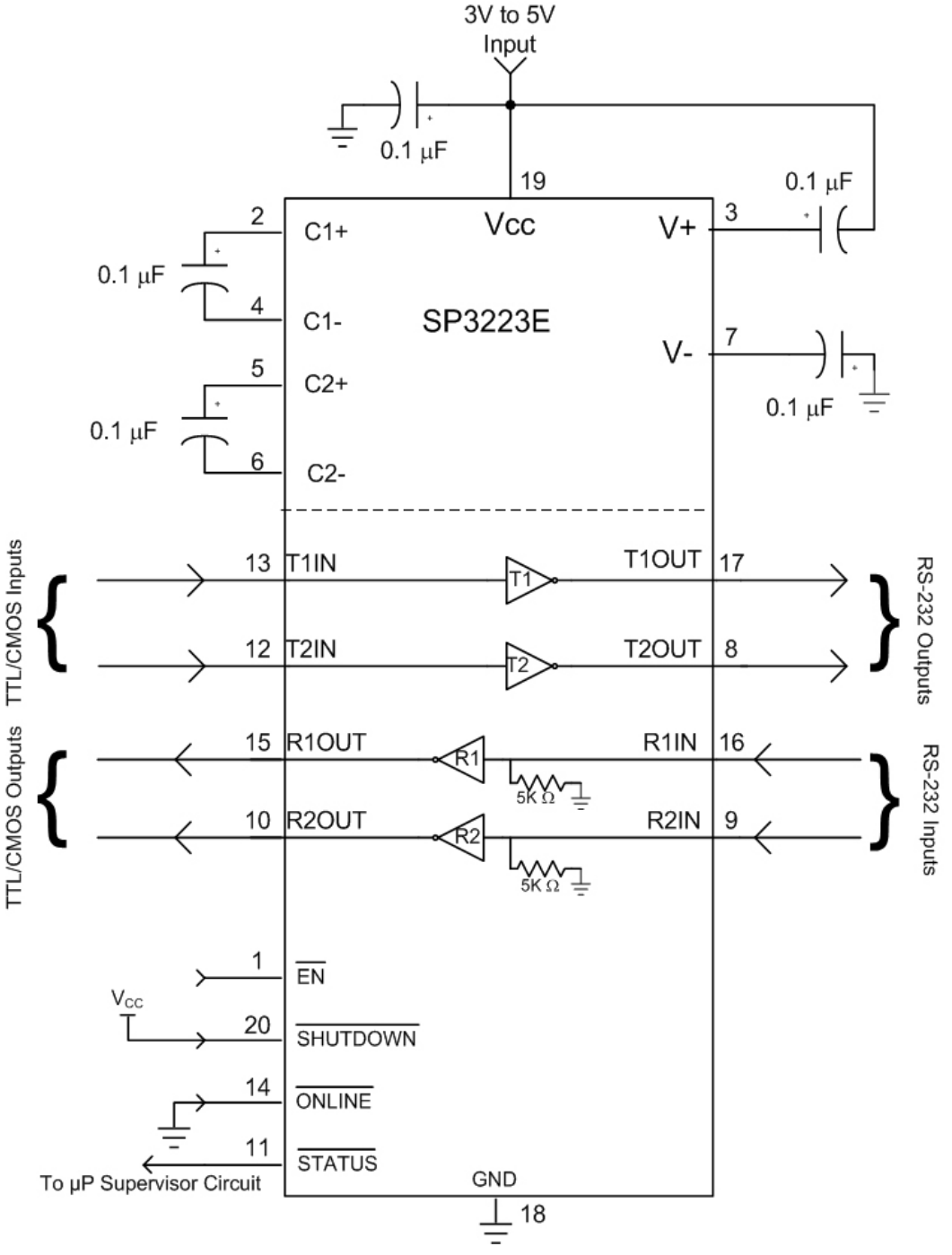


Figure 1. SP3223E Typical Operating Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 250Kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

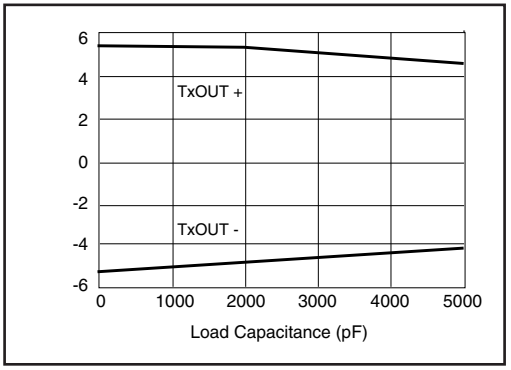


Figure 2. Transmitter Output Voltage VS. Load Capacitance for the SP3223EB

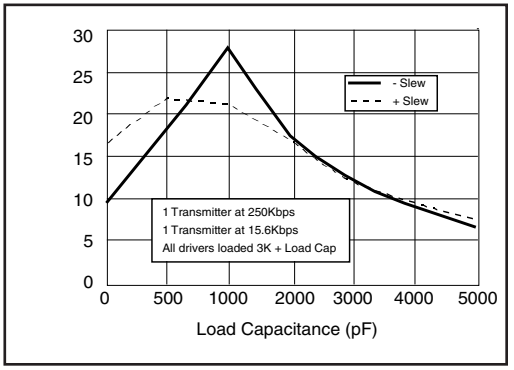


Figure 3. Slew Rate VS. Load Capacitance for the SP3223EB

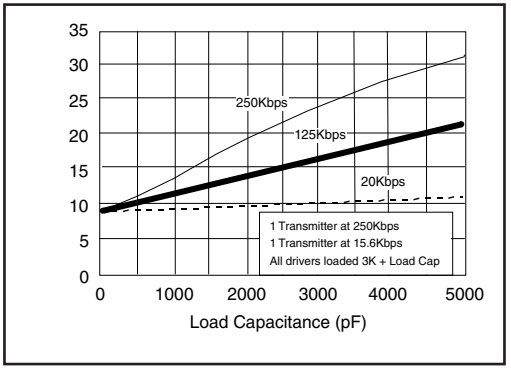


Figure 4. Supply Current VS. Load Capacitance when Transmitting Data for the SP3223EB

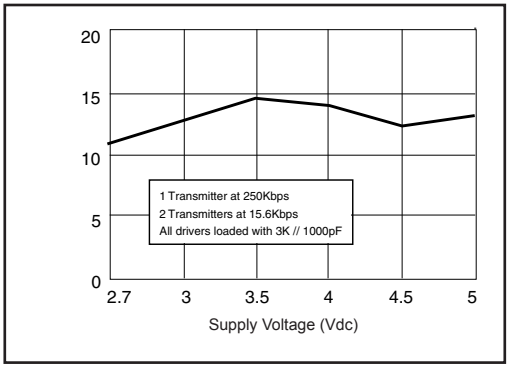


Figure 5. Supply Current VS. Supply Voltage for the SP3223EB

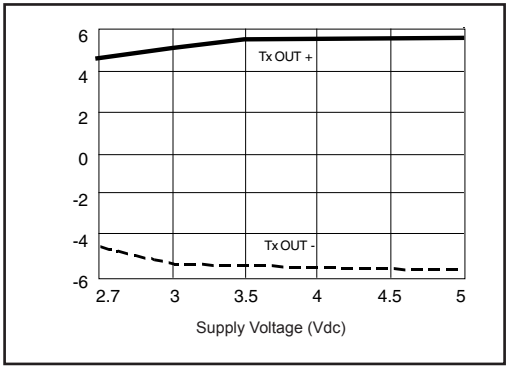


Figure 6. Transmitter Output Voltage VS. Supply Voltage for the SP3223EB

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000Kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

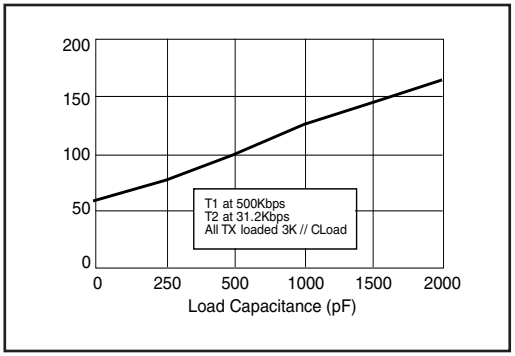


Figure 7. Transmitter Skew VS. Load Capacitance for the SP3223EU

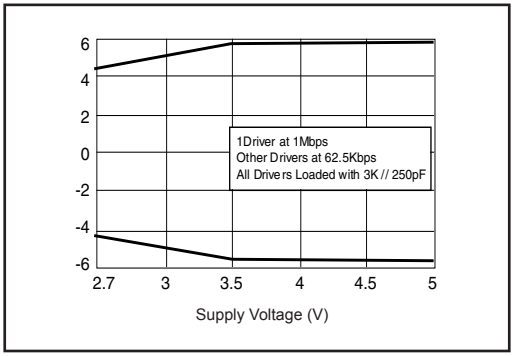


Figure 8. Transmitter Output Voltage VS. Supply Voltage for the SP3223EU

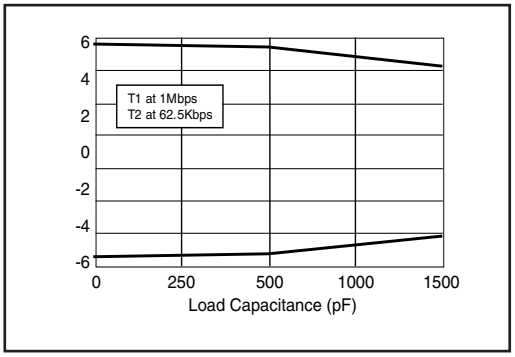


Figure 9. Transmitter Output Voltage VS. Load Capacitance for the SP3223EU

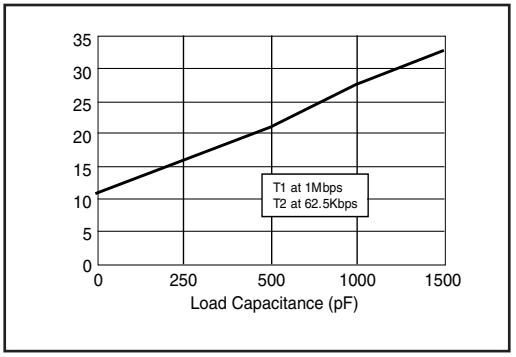


Figure 10. Supply Current VS. Load Capacitance for the SP3223EU

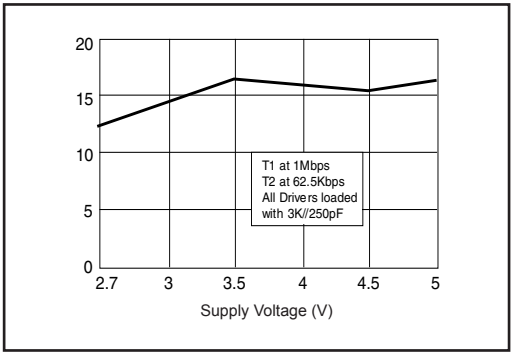


Figure 11. Supply Current VS. Supply Voltage for the SP3223EU

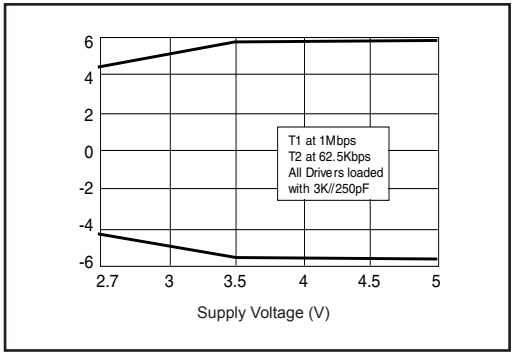


Figure 12. Transmitter Output Voltage VS. Supply Voltage for the SP3223EU

Name	Function	Pin #
$\overline{EN}$	Receiver Enable, Apply logic LOW for normal operation. Apply logic HIGH to disable receiver outputs (high-Z state).	1
C1+	Positive terminal of the voltage doubler charge-pump capacitor	2
V+	Regulated +5.5V output generated by charge pump	3
C1-	Negative terminal of the voltage doubler charge-pump capacitor	4
C2+	Positive terminal of the inverting charge-pump capacitor	5
C2-	Negative terminal of the inverting charge-pump capacitor	6
V-	Regulated -5.5V output generated by charge pump	7
T_2OUT	RS-232 Driver output	8
R_2IN	RS-232 receiver input	9
R_2OUT	TTL/CMOS receiver output	10
$\overline{STATUS}$	TTL/CMOS output indicating online and shutdown status	11
T_2IN	TTL/CMOS driver input	12
T_1IN	TTL/CMOS driver input	13
$\overline{ONLINE}$	Apply logic HIGH to override AUTO ON-LINE ® circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to table 2).	14
R_1OUT	TTL/CMOS receiver output	15
R_1IN	RS-232 receiver input	16
T_1OUT	RS-232 Driver output	17
GND	Ground	18
Vcc	+3.0V to +5.5V supply voltage	19
$\overline{SHUTDOWN}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE ® circuitry and $\overline{ONLINE}$ (refer to table 2).	20

Table 2. Pin Description

DESCRIPTION

The **SP3223** is a 2-driver/2-receiver device ideal for portable or handheld applications. The **SP3223** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or handheld applications such as notebook or handheld computers. The **SP3223** devices feature **Exar's** proprietary on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply.

These devices are an ideal choice for power sensitive designs. Featuring ***AUTO ON-LINE®*** circuitry, the **SP3223** reduces the power supply drain to a 1µA supply current. In many portable or handheld applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

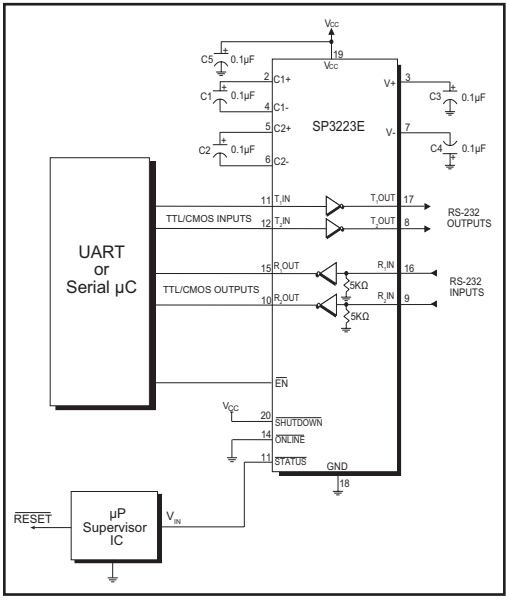


Figure 13. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

THEORY OF OPERATION

The **SP3223** series is made up of four basic circuit blocks:
1. Drivers, 2. Receivers, 3. The Exar proprietary charge pump, and 4. ***AUTO ON-LINE®*** circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. Unused driver inputs should be connected to GND or V_{CC}.

The drivers can guarantee output data rates fully loaded with 3kΩ in parallel with 1000pF, (SP3223EU, C_L = 250pF) ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output on the E and EB versions is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The Slew Rate of EU version is not limited to enable higher speed data transfers. The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 14 shows a loopback test circuit used to test the RS-232 Drivers. *Figure 15* shows the test results where one driver was active at 250kbps and all drivers are loaded with an RS-232 receiver in parallel with a 1000pF capacitor. RS-232 data transmission rate of 120kbps to 1Mbps provide compatibility with designs in personal computer peripherals and LAN applications.

Device: SP3223			
$\overline{SHUTDOWN}$	$\overline{EN}$	T_XOUT	R_XOUT
0	0	High Z	Active
0	1	High Z	High Z
1	0	Active	Active
1	1	Active	High Z

Table 3. $\overline{SHUTDOWN}$ and $\overline{EN}$ Truth Tables
Note: In AUTO $\overline{ON}$-LINE® Mode where $\overline{ONLINE}$ = GND and $\overline{SHUTDOWN}$ = V_{CC}, the device will shut down if there is no activity present at the Receiver inputs.

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers have an inverting output that can be disabled by using the $\overline{EN}$ pin.

Receivers are active when the AUTO ON-LINE® circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100µs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1µA. Driving $\overline{EN}$ to a logic HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the **SP3223** driver and receiver outputs can be found in *Table 2*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pull-down resistor to ground will commit the output of the receiver to a HIGH state.

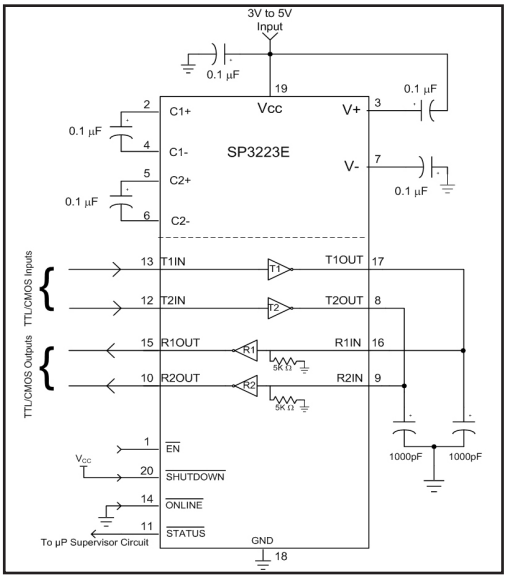


Figure 14. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

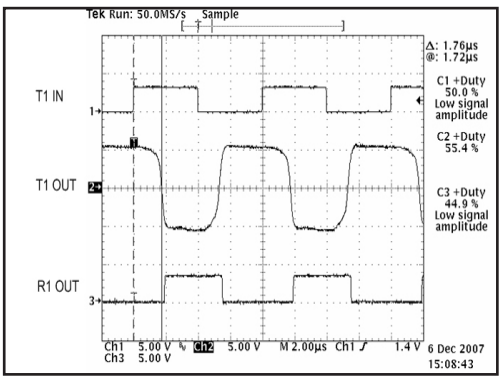


Figure 15. Loopback Test Circuit result at 250Kbps (All Drivers Fully Loaded)

Charge Pump

The charge pump uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of +/-5.5V regardless of input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1
— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2
— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3
— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4
— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is switched to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The Exar charge pump is designed to operate reliably with a range of low cost capacitors. Either polarized or non polarized capacitors may be used. If polarized capacitors are used they should be oriented as shown in the Typical Operating Circuit. The V+ capacitor may be connected to either ground or Vcc (polarity reversed.)

The charge pump operates with 0.1µF capacitors for 3.3V operation. For other supply voltages, see table 4 for required capacitor values. Do not use values smaller than those listed. Increasing the capacitor values (e.g., by doubling in value) reduces ripple on the transmitter outputs and may slightly reduce power consumption. C2, C3, and C4 can be increased without changing C1's value.

For best charge pump efficiency locate the charge pump and bypass capacitors as close as possible to the IC. Surface mount capacitors are best for this purpose. Using capacitors with lower equivalent series resistance (ESR) and self-inductance, along with minimizing parasitic PCB trace inductance will optimize charge pump operation. Designers are also advised to consider that capacitor values may shift over time and operating temperature.

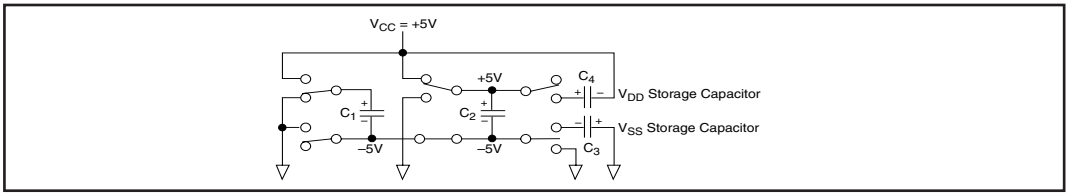


Figure 16. Charge Pump - Phase 1

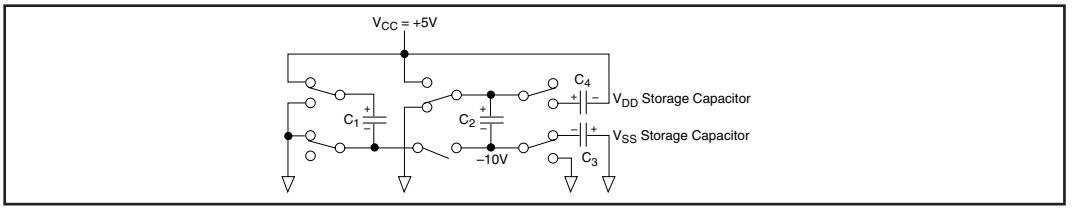


Figure 17. Charge Pump - Phase 2

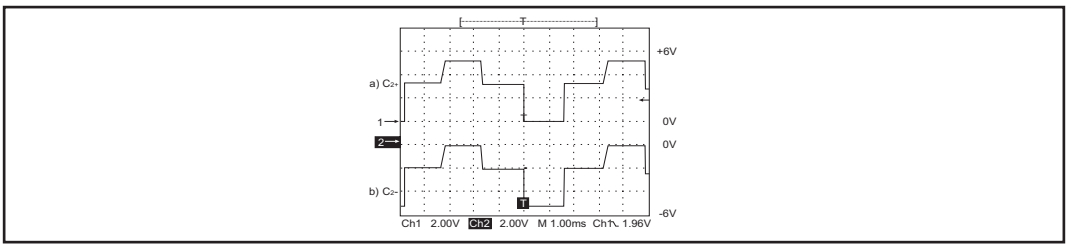


Figure 18. Charge Pump Waveforms

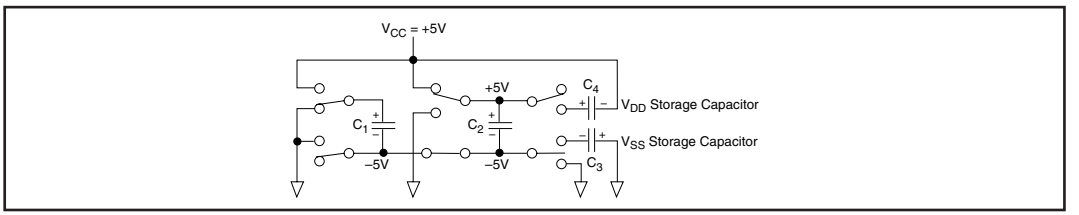


Figure 19. Charge Pump - Phase 3

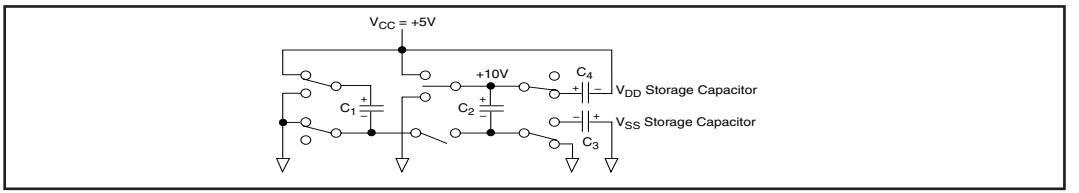


Figure 20. Charge Pump - Phase 4

Minimum recommended charge pump capacitor value	
Input Voltage V_{CC}	Charge pump capacitor value
3.0V to 3.6V	C1 - C4 = 0.1µF
4.5V to 5.5V	C1 = 0.047µF, C2-C4 = 0.33µF
3.0V to 5.5V	C1 - C4 = 0.22µF

Table 4. Minimum Charge Pump Capacitor values

AUTO ON-LINE® Circuitry

The **SP3223** device has **AUTO ON-LINE®** circuitry on board that saves power in applications such as laptop computers, PDA's, and other portable systems.

The **SP3223** device incorporates an **AUTO ON-LINE®** circuit that automatically enables itself when the external transmitter is enabled and the cable is connected. Conversely, the **AUTO ON-LINE®** circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1µA. This function is externally controlled by the ONLINE pin. When this pin is tied to a logic LOW, the **AUTO ON-LINE®** function is active. Once active, the device is enabled until there is no activity on receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitter at the other end of the cable with a ±5V minimum. When the external transmitter is disabled or the cable is disconnected, the receiver input will be pulled down by its internal 5kΩ resistor to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When the ONLINE pin is HIGH, the **AUTO ON-LINE®** mode is disabled.

The **AUTO ON-LINE®** circuit has two stages:

1) Inactive Detection
2) Accumulated Delay

The first stage, shown in Figure 22, detects an inactive input. A logic HIGH is asserted on R_XINACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R_XINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the **AUTO ON-LINE®** circuitry, shown in Figure 23, processes the receiver's R_XINACT signal with an accumulated delay that disables the device to a 1µA typical supply current. The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitter is disabled, or the $\overline{\text{SHUTDOWN}}$ pin is invoked. The typical accumulated delay is around 20µs. When the **SP3223** drivers and internal charge pump are disabled, the supply current is reduced to 1µA typical. This can commonly occur in handheld or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are truned off. The **AUTO ON-LINE®** mode can be disabled by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the **AUTO ON-LINE®** function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. Table 5 summarizes the logic of the **AUTO ON-LINE®** operating modes. The truth table logic of the **SP3223** driver and receiver outputs can be found in *Table 3.*

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitter is enabled and the cable is connected.

When the **SP3223** device is shutdown, the charge pumps are turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DTR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the **AUTO ON-LINE®** circuitry so this connection acts like a shutdown input pin

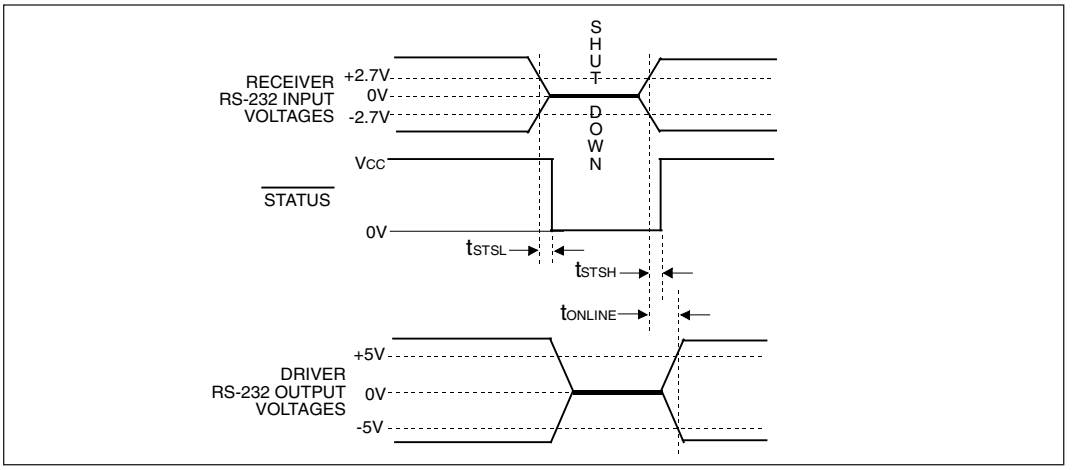


Figure 21. AUTO ON-LINE® Timing Waveforms

RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHUTDOWN}}$	$\overline{\text{ONLINE}}$	$\overline{\text{STATUS}}$	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation (AUTO ON-LINE©)
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown (AUTO ON-LINE©)
YES	LOW	HIGH/LOW	HIGH	Shutdown
NO	LOW	HIGH/LOW	LOW	Shutdown

Table 5. AUTO ON-LINE® Logic

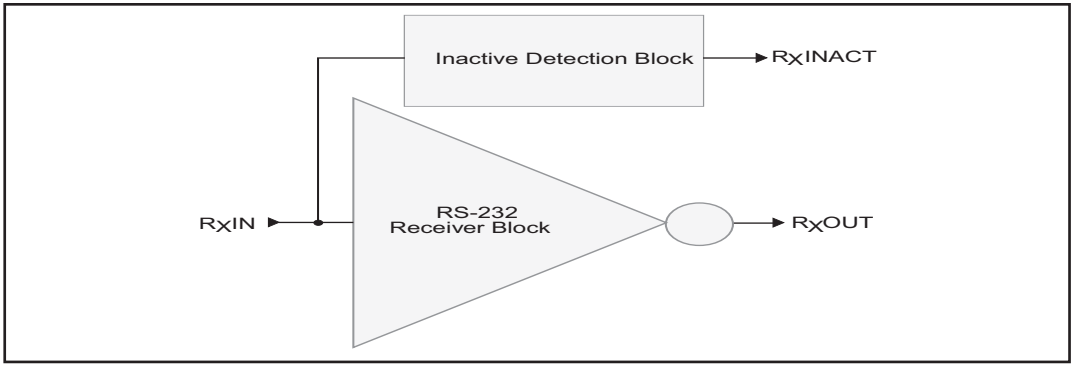


Figure 22. Stage I of AUTO ON-LINE® Circuitry

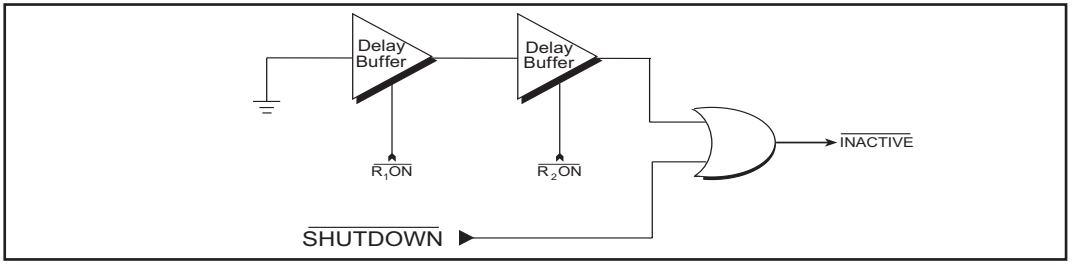


Figure 23. Stage II of AUTO ON-LINE® Circuitry

ESD TOLERANCE

The **SP3223** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC61000-4-2 Air-Discharge
c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 24. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 25. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method. With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

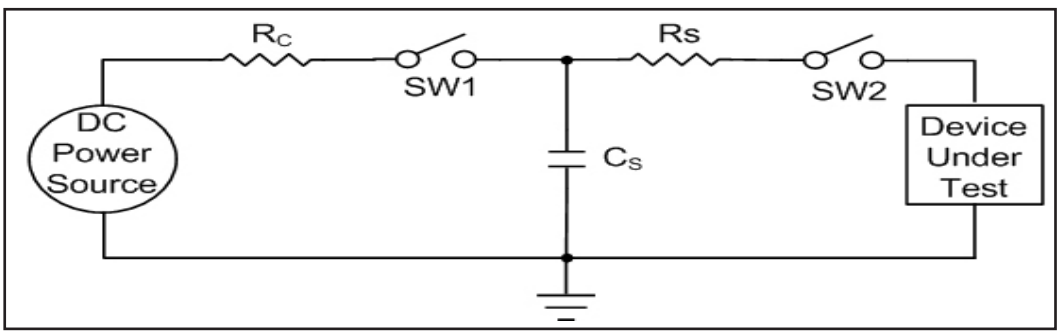


Figure 24. ESD Test Circuit for Human Body Model

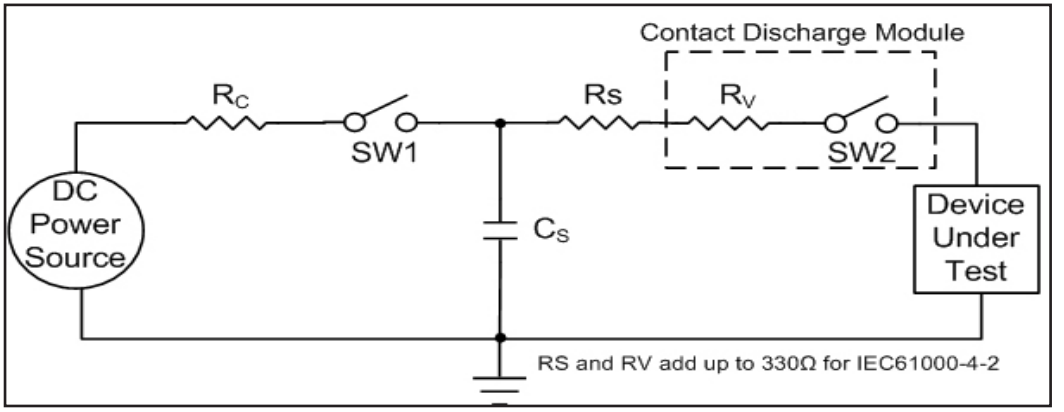


Figure 25. ESD Test Circuit for IEC61000-4-2

The circuit model in *Figures 24* and *25* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

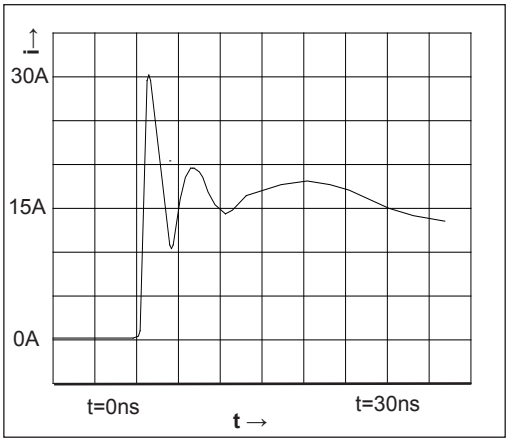
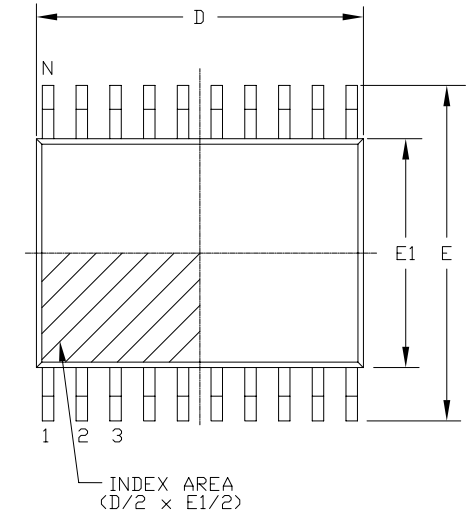


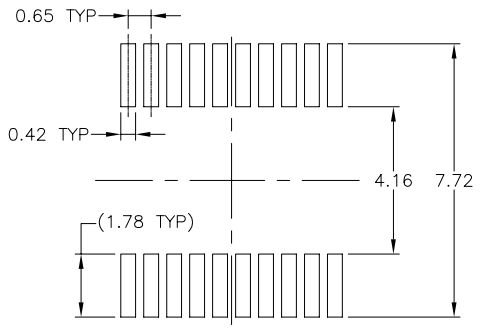
Figure 26. ESD Test Waveform for IEC61000-4-2

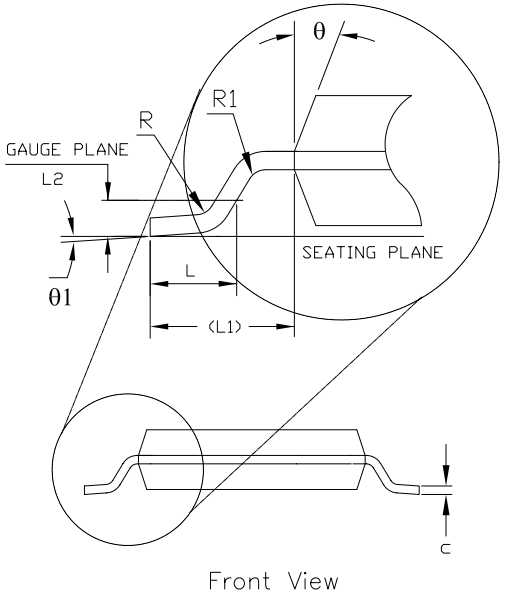
DEVICE PIN TESTED	HUMAN BODY MODEL	Air Discharge	IEC61000-4-2 Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

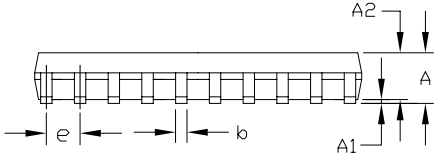
Table 6. Transceiver ESD Tolerance Levels

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/19/06	JL
B	ADD LAND PATTERN RECOMMENDATION	10/27/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL



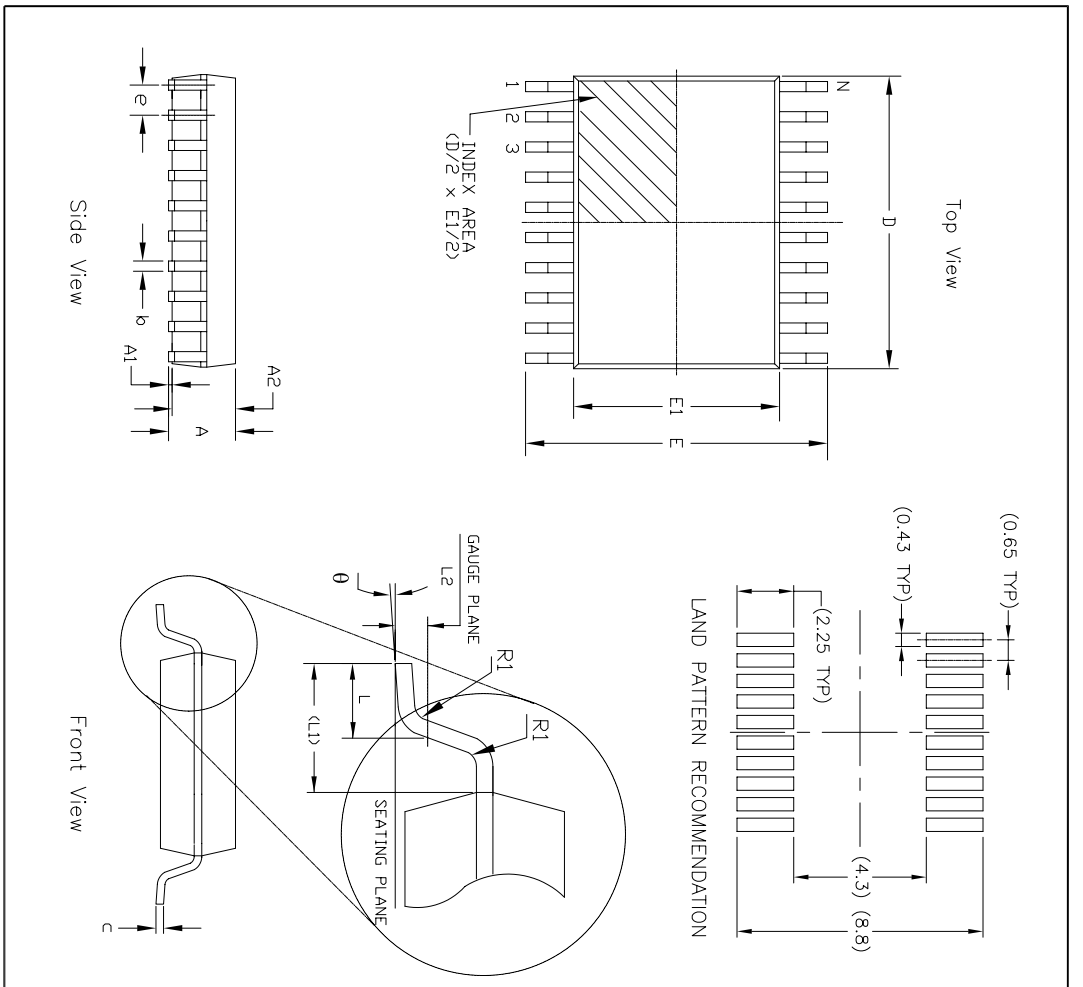






20 Pin TSSOP JEDEC MO-153 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	6.40	6.50	6.60	0.252	0.256	0.260
N	20			20		

EXAR Powering Connectivity	EXAR CORPORATION		
	20 PIN TSSOP PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 20-PIN TSSOP		
By: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1



REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A.	DRAWING ORIGINATION	04/24/06	JL
B	ADD LAND PATTERN RECOMMENDATION	07/25/07	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

20 Pin SSOP JEDEC MO-150 Variation AE

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65 BSC			0.026 BSC	
L	0.55	0.75	0.95	0.022	0.030	0.037
L1		1.25 REF			0.049 REF	
L2		0.25 BSC			0.010 BSC	
R1	0.09	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
D	6.90	7.20	7.50	0.272	0.283	0.295
N		20			20	

EXAR CORPORATION

20 PIN SSOP PACKAGE OUTLINE

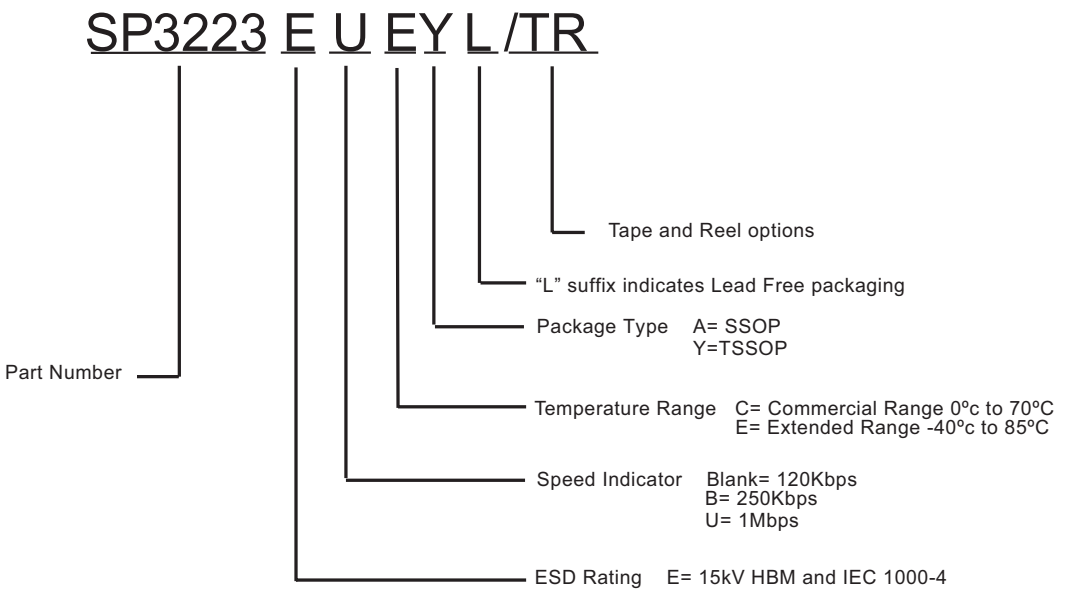
Packaging Approval:		Drawing No:	20-PIN SSOP
By: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1

ORDERING INFORMATION

Part Number	Temperature Range	Package Types
SP3223EBCA-L	0°C to +70°C	20-pin SSOP
SP3223EBCA-L/TR	0°C to +70°C	20-pin SSOP
SP3223EBCY-L	0°C to +70°C	20-pin TSSOP
SP3223EBCY-L/TR	0°C to +70°C	20-pin TSSOP
SP3223EBEA-L	-40°C to +85°C	20-pin SSOP
SP3223EBEA-L/TR	-40°C to +85°C	20-pin SSOP
SP3223EBEY-L	-40°C to +85°C	20-pin TSSOP
SP3223EBEY-L/TR	-40°C to +85°C	20-pin TSSOP
SP3223ECA-L	0°C to +70°C	20-pin SSOP
SP3223ECA-L/TR	0°C to +70°C	20-pin SSOP
SP3223ECY-L	0°C to +70°C	20-pin TSSOP
SP3223ECY-L/TR	0°C to +70°C	20-pin TSSOP
SP3223EEA-L	-40°C to +85°C	20-pin SSOP
SP3223EEA-L/TR	-40°C to +85°C	20-pin SSOP
SP3223EEY-L	-40°C to +85°C	20-pin TSSOP
SP3223EEY-L/TR	-40°C to +85°C	20-pin TSSOP
SP3223EUCA-L	0°C to +70°C	20-pin SSOP
SP3223EUCA-L/TR	0°C to +70°C	20-pin SSOP
SP3223EUCY-L	0°C to +70°C	20-pin TSSOP
SP3223EUCY-L/TR	0°C to +70°C	20-pin TSSOP
SP3223EUEA-L	-40°C to +85°C	20-pin SSOP
SP3223EUEA-L/TR	-40°C to +85°C	20-pin SSOP
SP3223EUEY-L	-40°C to +85°C	20-pin TSSOP
SP3223EUEY-L/TR	-40°C to +85°C	20-pin TSSOP

Note: "-L" indicates lead free packaging, "/TR" is for tape and reel option

PRODUCT NOMENCLATURE



REVISION HISTORY

DATE	REVISION	DESCRIPTION
10-06-06	---	Legacy Sipex data sheet
Nov 2010	1.0.0	Convert to Exar data sheet format and remove EOL parts.
June 2012	1.0.1	Correct type error on page 1 pin diagram. Pin 9 should be R2IN not R1IN, Change ESD protection levels to IEC61000-4-2.

Notice

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Datasheet June 2012

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